

RF Power MOSFET Transistor 10 W, 2 - 175 MHz, 28 V

Rev. V1

Features

- N-Channel enhancement mode device
- DMOS structure
- Lower capacitances for broadband operation
- Common source configuration
- Low noise floor
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS AT 25° C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	2.8	A
Power Dissipation	P_D	35	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance	θ_{JC}	2	°C/W

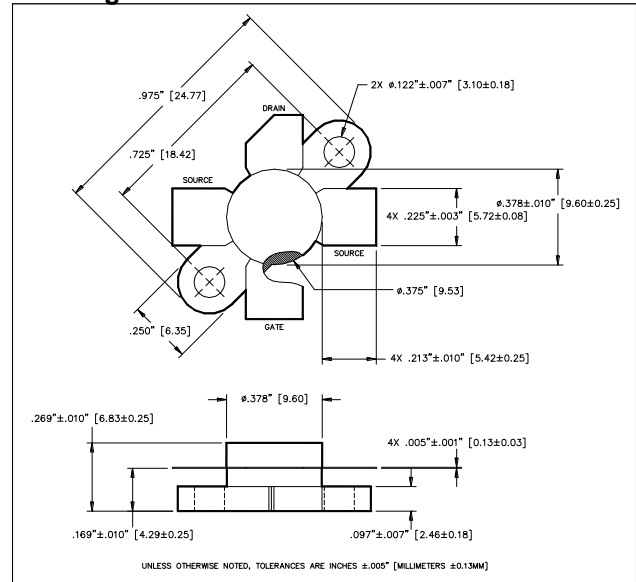
TYPICAL DEVICE IMPEDANCE

F (MHz)	Z_{IN} (Ω)	Z_{LOAD} (Ω)
30	20 - j11.0	23.0 + j3.0
50	24.0 - j15.0	19.0 + j5.0
100	18.0 - j18.0	14.0 + j6.0
200	12.0 - j19.0	9.0 + j5.0
$V_{DD} = 28V$, $I_{DQ} = 100mA$, $P_{OUT} = 10.0W$		

Z_{IN} is the series equivalent input impedance of the device from gate to source.

Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to ground.

Package Outline



LETTER DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.64	24.89	.970	.980
B	18.29	18.54	.720	.730
C	20.07	20.83	.790	.820
D	9.47	9.73	.373	.383
E	6.22	6.48	.245	.255
F	5.64	5.79	.222	.228
G	2.92	3.30	.115	.130
H	2.29	2.67	.090	.105
J	4.04	4.55	.159	.179
K	6.58	7.39	.259	.291
L	.10	.15	.004	.006

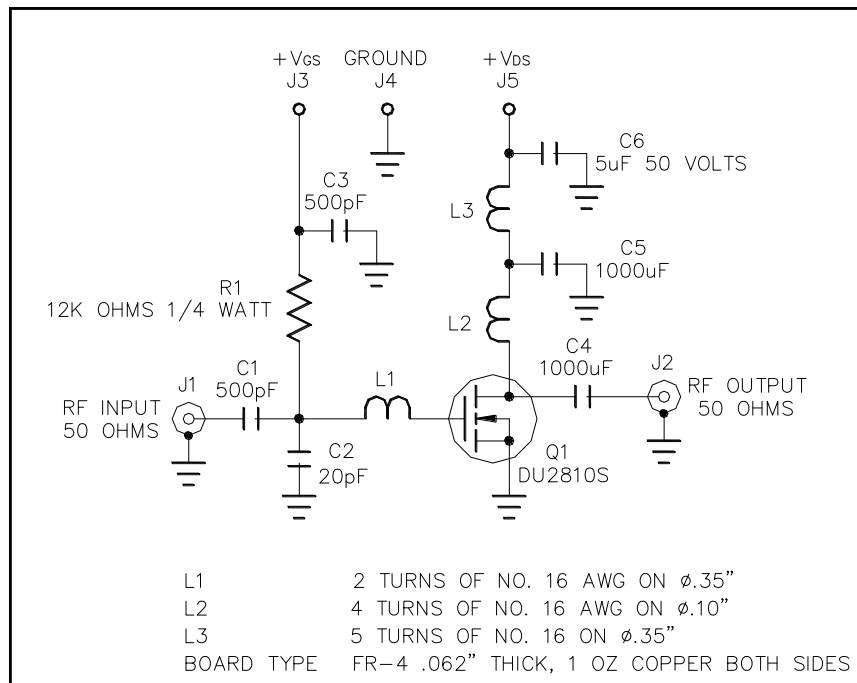
ELECTRICAL CHARACTERISTICS AT 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS} = 0.0 V$, $I_{DS} = 4.0 mA$
Drain-Source Leakage Current	I_{DSS}	-	2.0	mA	$V_{GS} = 28.0 V$, $V_{DS} = 0.0 V$
Gate-Source Leakage Current	I_{GSS}	-	2.0	μA	$V_{GS} = 20.0 V$, $V_{DS} = 0.0 V$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS} = 10.0 V$, $I_{DS} = 20 mA$
Forward Transconductance	G_M	160	-	S	$V_{DS} = 10.0 V$, $I_{DS} = 200 mA$, Pulsed 80-300 μs
Input Capacitance	C_{ISS}	-	14	pF	$V_{DS} = 28.0 V$, $F = 1.0 MHz$
Output Capacitance	C_{OSS}	-	10	pF	$V_{DS} = 28.0 V$, $F = 1.0 MHz$
Reverse Capacitance	C_{RSS}	-	4.6	pF	$V_{DS} = 28.0 V$, $F = 1.0 MHz$
Power Gain	G_P	13	-	dB	$V_{DD} = 28.0 V$, $I_{DQ} = 100 mA$, $P_{OUT} = 10 W$ $F = 175 MHz$
Drain Efficiency	η_D	55	-	%	$V_{DD} = 28.0 V$, $I_{DQ} = 100 mA$, $P_{OUT} = 10 W$ $F = 175 MHz$
Load Mismatch Tolerance	VSWR-T	-	20:1	-	$V_{DD} = 28.0 V$, $I_{DQ} = 100 mA$, $P_{OUT} = 10 W$ $F = 175 MHz$

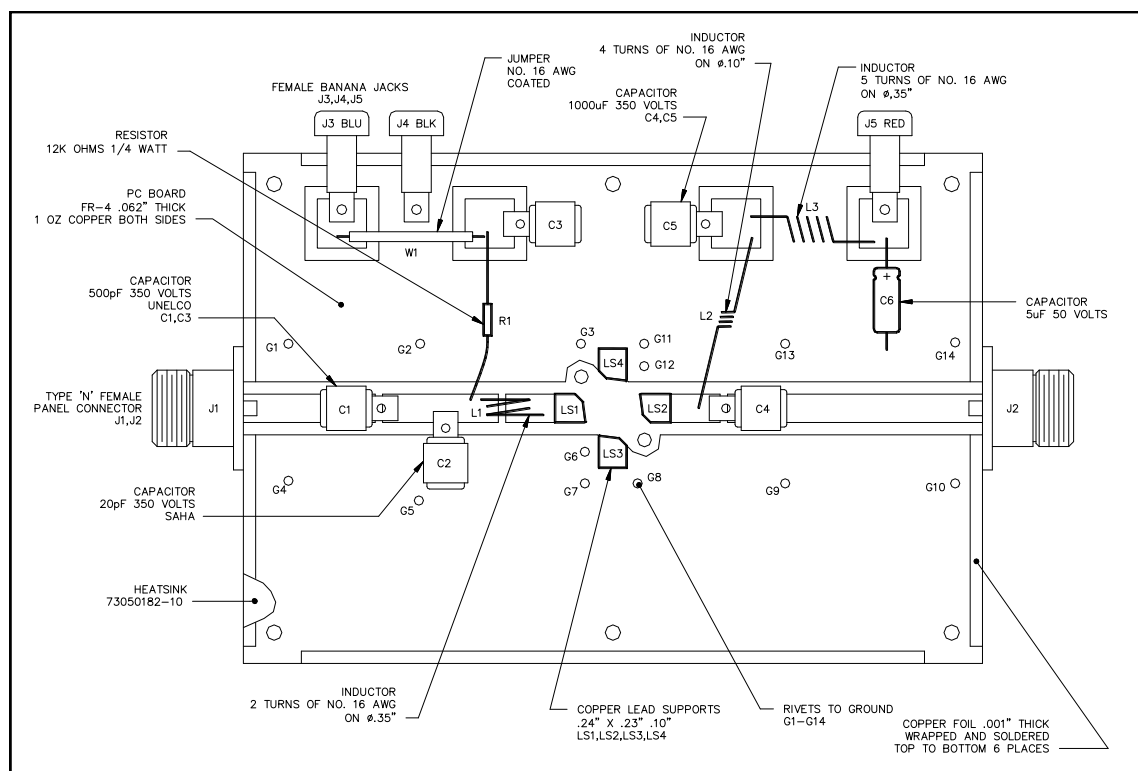
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TEST FIXTURE SCHEMATIC



TEST FIXTURE ASSEMBLY



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