High Speed 1:2 Demultiplexer **DMX-64**

Overview

General Description

The DMX-64 is the high speed ADSANTEC 5190B SiGe 1 :2 demultiplexer (DEMUX) chip in a connectorized module. The demultiplexer is a broadband 1:2 deserializer that converts a DC to 64 Gb/s input signal into two half rate output signals using a half rate clock. The DMX-64 can be operated single ended or differentially. The DMX-64 is suitable for laboratory testing and use in test equipment.

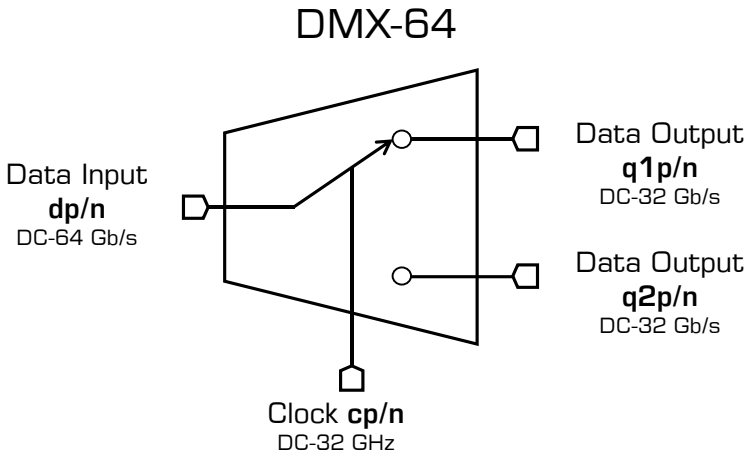
Features

- 64 Gb/s input data/ 32 Gb/s output data rate as a DEMUX
- Single Ended or Differential Operation
- Low Jitter

Applications

- Test Instrumentation
- High Speed Serializer/Deserializer
- Fiber Optic Test Systems

Functional Block Diagram



Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
DMX-64	64 Gb/s Connectorized Package	Module	RoHS	Active	5A991.b.1
ASNT-5190B	24 Pin Surface Mount	CQFP	See adsantec.com		

[1] Refer to our website for a list of definitions for terminology presented in this table.

215 Vineyard Court, Morgan Hill CA 95037 | Ph: 408.778.4200 | Fax: 408.778.4300 | info@markimicrowave.com

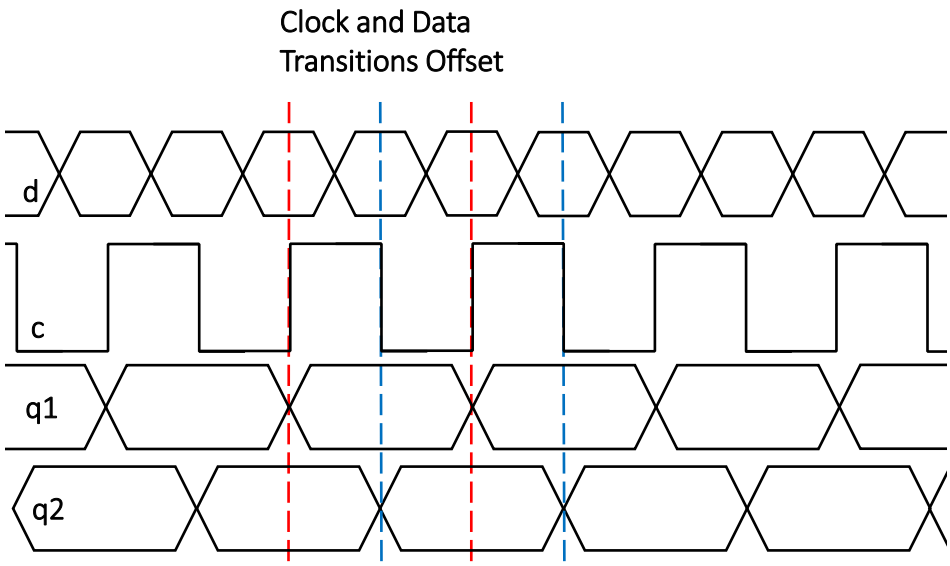
Application Information

Overview

The DMX-64 is a broadband demultiplexer module designed for use in a laboratory or test equipment environment. The module consists of an Adsantec ASNT-5190B broadband digital 1:2 demultiplexer chip fabricated in a SiGe process that is packaged with broadband bias circuitry and input/output connections to support operation up to 64 Gb/s on the input. All ports can be operated single ended or differentially with or without 50Ω loads and DC blocks (DCZM29F29 and DCZM24F24 DC blocks are recommended).

Operation as a Demultiplexer

To operate as a demultiplexer, connect port d to the high speed signal you would like to deserialize. The clock signal c must use a signal source at half the data rate, but with the same phase, to allow accurate clocking. The precise timing of the input signals is critical, as each zero crossing of the clock will cause the output signal to switch between input values. If the clock is not aligned with the center of the input erroneous output signals will occur. Below is the recommended timing diagram for operation as a Demux.

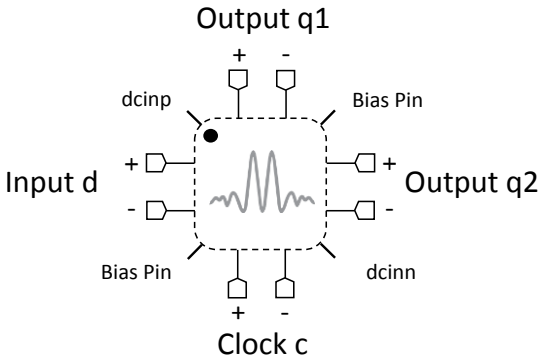


The duty cycle of the clock should be between 45% and 55%. The duty cycle can be adjusted by biasing the dcp and dcn pins between 0 and -3.3 V. If duty cycle adjustment is not required these pins may be left unconnected.

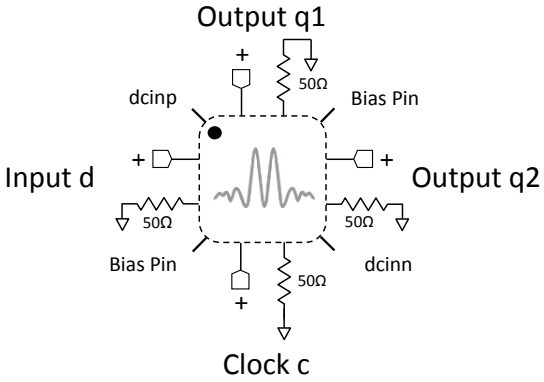
Port Configurations and Functions

Port Diagram

A top view of the DMX-64 package is shown below. The device is designed to work optimally with differential input and output signals, but can be used single ended with unused ports (either one) terminated in a 50Ω load.

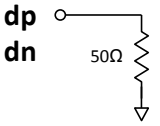
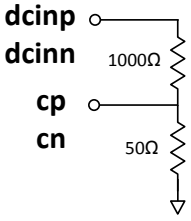
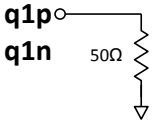
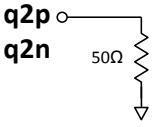


Differential I/O



Single Ended I/O

Port Functions

Port	Function (Multiplexer)	Description	Equivalent Circuit
dn **dp**	DC-64 Gb/s Data Input	d is a differential data input. Each port is terminated in 50Ω.	
cp **cn**	DC-32 GHz Clock Input	The transitions of the differential c signal controls whether the input signal is routed to q1 or q2. The dcin pins are optional and allow for compensation of the duty cycle distortion on the clock.	
dcinp **dcinn**	Clock control voltage		
q1p **q1n**	DC-32 GB/s Data Output	q1 is a differential data output. DC common mode voltage that can be blocked or terminated in a 50Ω load.	
q2p **q2n**	DC-32GB/s Data Output	q2 is a differential data output. DC common mode voltage that can be blocked or terminated in a 50Ω load.	

Specifications

Operating Conditions

Maximum/Minimum indicate limits, beyond which damage may occur to the device. Typical indicates recommended range. If typical value is not given, all values provide equivalent performance.

Parameter	Minimum	Typical	Maximum
DC parameters			
Supply Voltage (V)	-3.1	-3.3	-3.6
Supply Current (mA)		180	
Power Consumption (mW)		594	650
High Speed Input			
Differential Input Voltage Swing ports **d**, **c** (mV peak-peak)	50		
Single Ended Input Voltage Swing ports **d**, **c** (mV peak-peak)			1000
Input Datarate ports **d** (Gb/s)	DC		64
Input Common Mode Voltage Ports **d**, **c** (mV)	-800		0
Input Voltage Ports **dcinp/n** (V)	-3.3		0
High Speed Outputs			
Differential Output Voltage Swing ports **q1, q2** (mV peak-peak)		400	
Output Datarate ports **q1, q2** (Gb/s)	DC		32
Output Common Mode Voltage Port **q1, q2** (mV)		200	

Sequencing, DC Blocking, and Termination Requirements

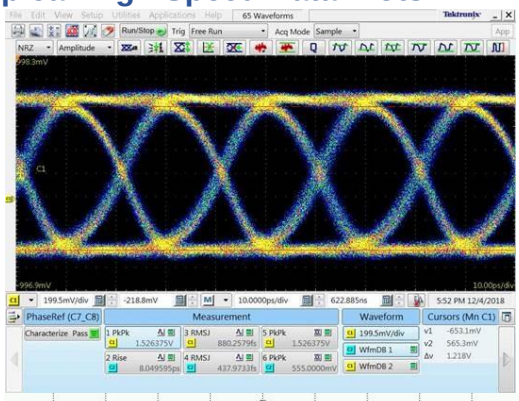
There is no requirement to apply power to the ports in a specific order.

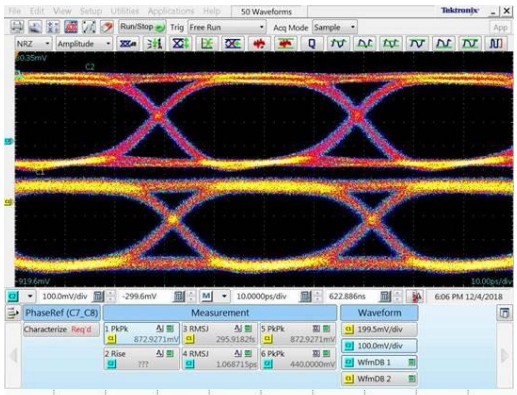
If operating single ended, a 50Ω termination on the unused output ports will significantly improve performance. Input ports may be terminated to improve noise performance.

DC blocks are required on inputs when common mode voltage will exceed maximum or minimum ratings. DC blocks are optional on output ports.

Typical High Speed Data Plots

50 Gb/s Data Input

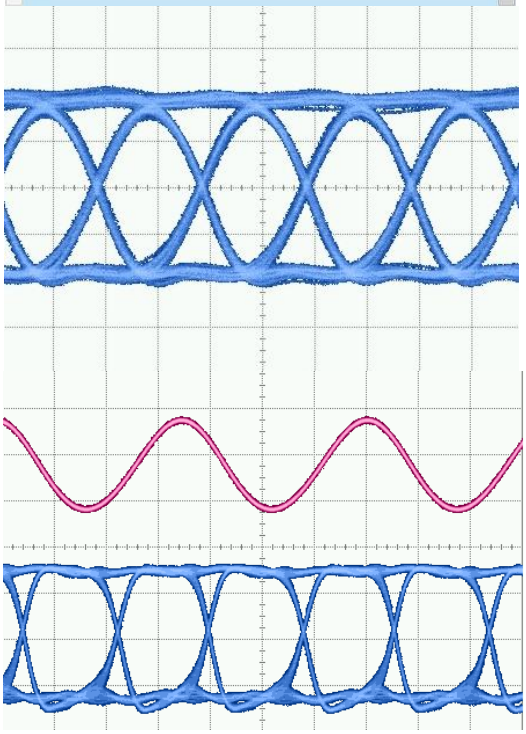


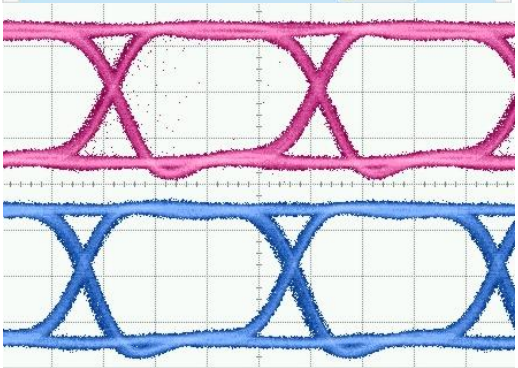


q1 output 25 Gb/s

q2 output 25 Gb/s

40 Gb/s Data Input



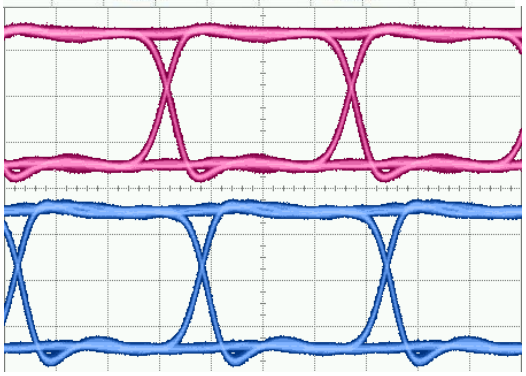


q1 output 20 Gb/s

q2 output 20 Gb/s

14 GHz Clock Input

28 Gb/s Data Input

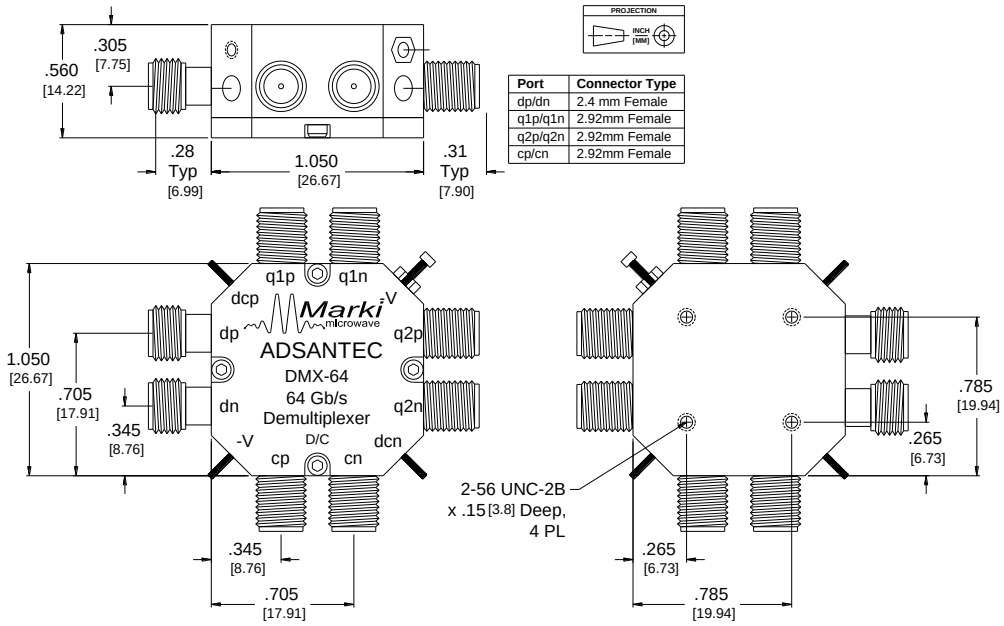


q1 output 14 Gb/s

q2 output 14 Gb/s

Mechanical Data

Package Outline Drawing



Package Information

Parameter	Details	Rating
Connector Torque	Maximum Acceptable Torque on Connectors	8 in-lb
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	TBD
Weight	Grams	31

Revision History

7/31/17 Initial Datasheet release Rev-

9/15/17 Added High Speed Plots Rev A