

MMIC 18-42GHz Quadrature Hybrid

MQH-1842

1 Device Overview

1.1 General Description

The MQH-1842 is a MMIC 18GHz - 42 GHz quadrature (90°) hybrid. Passive GaAs MMIC technology allows production of smaller constructions that replace larger form factor circuit board constructions. Tight fabrication tolerances allow for less unit to unit variation than traditional coupler technologies. The MQH-1842 is available as a wire bondable chip. Low unit to unit variation allow for accurate simulations using the provided S4P file taken from measured production units. Applications include single sideband upconverters, image rejection downconverters, IQ modulators, balanced amplifiers, microwave correlators, and microwave Butler matrices.

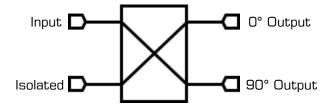


Bare Die

1.2 Features

- Designed for K/Ka-band applications
- High amplitude and phase balance
- High isolation
- Low insertion loss
- S4P data MQH-1842.zip

1.3 Functional Block Diagram



1.4 Part Ordering Options¹

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
MQH- 1842CH	Wire bondable die	СН	RoHS	Active	EAR99

¹ Refer to our <u>website</u> for a list of definitions for terminology presented in this table.



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Revision History

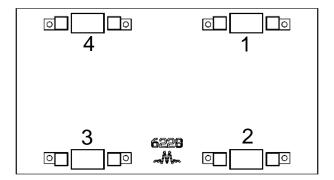
Revision Code Revision Date		Comment	
-	May 2018	Datasheet Initial Release	



2 Port Configurations and Functions

2.1 Port Diagram

A top-down view of the MQH-1842CH package outline drawing is shown below. The MMIC quadrature hybrid are passive reciprocal devices allowing any port to be used as the input.



2.2 Port Functions²

Port	Configuration A	Configuration B	Description	Equivalent Circuit
Port 1	Input	O° Output	Port 1 is DC short to port 3 and open to ground.	
Port 2	O° Output	Input	Port 2 is DC short to port 4 and open to ground.	Port 1⊶⊸Port 2
Port 3	90° Output	Isolated	Port 3 is DC short to port 1 and open to ground.	Port 4∘— Port 3
Port 4	Isolated	90° Output	Port 4 is DC short to port 2 and open to ground.	
Pad	Ground	Ground	CH package ground path is provided through the substrate and ground bond pads.	Pad∘—_

 $^{^{\}rm 2}$ Each configuration describes a different application of the same product.



Port	Configuration Configuration C		Description	Equivalent Circuit
Port 1	O° Output	Isolated	Port 1 is DC short to port 3 and open to ground.	
Port 2	Isolated	90° Output	Port 2 is DC short to port 4 and open to ground.	Port 1⊶—⊸Port 2
Port 3	Input	Input O° Output Port 3 is DC short to port 1 and open to ground.		Port 4 Port 3
Port 4	90° Output	Input	Port 4 is DC short to port 2 and open to ground.	
Pad	Ground	Ground	CH package ground path is provided through the substrate and ground bond pads.	Pad⊶



3 Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
DC Current, Any Port	TBD	mA
Power Handling, at Any Port	TBD	dBm
Operating Temperature	-55 to +100	°C
Storage Temperature	-65 to +125	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	N/A

3.3 Electrical Specifications³

The electrical specifications apply at $T_A=+25^{\circ}C$ in a 50Ω system.

Min and Max limits are guaranteed at $T_A\!\!=\!+25^{\circ}\text{C}.$

Parameter	Frequency (GHz)	Min	Тур.	Max	Units
Coupling			3		dB
Nominal Phase Shift			90		Degrees
Amplitude Balance			±1.5	±2.5	dB
Phase Balance	18-42		±4	±12	Degrees
Excess Through Line Insertion Loss			1.5	3	dB
Isolation		7.5	15		dB
VSWR			1.5		
Impedance			50		Ω

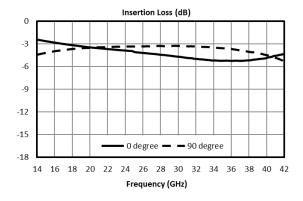
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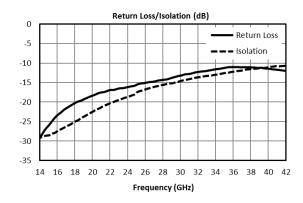
 $^{^{3}}$ Quadrature hybrid is reciprocal. Reverse measurement is equivalent to forward measurement.



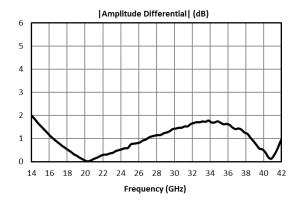
3.4 Typical Performance Plots

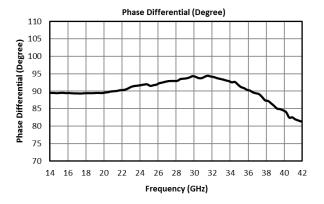
3.4.1 Insertion Loss, Return Loss, and Isolation





3.4.2 Amplitude and Phase Balance







4 Die Mounting Recommendations

4.1 Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 $^{\circ}$ C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

Circuit Considerations — $50~\Omega$ transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

4.2 Handling Precautions

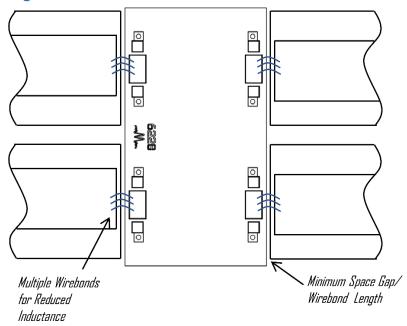
General Handling

Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

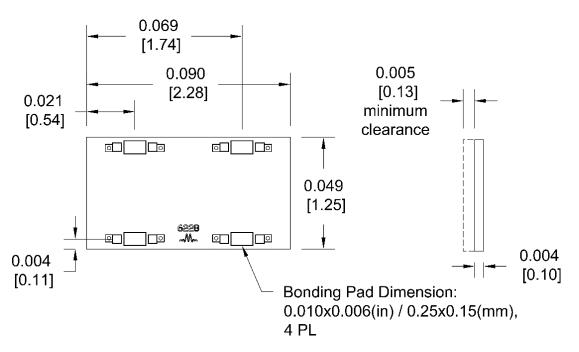


4.3 Bonding Diagram



5 Mechanical Data

5.1 CH Package Outline Drawing



- 1. CH Substrate material is 0.004 in thick GaAs.
- 2. I/O trace finish is 5 microns Au. Ground plane finish is 4 microns Au.

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