TGC4603-SM

Ka-band Doubler with 1 Watt Amplifier

Applications

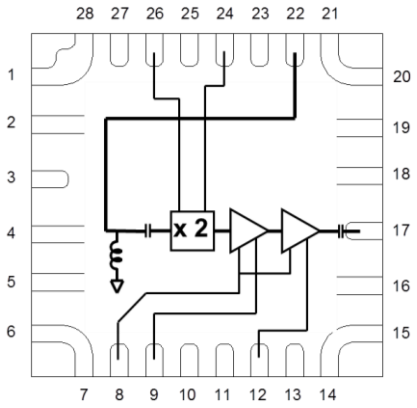
- Ka-band VSAT

28-pin 5x5mm QFN package

Product Features

- RF Output Frequency Range: 27 – 32 GHz
- Input Frequency Range: 13.5 – 16 GHz
- 31.5 dBm Pout
- 70 dBc Input Frequency Isolation
- Bias: VD1=VD2 = 6 V, ID1+ID2 = 1100 mA, VDX2 = 6V, IDX2 = 100mA, VGX2 = -1.2 V, VGPA = -0.6 V Typical
- Package Dimensions: 5 x 5 x 1.3 mm

Functional Block Diagram



General Description

The Qorvo TGC4603-SM packaged MMIC combines a frequency doubler with a multi-stage amplifier, operating at input frequencies of 13.5 - 16 GHz. With greater than 70 dBc isolation between the input and the doubled output frequency, the TGC4603-SM achieves more than 1 Watt output power, with only 3 dBm input power. This performance makes this doubler ideally suited for Ka-Band satellite ground terminal applications. The TGC4603-SM provides the frequency doubling function in a compact 5 mm x 5 mm package footprint.

The TGC4603-SM is RoHS compliant.

Evaluation boards are available upon request.

Pin Configuration

Pin No.	Label
1,2,3,4,5,6,7,14,15, 16,18,19,20,21,23, 28	GND
8	VGPA
9	VD1
10,11,13,25,27	N/C
12	VD2
17	RFOUT
22	RFIN
24	VDX2
26	VGX2

Ordering Information

Part No.	ECCN	Description
TGC4603-SM	3A001.b.2.c	13.5-16 GHz Doubler with 1 Watt Amplifier

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, VD1, VD2, VDX2	6.5 V
Gate Voltage, VGPA, VGX2	-2.5 to 0.5 V
Drain to Gate Voltage	12 V
Drain Current, ID1	500 mA
Drain Current, ID2	1400 mA
Gate Current, IGPA	-5 to +20
Gate Current, IGX2	-5 to +20
RF CW Input Power	18 dBm
Channel Temperature, Tch	200 ˚C
Mounting Temperature (30 sec)	260 ˚C
Storage Temperature	-40 to 150 ˚C

Notes

1. Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
VD1, VD2, VDX2		6	6.5	V
ID1+ID2 (P_in = 3 dBm)		1100		mA
IDX2		125		mA
VGPA		-0.6		V
VGX2		-1.2		V
IGPA		6		mA
IGX2		0.1		mA

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Specifications

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, VD1=VD2=VDX2= 6 V, ID1+ID2= 1100 mA, IDX2= 125 mA, VGX2 = -1.2 V, VGPA= -0.6 V typical.

Parameter	Min	Typical	Max	Units
Input Frequency	13.5		16	GHz
Output Frequency	27		32	GHz
Output Power, P_in = 3 dBm		31.5		dBm
Fundamental Output Rejection		75		dBc
Third Harmonic Output Rejection		70		dBc
Input Return Loss		-10		dB
Output Return Loss		-10		dB

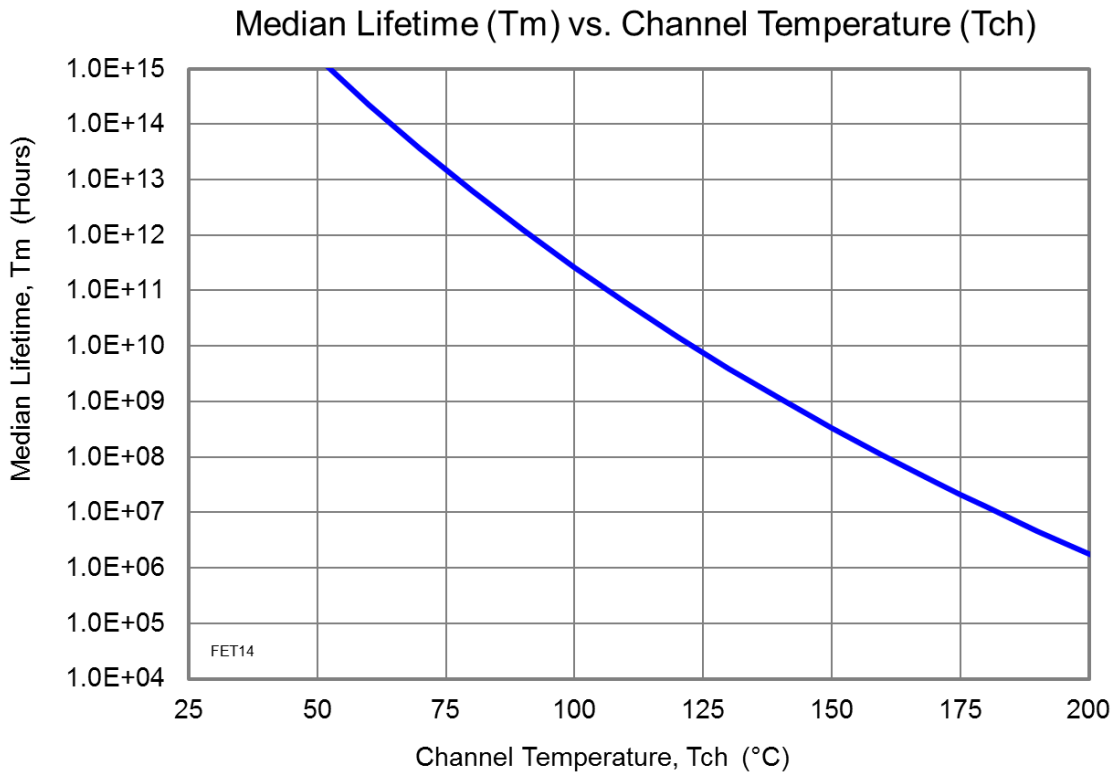
Specifications

Thermal and Reliability Information

Parameter	Condition	Rating
Thermal Resistance, θ_{JC}, measured to back of package	Tbase = 85 °C	θ_{JC} = 14 °C/W
Temperature (Tch), and Median Lifetime (Tm) Under RF Drive	Tbase = 85 °C, VD1=Vd2=VDX2=6 V, Id = 1430 mA, Pdiss= 8.58 W	Tch = 190 °C Tm = 4.6E6 Hours

Notes:

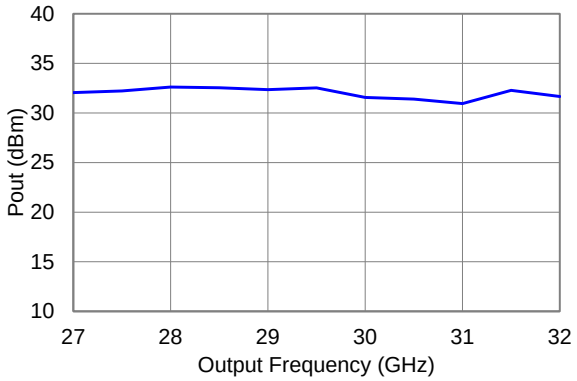
1. Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.
2. Channel temperature must not exceed maximum ratings.



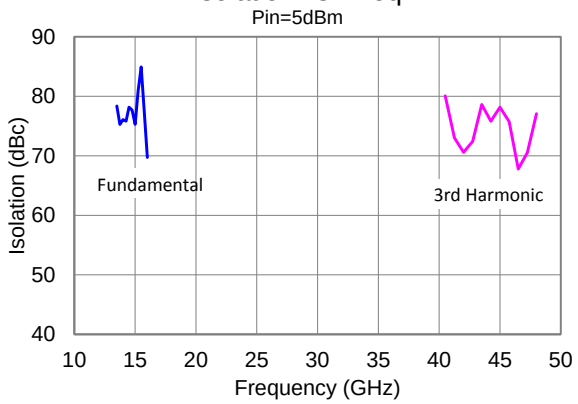
Typical Performance

Test conditions unless otherwise noted: 25 °C, VD1=VD2=VDX2= 6 V, ID1+ID2= 1100 mA, IDX2= 125 mA, VGX2 = -1.2 V, VGPA= -0.6 V typical.

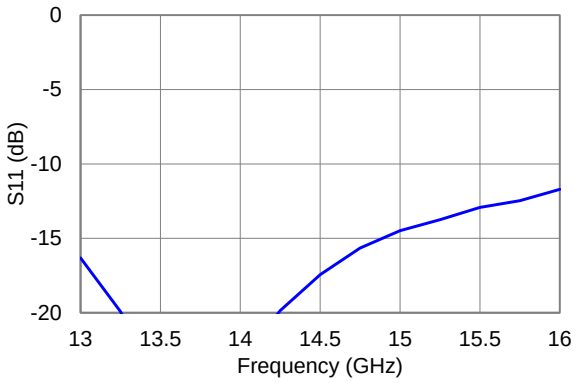
Output Power vs. Freq



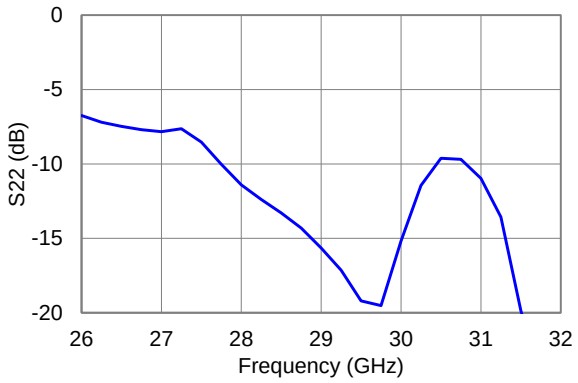
Isolation vs. Freq



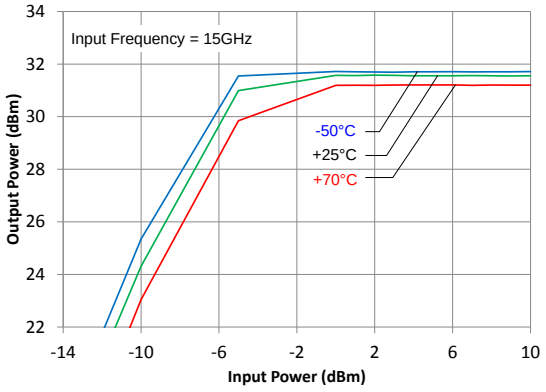
Input Return Loss vs. Freq



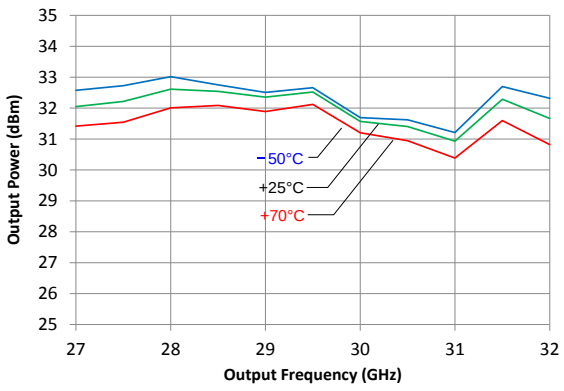
Output Return Loss vs. Freq



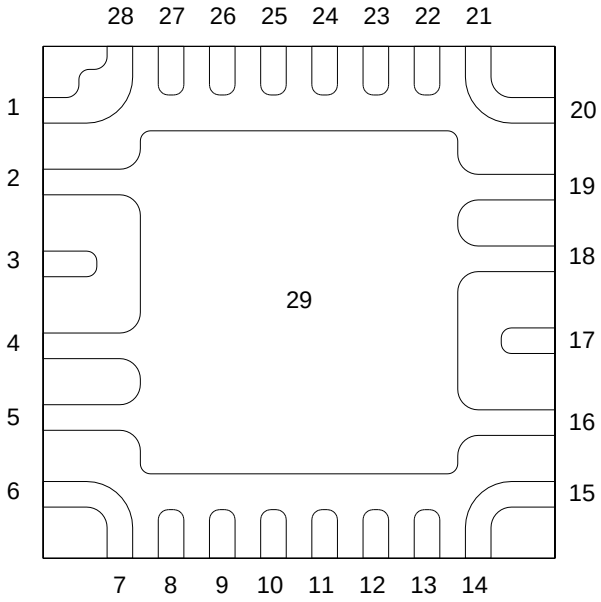
Pin vs. Pout over Temperature



Output Power vs. Freq over Temperature



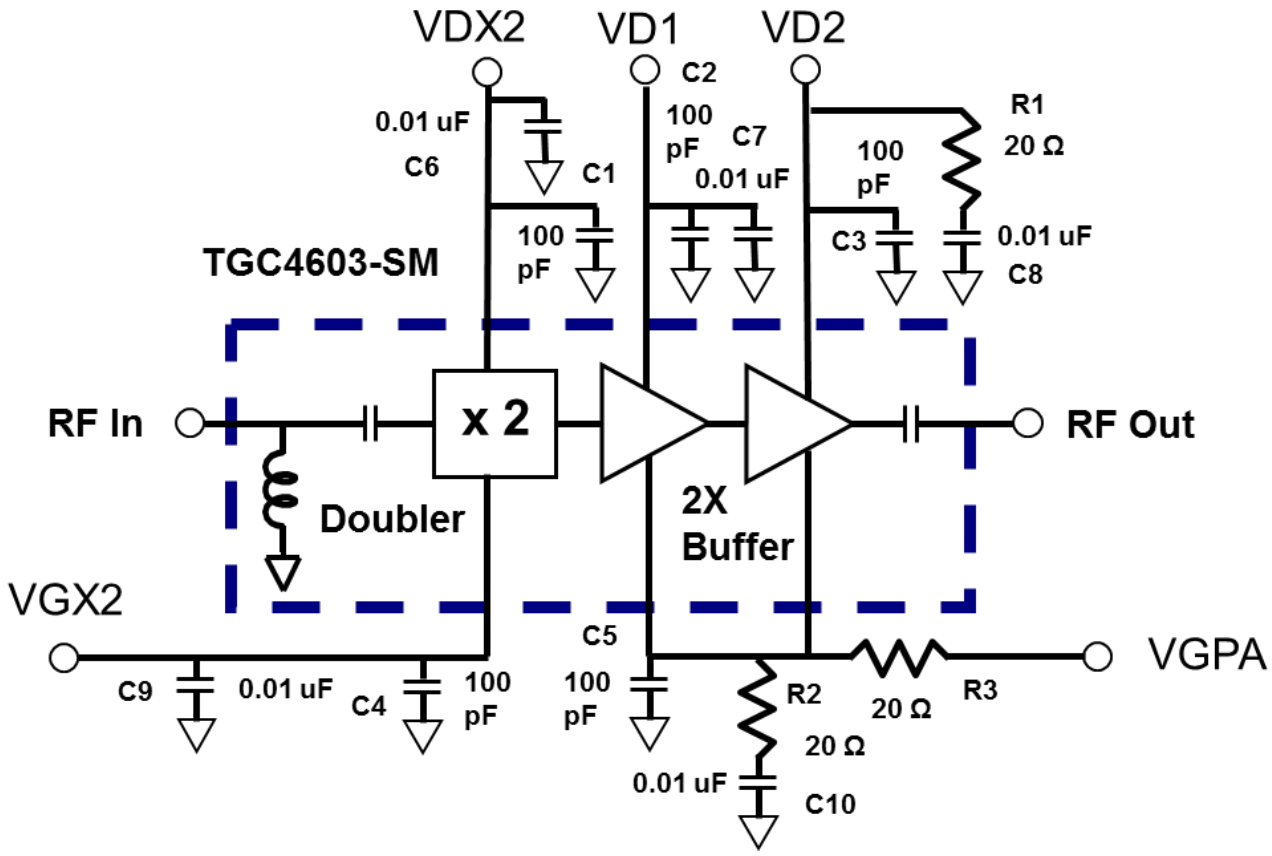
Pin Description



Top view

Pin	Symbol	Description
1,2,3,4,5,6,7,14,15, 16,18,19,20,21,23,28	GND	Ground. Must be grounded on PCB
8	VGPA	Gate voltage for Power Amplifier. See Application Circuit on page 7
9	VD1	Drain voltage for Power Amplifier. See Application Circuit on page 7
10,11,13,25,27	N/C	No internal connection. May be left open on the PCB.
12	VD2	Drain voltage for Power Amplifier. See Application Circuit on page 7
17	RFOUT	RF Output matched to 50 ohms.
22	RFIN	RF Input matched to 50 ohms.
24	VDX2	Drain voltage for Doubler circuit. See Application Circuit on page 7
26	VGX2	Gate voltage for Doubler circuit. See Application Circuit on page 7
29	GND	Backside Paddle Ground. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 10 for suggested footprint.

Application Circuit



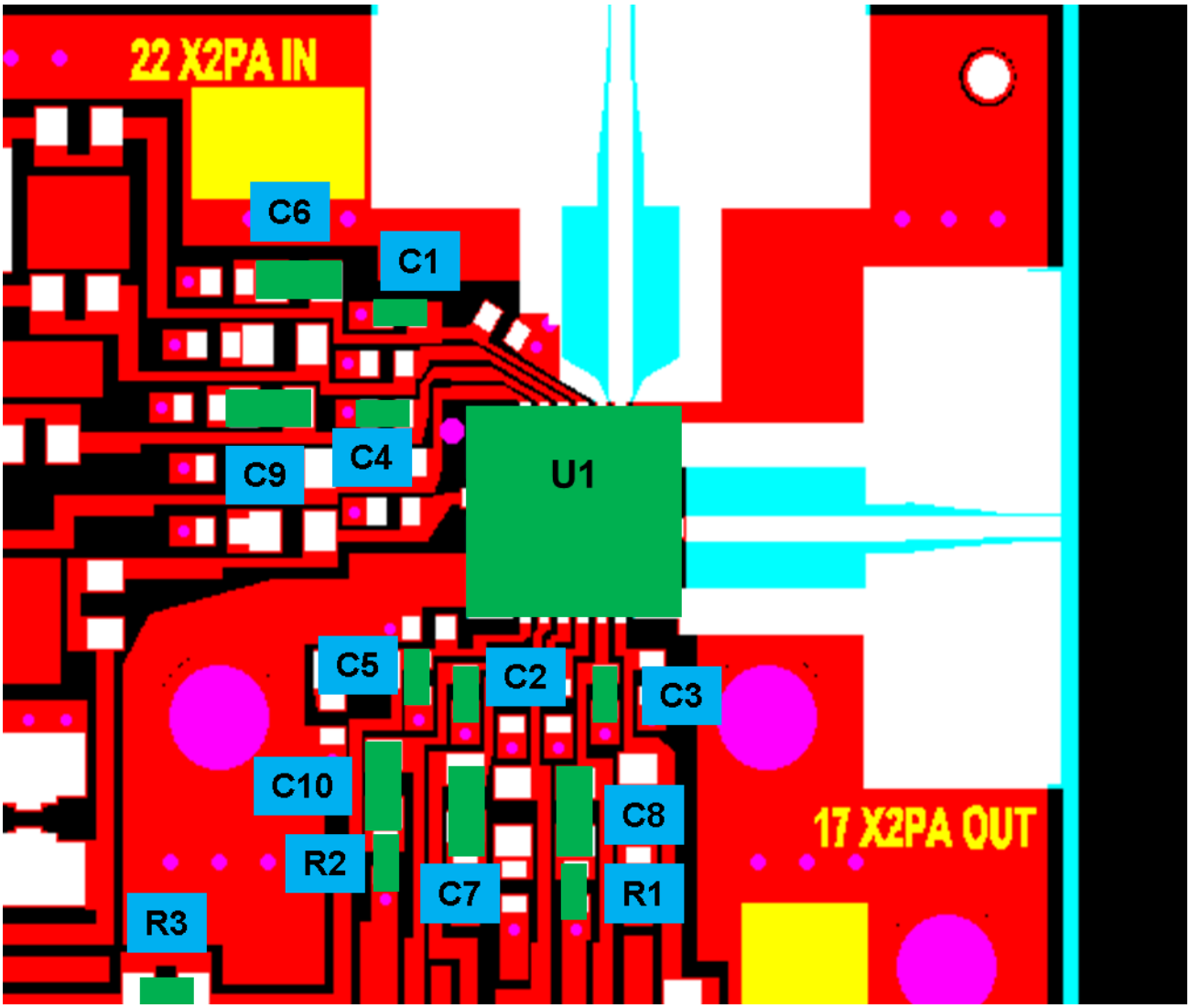
Bill of Material:

Ref Des	Description	Value	Size	Source
C1 – C5	Capacitor	100pF	0402	Various
C6 – C10	Capacitor	0.01uF	0402	Various
R1 – R3	Resistor	20 ohm	0402	Various
U1	TGC4603-SM		5x5mm	Qorvo

Application Circuit

PC Board Layout: Evaluation Board

Top RF layer is 0.010” thick Rogers RO3203, ϵr = 3.0. Metal layers are 0.5-oz copper. Microstrip 50 Ω line detail: width = 0.025”



Application Circuit

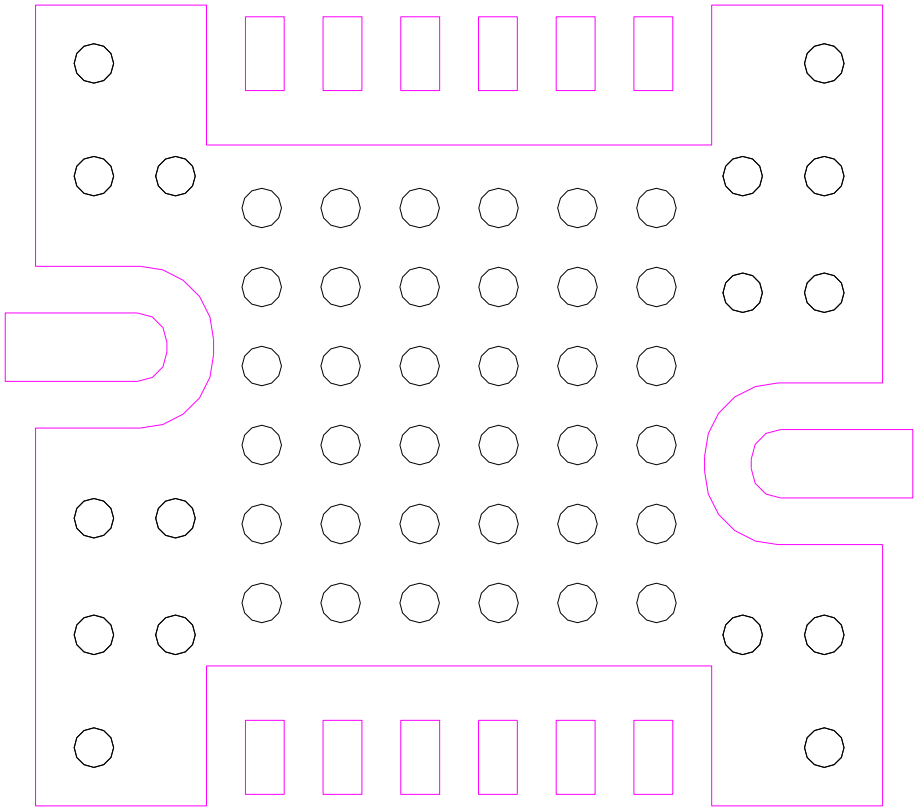
Evaluation Board Bias Procedures

Laboratory Bias-up Procedure	Laboratory Bias-down Procedure
Set VGX2 to -1.2 V	Turn off RF supply
Set VGPA to -1.5 V (pinch-off)	Set VGPA to -1.5 V
Set VD1, VD2 and VDX2 to 6 V	Turn VD1, VD2, and VDX2 to 0 V
Adjust VGPA more positive until target ID1q+ID2q quiescent current reaches 590mA.	Turn VGX2 to 0 V
Apply RF signal to RF Input.	Turn VGPA to 0 V

Mechanical Information

PCB Mounting Pattern

All dimensions are in millimeters

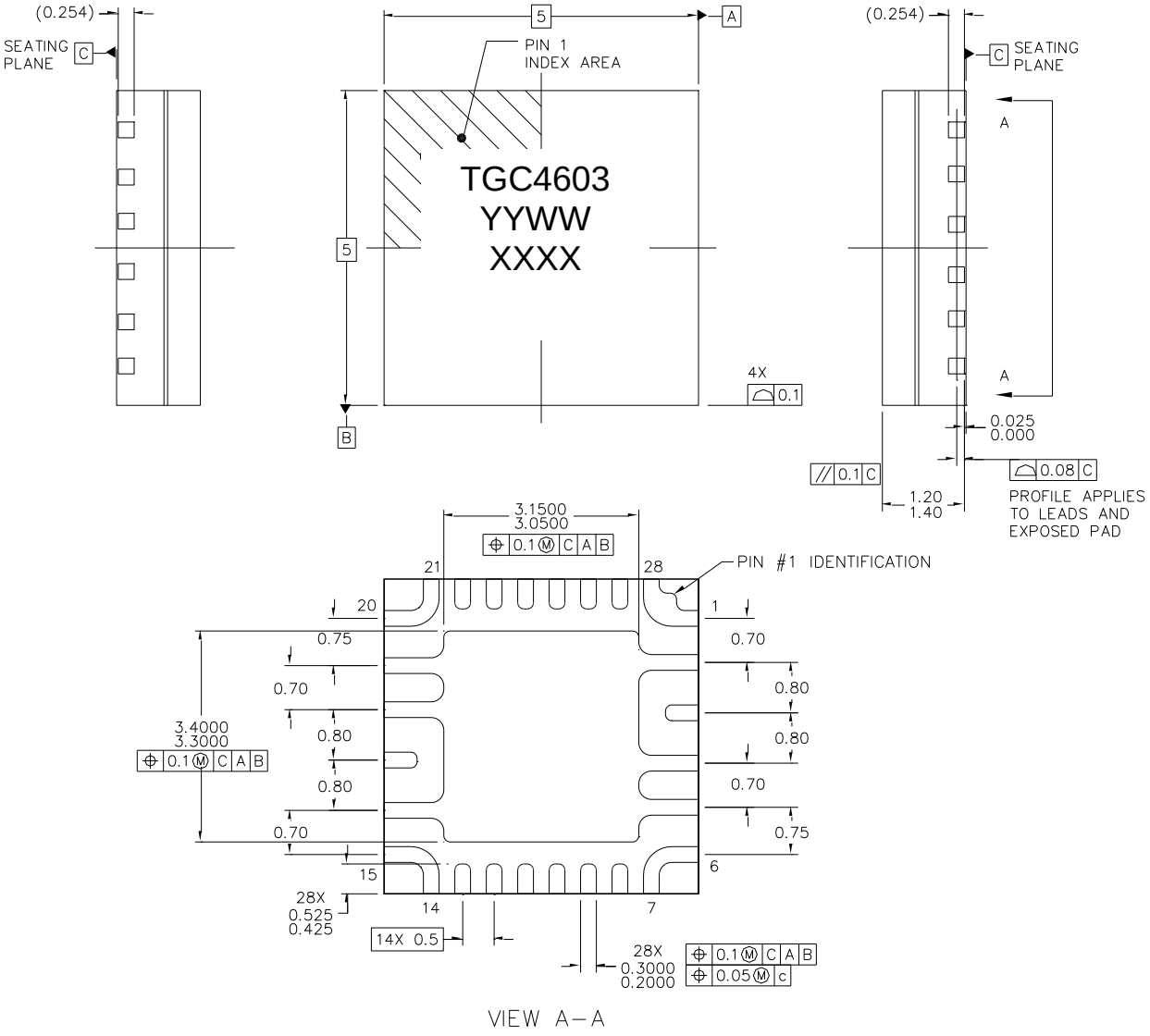


Notes:

1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
2. One ounce Cu plating inside vias is recommended. Vias shown are 0.254 mm (0.010”) diameter on 0.5 mm (0.020”) centers.
3. Ground / thermal vias are critical for the proper performance of this device. Vias have a final plated thru diameter of approximately 0.2 mm (0.008”).

Mechanical Information

Package Information and Dimensions



Notes:

1. Dimensions are in mm.
2. Tolerances: +/- 0.030 mm unless specified otherwise

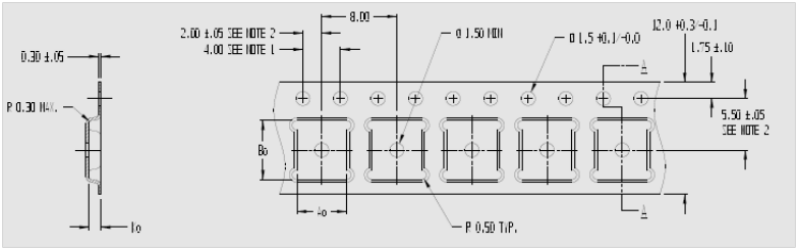
The TGC4603-SM will be marked with the “YYWW” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the year the part was manufactured, the “WW” is the work week and the “XXXX” is the last 4 digits of the lot number.

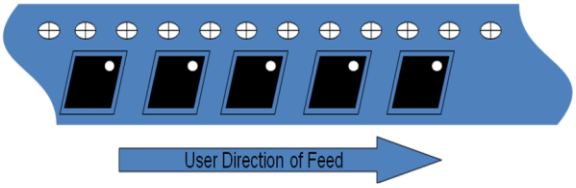
This package is lead-free/RoHS-compliant with a copper alloy base (CDA194), and the plating material on the leads is NiPdAu. It is compatible with a lead-free (maximum 260 °C reflow temperature) soldering process.

Tape and Reel Information

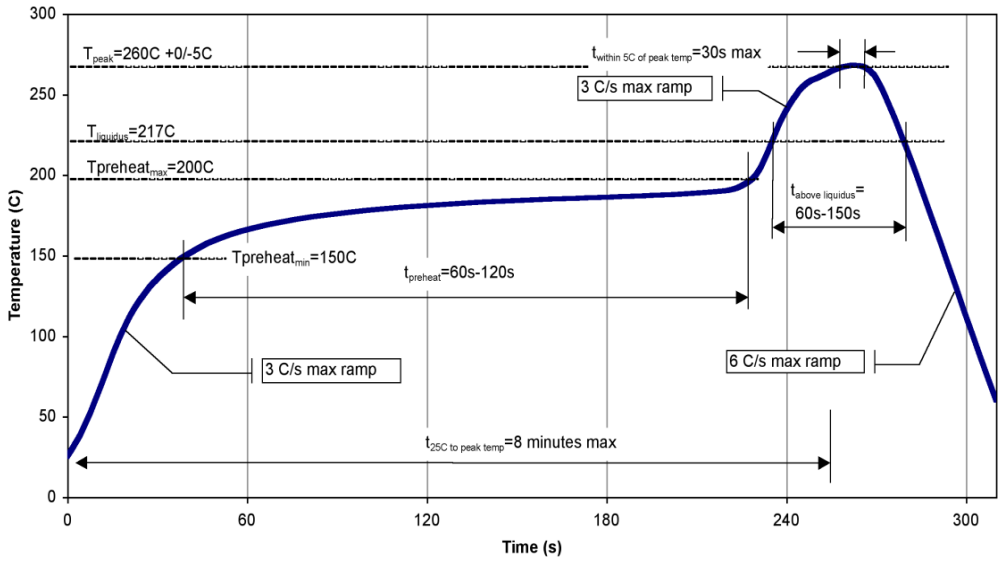
Standard T/R size = 200 pieces on a 7” reel.

Material		Cavity (mm)				Distance Between Centerline (mm)		Carrier Tape (mm)	Cover Carrier (mm)
Vendor	Vendor P/N	Length (A0)	Width (B0)	Depth (K0)	Pitch (P1)	Length direction (P2)	Width Direction (F)	Width (W)	Width (W)
Tek-Pak	QFN0500X0500F-L500	5.3	5.3	1.65	8.0	2.00	5.50	12.0	9.20





Recommended Soldering Temperature Profile



Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1A
Value:	450 V
Tests:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

MSL Rating

The part is rated Moisture Sensitivity Level 1 at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce 3A001.b.2.c

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°C

Use of no clean solder to avoid washing is required
Ultrasonic cleaning is prohibited

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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For technical questions and application information:

Email: applications.engineering@qorvo.com

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