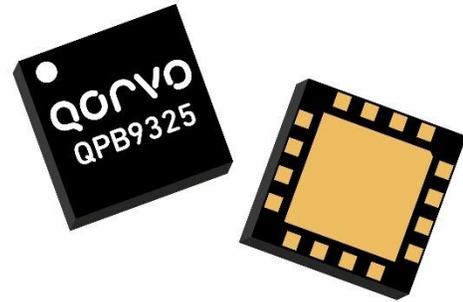


Product Overview

The Qorvo® QPB9325 is a highly integrated front-end module targeted for TDD macro or picocell base stations. The LNA switch module integrates RF functional blocks such as a pin-diode based high power switch capable of handling up to 52 W with an LTE signal (8 dB PAR) along with two LNA stages. Further integration is also implemented where the pin diode driver and dc-dc converter circuits are implemented inside the module to enable only the need for an external 5 V power supply. The control voltage for the switch and gain control. mode is with 3.3 V logic.

The QPB9325 can be utilized across the 3.6-3.8 GHz range to provide 1.2 dB noise figure for operation in the receive mode and 0.5 dB insertion loss in the transmit mode. The LNAs utilize Qorvo’s high performance E-pHEMT process while the switch allows for power levels up to 360 W peak power to be routed to an external load termination.

The QPB9325 is packaged in a RoHS-compliant, compact 8x8 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based architectures.

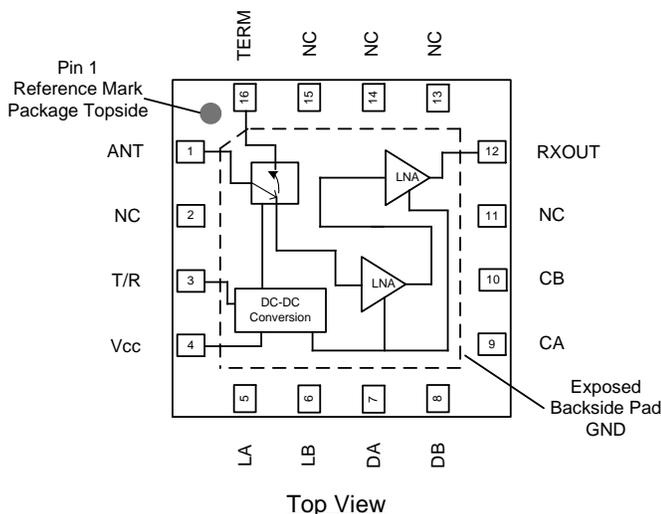


16 Pin 8 mm x 8 mm Leadless SMT Package

Key Features

- 3.6-3.8 GHz frequency range
- Integrates a high power switch, two LNA stages, pin diode driver circuits, and dc converter
- Ideal for TDD systems with an isolator
- Only requires a 5 V supply with 3.3 V logic Ctrl.
- Max RF Input power: 52 W Pavg (8 dB PAR)
- 34.1 dB gain
- 1.2 dB noise figure
- -2.2 dBm IIP3 (Rx mode)
- 0.5 dB Insertion Loss (Tx mode)
- Compact package size, 8x8 mm

Functional Block Diagram



Applications

- Wireless Infrastructure
- Macro or picocell base stations
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9325TR13	2500 pcs on a 13" reel
QPB9325EVB	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-50 to +150 °C
Max Operating Temperature	+115 °C
V _{CC}	+6 V
RF at ANT (Tx Mode) ⁽¹⁾	+47.2 dBm
RF at ANT (Tx Mode) ⁽²⁾	+44.2 dBm
RF at ANT (Rx Mode) ⁽²⁾	+20 dBm

Notes:

- 10s, 8 dB PAR, 88% duty cycle, +100 °C, 1CH LTE
- Indefinitely, 8 dB PAR, 88% duty cycle, +100 °C, 1CH LTE

Operation of this device outside the parameter ranges given above may cause permanent damage.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} = +5.0 V, Temp. = +25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		3600		3800	MHz
Test Frequency			3700		MHz
Gain	Rx mode	31	34.1		dB
Gain Flatness	Rx mode		1.0		dB
Noise Figure	Rx mode		1.2	1.65	dB
Input IP3	Rx mode, Pin/tone = -33dBm, Δf = 1MHz	-10	-2.2		dBm
Input P1dB	Rx mode	-20	-15		dBm
Input Return Loss (ANT)	Rx mode		30		dB
Output Return Loss (Rx Out)	Rx mode		26		dB
Reverse Isolation	Rx mode		58		dB
Insertion Loss	Tx mode		0.5	1.0	dB
Input P0.1dB	Tx mode		>+46.6		dBm
Return Loss (ANT, TERM)	Tx mode		25		dB
Operating Current	Rx mode		240		mA
Operating Current	Tx mode		140	150	mA
Switching Speed (ANT to Rx Out)	RF<0.1dB after T/R command		2		uS
Switching Speed (ANT to Term)	RF<0.1dB after T/R command		1		uS
Switching Speed (ANT to Rx Out/Term)	ANT to RXOUT/TERM with RF<0.5dB after DC turn on		1		s
In Band Spurious Emission ⁽⁴⁾	Rx Mode at Rx out with Pin = -49dBm ⁽⁵⁾		-85		dBc
Out of Band Emissions ⁽⁶⁾	Rx Mode at Rx out from DC to 12275MHz		-73		dBm
Thermal Resistance	Rx mode			22	°C/W
Thermal Resistance	Tx mode			22	°C/W

Notes:

- Pin is a CW signal swept from 3.6 to 3.8GHz. Spec refers to any spurious mixing product that occurs from 3.6 to 3.8GHz.
- Recommend to follow Qorvo EVB layout for lowest spur level any deviation can increase spur level.
- Measure Pout with IBW = 4.5MHz over frequency range with no input power applied.

Recommended Operating Conditions

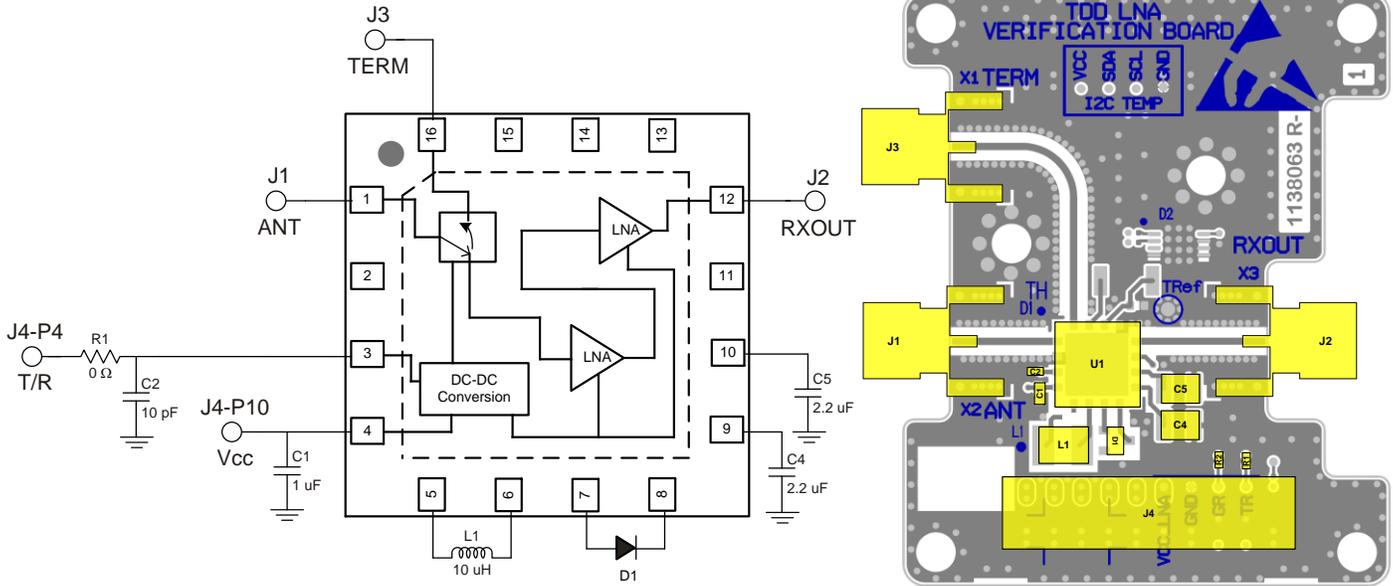
Parameter	Min	Typ	Max	Units
V _{CC}	+4.75	+5	+5.25	V
T/R Mode Low Voltage	0		0.8	V
T/R Mode High Voltage	2.0		3.6	V
T _{CASE}	-40		+105	°C
Tj for >10 ⁶ hours MTTF ⁽³⁾			+190	°C

Notes:

- For RX Mode operation

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Application Circuit Schematic and Layout



Note:
L1 is placed 5mm from bottom edge of U1 to top edge of L1 for in band spur suppression.

Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power Switch LNA Module	Qorvo	QPB9325
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 μF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 μF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	n/a	Diode, 200 V 200 mA SOT23	Various	
L1	10 μH	Inductor, Power, 10 μH, 20%, 0.84 A	Coilcraft	LPS4018-103ML

Logic Table

Parameter	High	Low
T/R	Rx Mode	Tx Mode

Typical Performance – Rx Mode

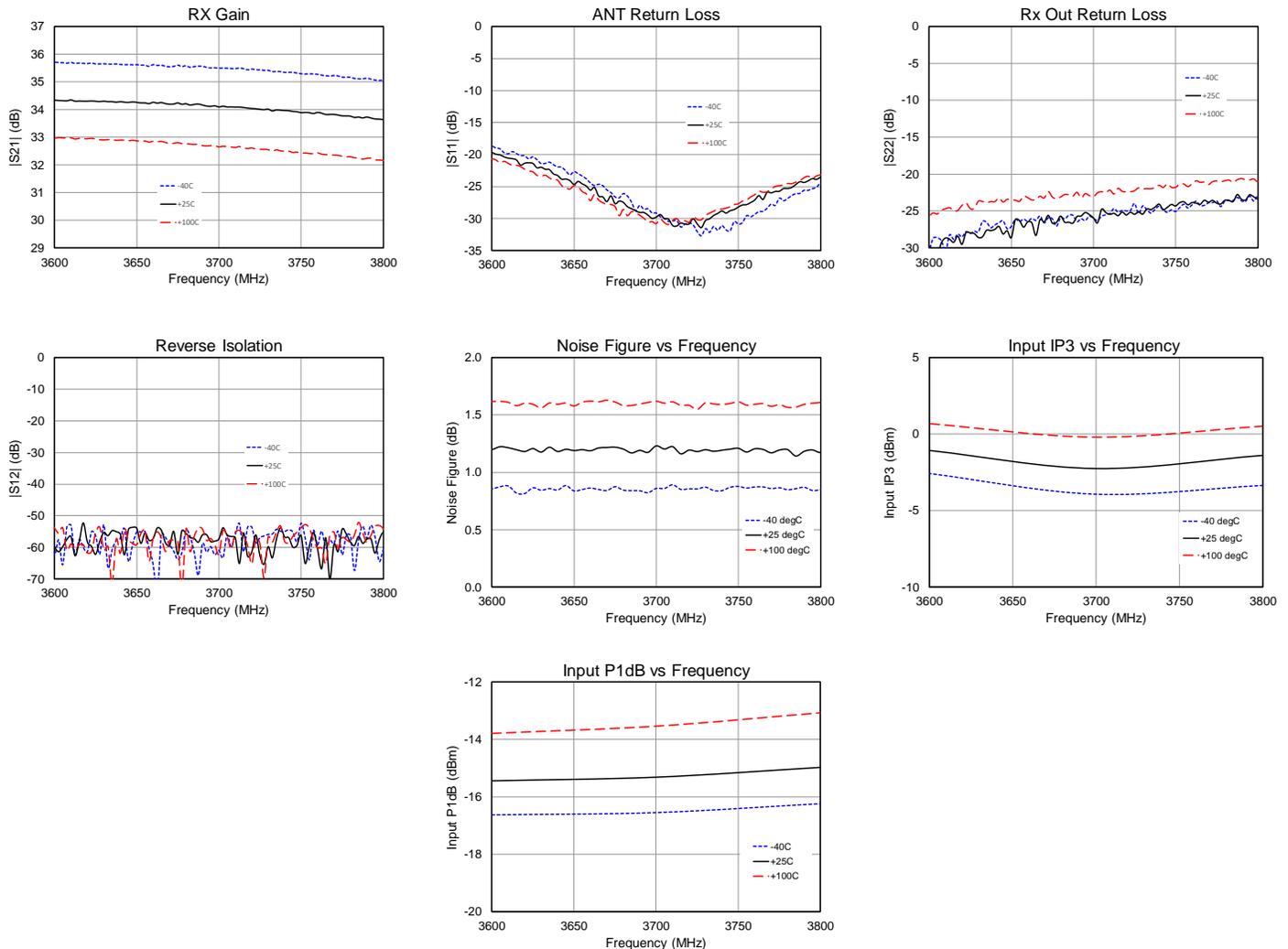
Parameter	Conditions ⁽¹⁾	Typical Value			Units
Frequency		3600	3700	3800	MHz
Gain		34.3	34.1	33.6	dB
Input IP3	Pin = -33 dBm/tone, Δf=1 MHz	-1.1	-2.2	-1.4	dBm
Input P1dB		-15.4	-15.3	-15.0	dBm
Noise Figure	De-embedded from Evaluation board PCB	1.2	1.2	1.2	dB
Return Loss	ANT port	20	30	24	dB
Return Loss	Rx Out port	30	26	24	dB
Reverse Isolation	Rx Out to ANT port	58	58	58	dB

Notes:

- Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $T/R = 3\text{ V}$, Temp. = $+25\text{ }^{\circ}\text{C}$

Performance Plots – Rx Mode

Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $T/R = 3\text{ V}$; Temp. = $+25\text{ }^{\circ}\text{C}$



Typical Performance – Tx Mode

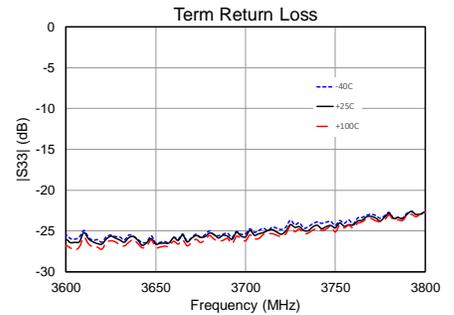
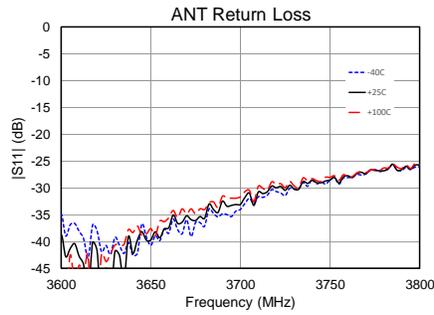
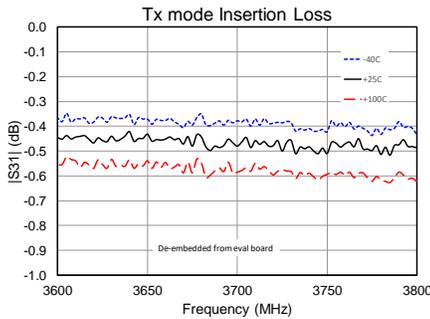
Parameter	Conditions ⁽¹⁾	Typical Value			Units
Frequency		3600	3700	3800	MHz
Insertion Loss	De-embedded from Evaluation board PCB	0.5	0.5	0.5	dB
Input P0.1dB compression	Pin = +46.6 dBm	0	0	0	dB
Return Loss	ANT port	40	33	26	dB
Return Loss	TERM port	26	25	23	dB

Notes:

1. Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $T/R = 0\text{ V}$, Temp. = $+25\text{ }^{\circ}\text{C}$

Performance Plots – Tx Mode

Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $T/R = 0\text{ V}$; Temp. = $+25\text{ }^{\circ}\text{C}$

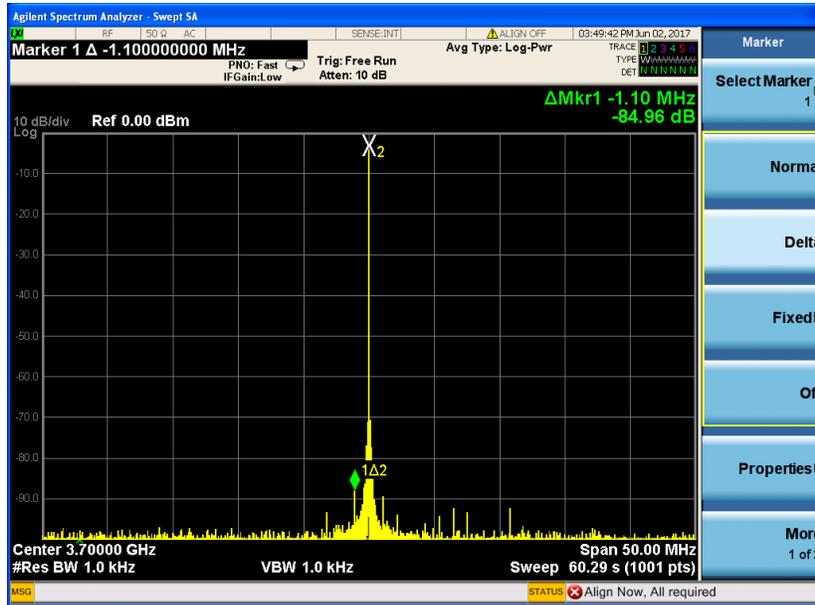


Application Circuit for Reduced Spurious

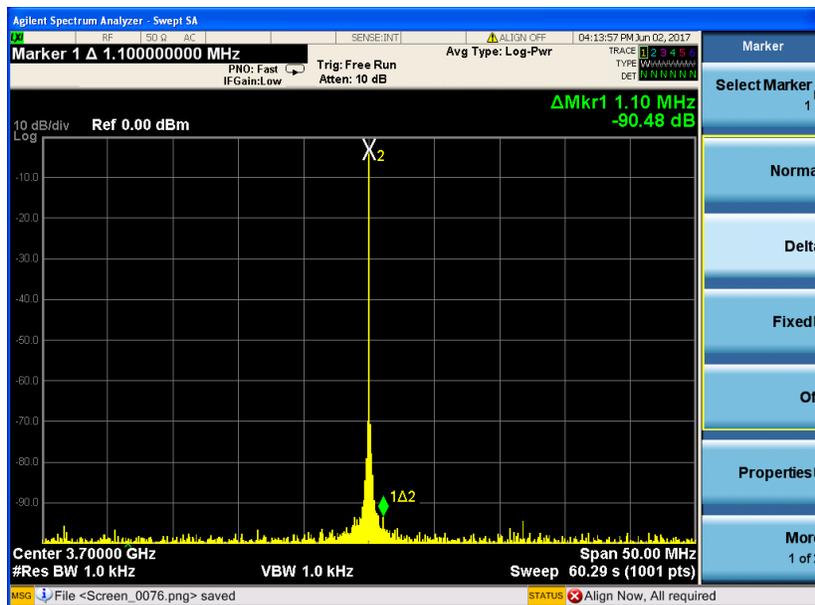
This section describes an alternative way to route the DC-DC converter signals for further improvement of in-band spurious emissions.

Spurious Performance – Modified PCB

Test conditions unless otherwise noted: $V_{CC} = +5.0\text{ V}$, $T/R = +3.0\text{ V}$, $R_{Fin} = -35\text{ dBm CW}$; $Temp. = +25\text{ }^\circ\text{C}$

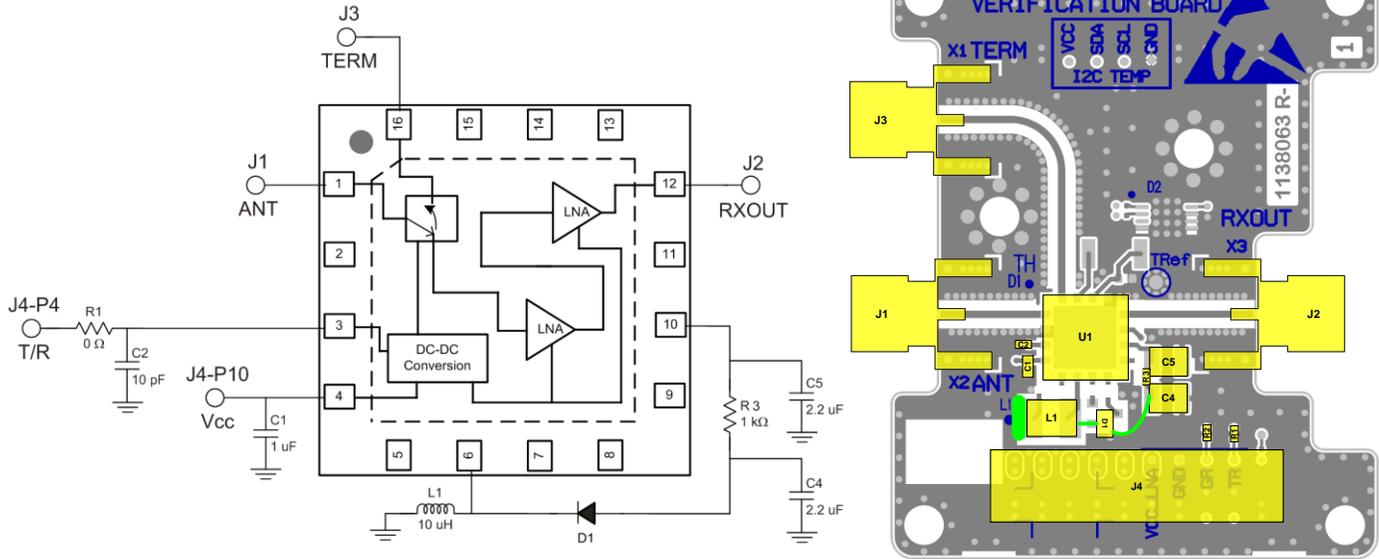


Original PCB Configuration



Modified PCB Configuration

Application Circuit Schematic and Layout – Modified PCB

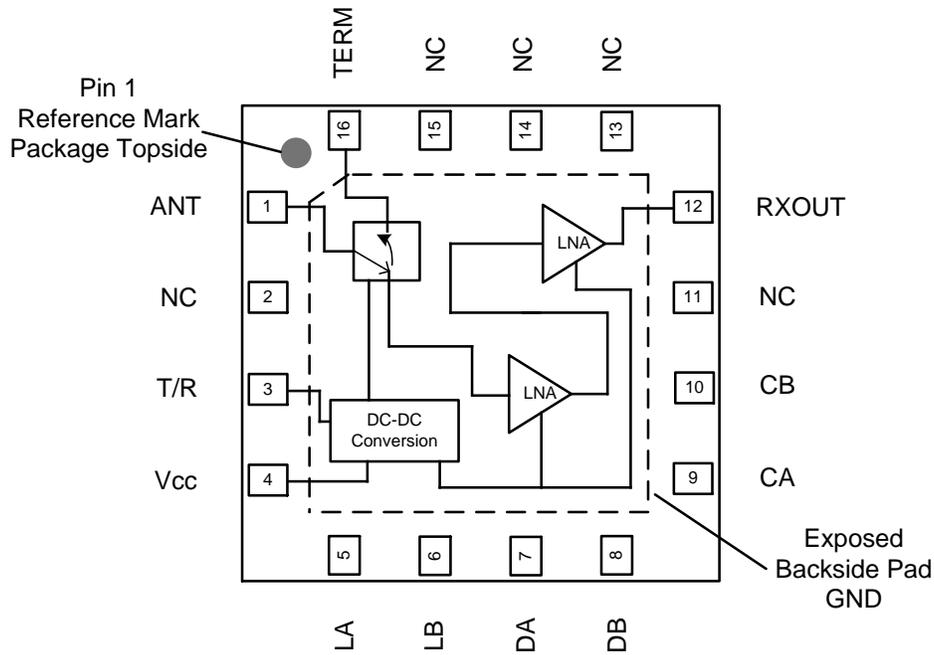


Note:
R3 is the only additional component. All other parts are same as unmodified Evaluation Board

Bill of Material – Modified PCB

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power Switch LNA Module	Qorvo	QPB9325
R1, R2	0 Ω	Resistor, Chip, 0402, 5%	Various	
C1	1 uF	Capacitor, Chip, 0603, 20%, X7R	Various	
C2	10 pF	Capacitor, Chip, 0402, NPO/COG, 5%	Various	
C4, C5	2.2 uF	Capacitor, Chip, 1210, 100 V, 10%, X7R	Various	
D1	n/a	Diode 200 V 200 mA SOT23	Various	
L1	10 uH	Inductor, Power, 10 uH, 20%, 0.84 A	Coilcraft	LPS4018-103ML
R3	1 kΩ	Resistor, Chip, 0402, 5%	Various	

Pin Configuration and Description

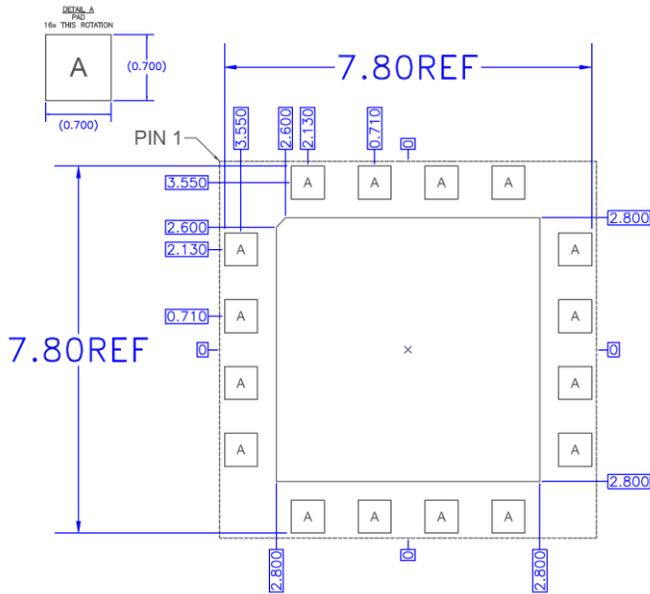
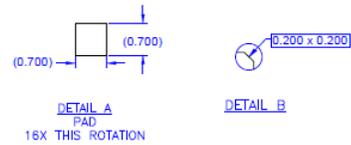
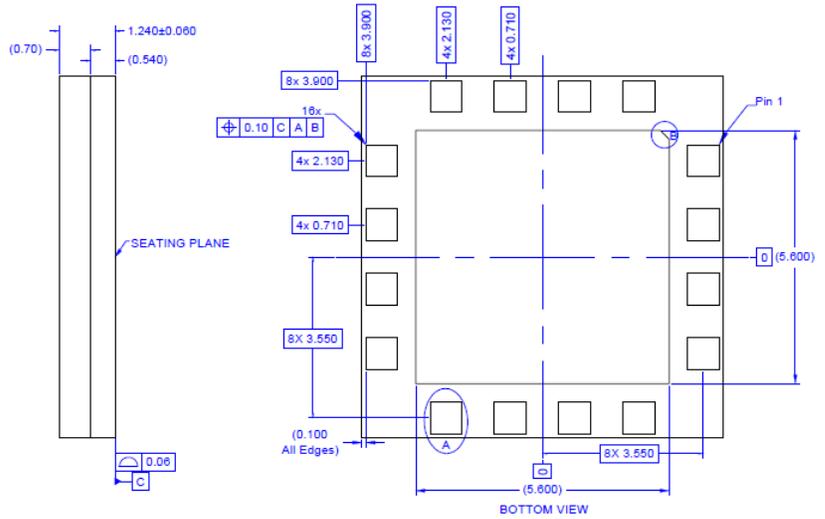
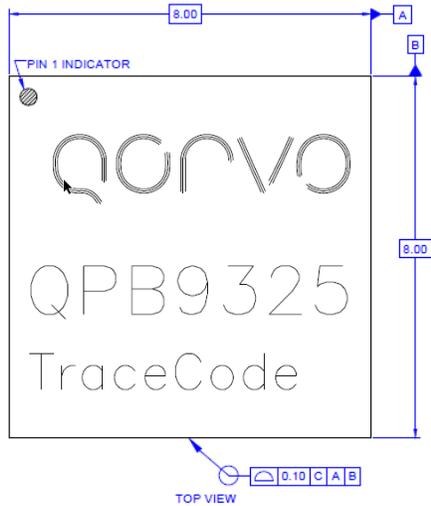


Top View

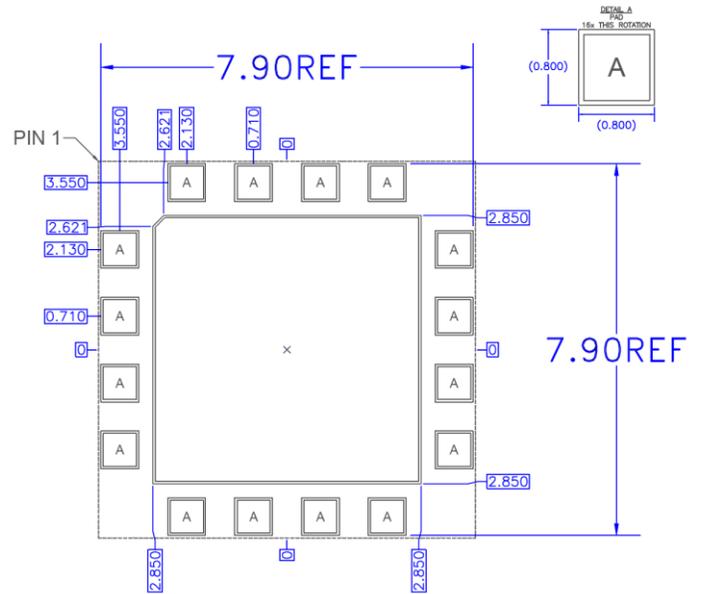
Pin No.	Label	Description
1	ANT	RF antenna input/output port 50 ohms. Internally DC blocked.
2, 11, 13, 14, 15	NC	No Internal Connection.
3	T/R	Switch Control, Tx mode Low state, Rx mode High state.
4	V _{cc}	DC Power Supply Voltage.
5	LA	External inductor connection for internal power supply.
6	LB	External inductor connection for internal power supply.
7	DA	External diode anode connection for internal power supply.
8	DB	External diode cathode connection for internal power supply.
9	CA	External bypass capacitor connection.
10	CB	External bypass capacitor connection.
12	Rx OUT	RF LNA output port 50 ohms. Internally DC blocked.
16	TERM	RF termination port 50 ohms. Internally DC blocked.
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB vias under the device are required.

Package Marking and Dimensions

Marking: Part number – QPB9325
Trace Code



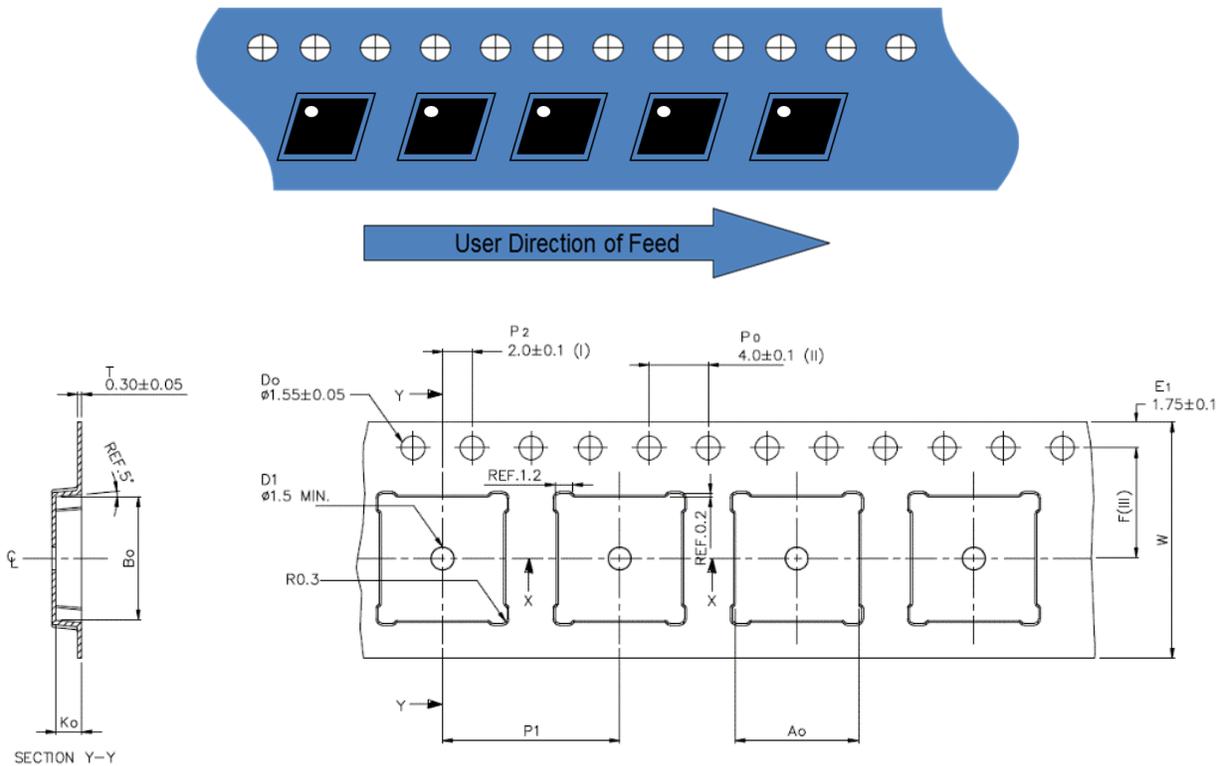
**RECOMMENDED
LAND PATTERN**



**RECOMMENDED
LAND PATTERN MASK**

- Notes:
1. All dimensions are in microns. Angles are in degrees.
 2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
 3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

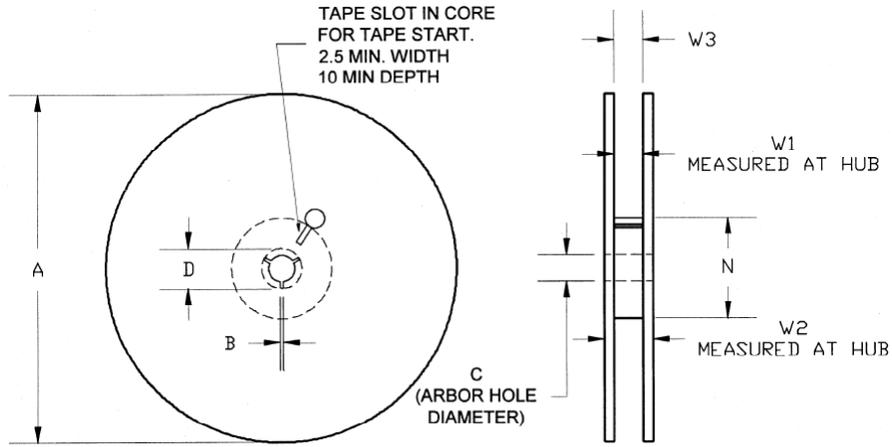
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.329	8.35
	Width	B0	0.329	8.35
	Depth	K0	0.069	1.76
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.0

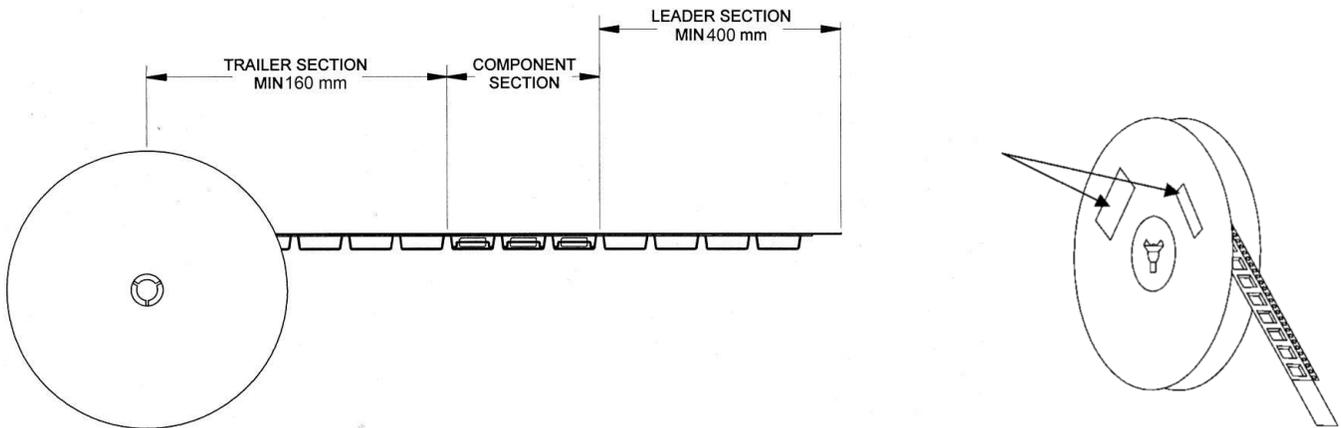
Tape and Reel Information – Reel Dimensions (13")

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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