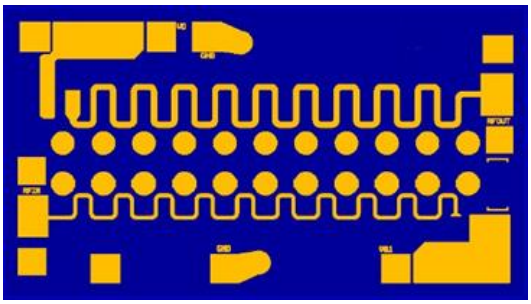
TGA4840

28 Gb/s Linear Driver



Product Description

The TriQuint TGA4840 is an optical modulator linear driver amplifier designed for the CFPx 100 Gb/s optical markets. The TGA4840 has 12 dB of gain and 1.6 Vpp output power and High BW of 50 GHz.

The TGA4840 provides Client side designers with system critical features such as: low power dissipation, high signal to noise ratio (SNR), fast rise and fall times, low output jitter.

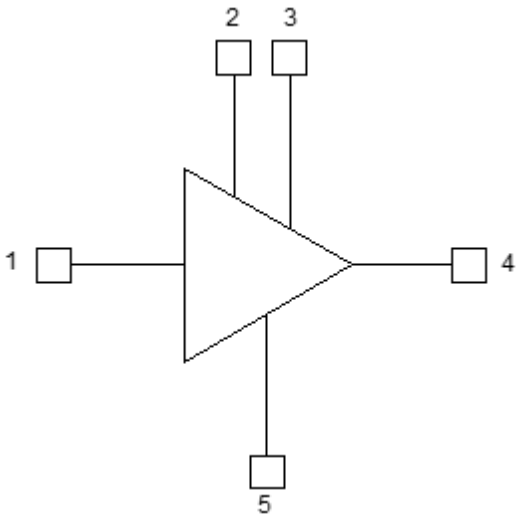
The TGA4840 finish is lead-free. This part is RoHS compliant.

Evaluation modules are available upon request.

Product Features

- 100G Low Power Driver
- Adjustable Output Amplitude, 1 to 3 Vpp
- Low Additive RMS Jitter, 500 fsec
- Gain, 12 dB at 15 GHz
- 3 dB Bandwidth, 50 GHz
- Low THD
- Low DC Power Dissipation, 165 mW @ 1.6 Vpp at Vd = 3.3 V
- Rise and Fall Times, 11 psec
- Die Size: 1.8 x 1.0 x 0.1 mm

Functional Block Diagram



Applications

- Test equipment.
- 28 Gb/s CFP/CFP2/CFP4 Linear Driver
- EML Driver

Ordering Information

Part No.	ECCN	Description
TGA4840	3A001.b.2.f	28 Gb/s Linear Driver

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage, Vd	6.5 V
Drain Voltage Termination, VdT	(VdT - IdT*50) <= 6.5 V
Gate Voltage, Vg	-5 to 0 V
Control Voltage, Vc	MAX [(Vd-7), -1.3 V] to +3.9 V
Drain to Gate Voltage	10 V
Drain Current, Id	213 mA
Drain Current Termination, IdT	72 mA
Ig	-15 to + 16 mA
RF CW Input Power	5 Vpp (18 dBm)
Channel Temperature, Tch	200 °C
Mounting Temperature (30 sec)	320 °C
Storage Temperature	-65 to 150 °C

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.
2. If VdT pin is being used:
   assure (VdT - IdT*50) – Vc >= -0.5 V.
3. If RFout / Vd pin is being used:
   assure Vd - Vc >= -0.5 V.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Temperature	-40		125	°C
Vd		3.3		V
Id		50		mA
Id(Under RF Drive, Constant Vg)		52		mA
Vg		-0.5		V
Vc		0.0		V
Ig		<1		mA
Ic		<2		mA

Note:

1. Recommended operating conditions are measured at specified test conditions of Vout = 1.6 Vpp when Vin = 0.5 Vpp, 28 Gb/s.

Electrical Specifications

Test conditions unless otherwise noted: 25 ˚C, Vd = 3.3 V, Vc = 0.0 V, Id = 50 mA, Vg ~ -0.5 V typical.

Parameter	Min	Typ	Max	Units
Operational Data rate		28		Gb/s
Small Signal Gain (S21) 0.01 – 20 GHz 20.1 – 35 GHz 35.1 – 45 GHz 45.1 – 50 GHz	 11 10 8 6	 12 12 11 10		dB
Input Return Loss (S11) 0.01 – 20 GHz 20.1 – 50 GHz		 -15 -10	 -11 -8	dB
Output Return Loss (S22) 0.01 – 10 GHz 10.1 – 35 GHz 35.1 – 50 GHz		 -23 -15 -8	 -20 -10 -6	dB
3 dB Bandwidth		50		GHz
Noise Figure 1 – 7 GHz 7.1 – 35 GHz		 5 3.5	 6 4	dB
Output Amplitude (Vin = 0.5 Vpp, 28 Gb/s)		1.6		Vpp
Crossing %		50		-
Additive RMS Jitter (See note 1)		500		fs
PP Jitter		2.7		ps
Risetime (20% - 80%)		10		ps
Falltime (80% - 20%)		11		ps
Output Voltage, Vpp, change with temp using Vc feedback loop (see note 2)		-0.002		Vpp / ºC
Output Voltage, Vpp, change with temp without Vc feedback loop (see note 2)		-0.01		Vpp / ºC

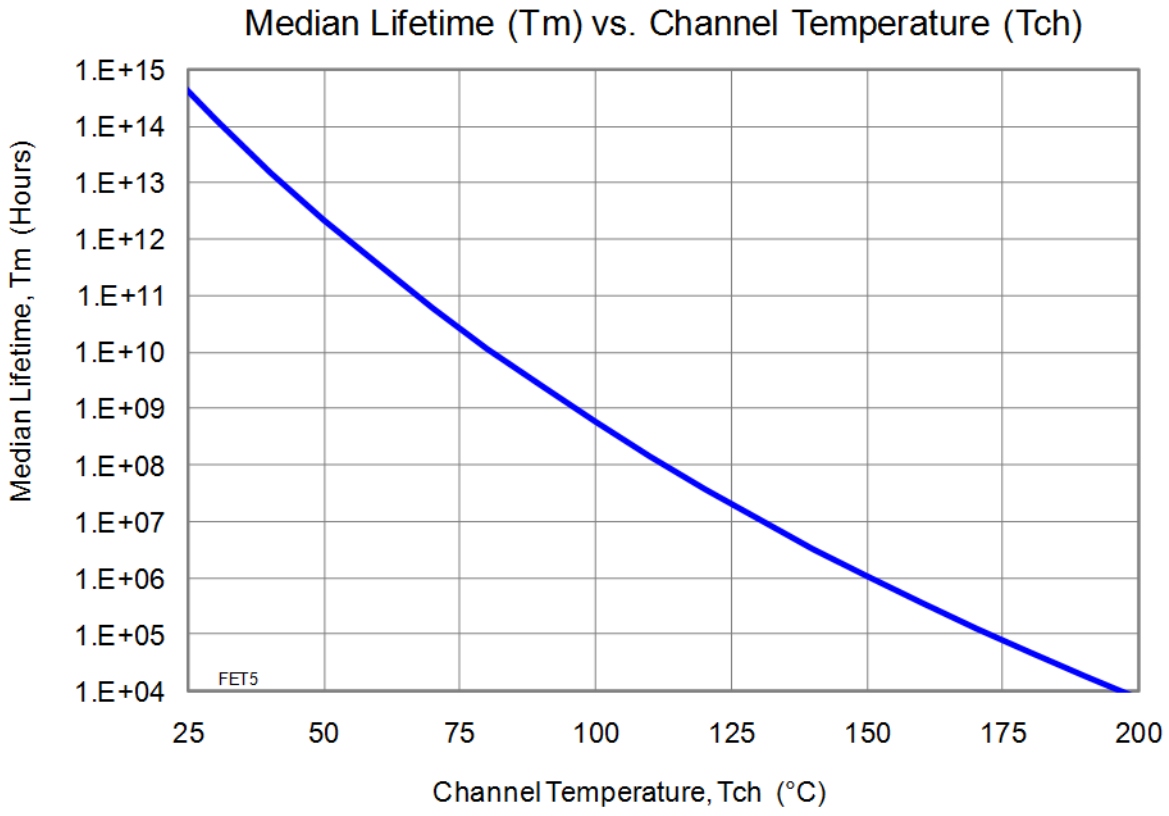
Notes:
1. Additive RMS Jitter defined as: Sqrt [(Total RMS Jitter)^2 – (Input RMS Jitter)^2]
2. Application note “Robust Bias Option for Optical Modulator Drivers” available upon request.

Thermal and Reliability Information

Parameter	Test Conditions	Value
Thermal Resistance, θ_{JC}, measured to back of package	Tbase = 70 °C	θ_{JC} = 43.1 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	Tbase = 70 °C Vd = 3.3 V, Id = 50 mA Pdiss = 0.165 W	Tch = 77 °C Tm = 1.9E+10 Hours
Channel Temperature (Tch), and Median Lifetime (Tm) Under RF Drive	Tbase = 70 °C Vd = 3.3 V, Id = 52 mA Vout = 1.6 Vpp Pdiss = 0.166 W	Tch = 77 °C Tm = 1.9E+10 Hours

Notes
1. Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.
2. θjc is the thermal resistance of the die mounted to a 0.020" thick Cu-Mo block using 0.8 mil conductive epoxy.

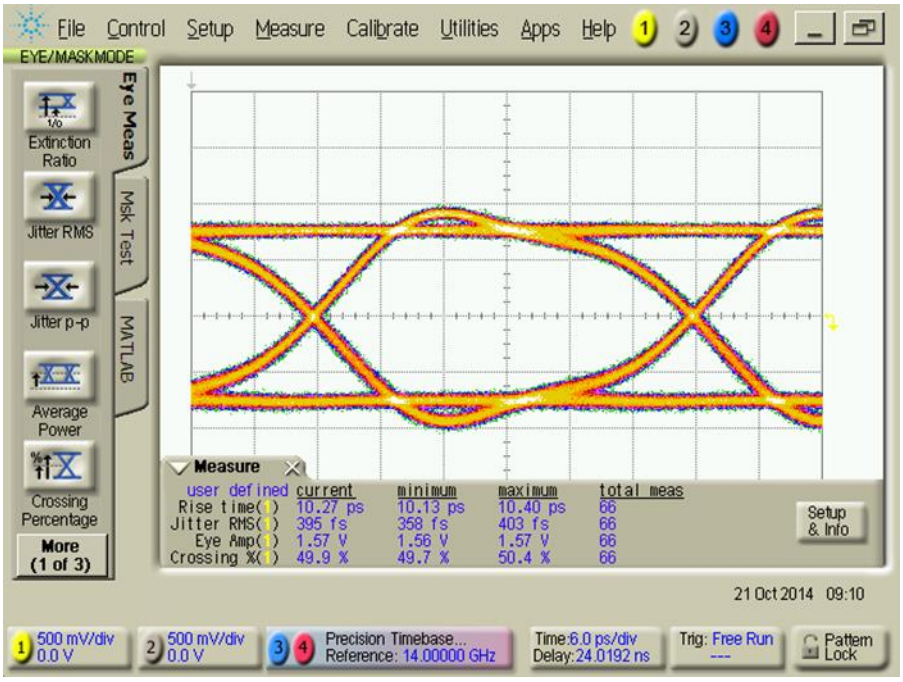
Median Lifetime



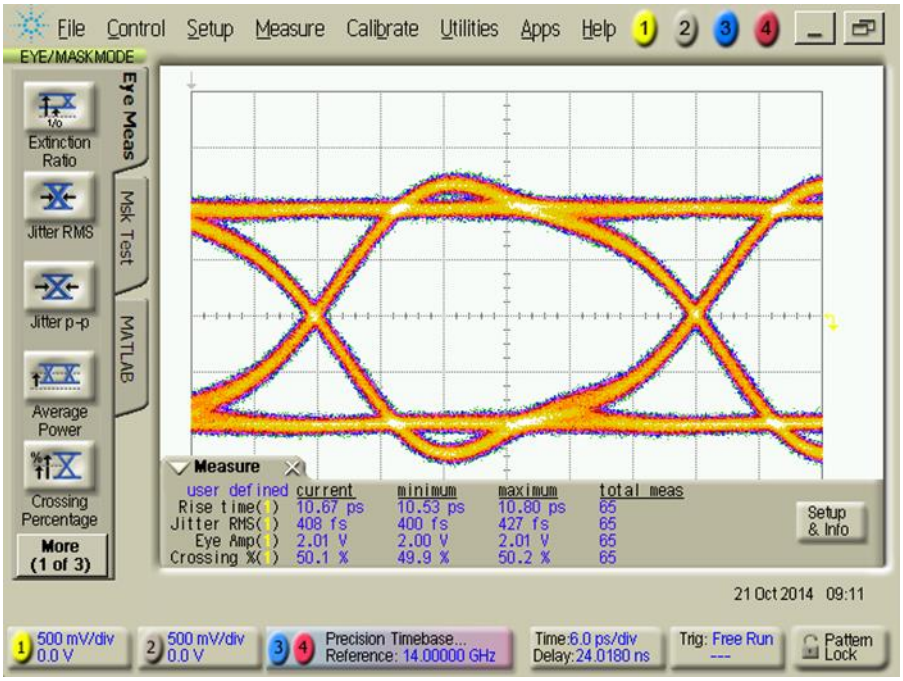
Typical Performance Electrical Eye Diagram

Vin = 0.5 Vpp, 28 Gb/s, PRBS signal 2^{31} -1, Vg adjusted to attain desired Vout., T = 25 °C

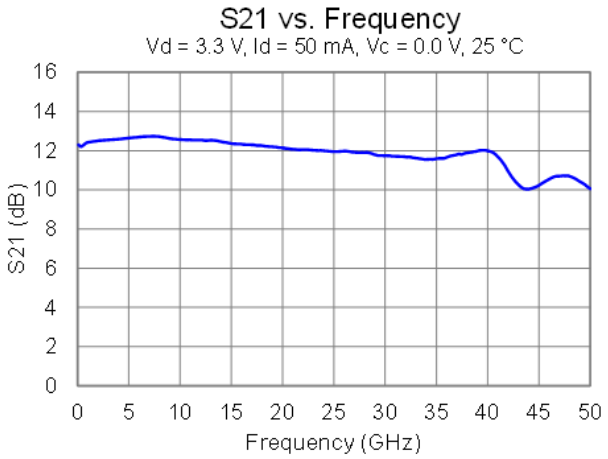
Vd = 3.3 V, Vc = 0.0 V, Id = 52 mA

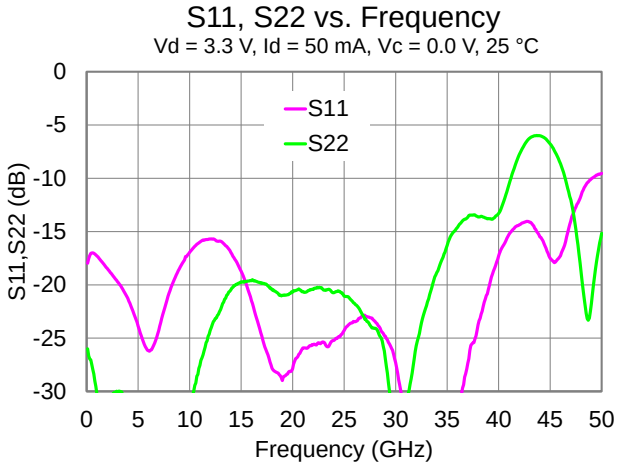


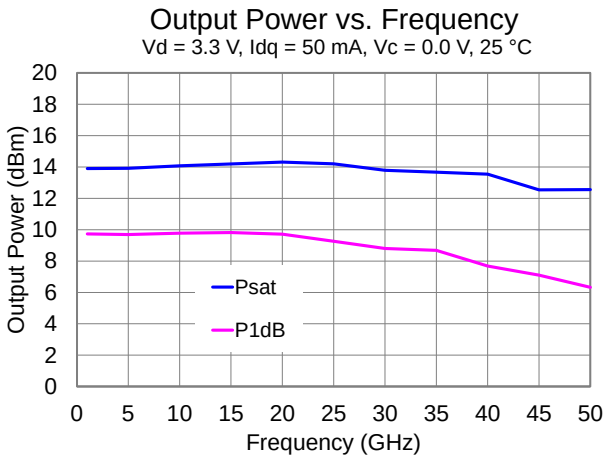
Vd = 3.3 V, Vc = 0.5 V, Id = 78 mA

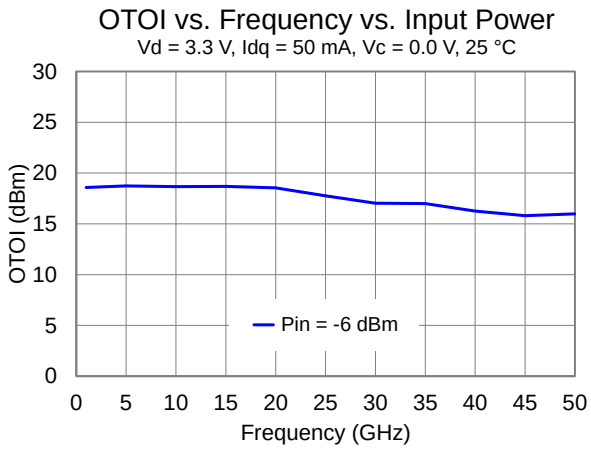


Typical Performance



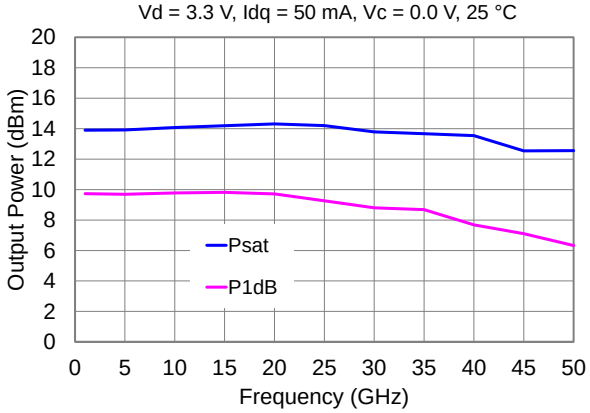




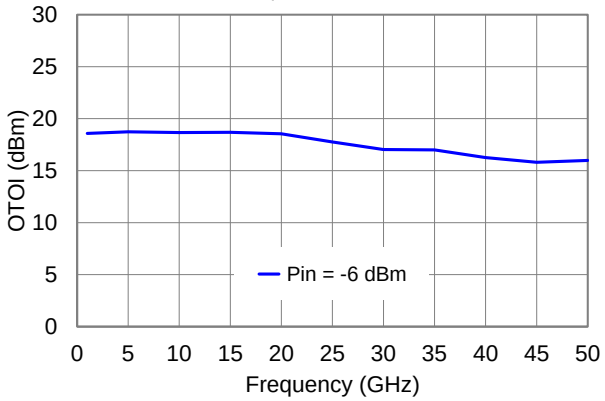


Typical Performance

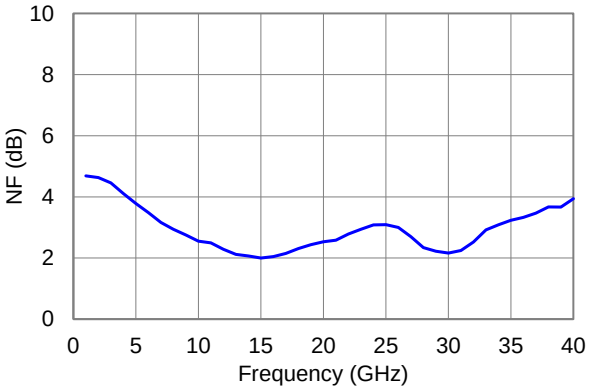
Output Power vs. Frequency
Vd = 3.3 V, Idq = 50 mA, Vc = 0.0 V, 25 °C



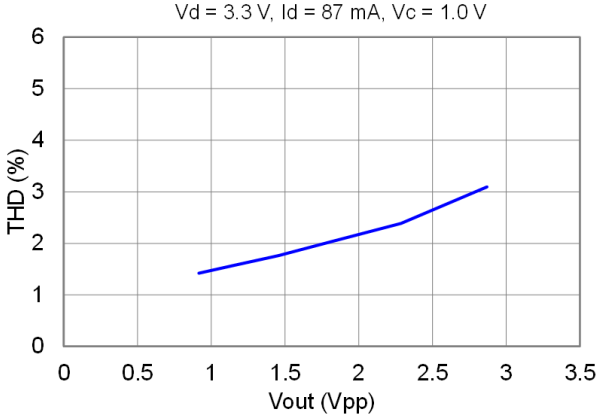
OTOI vs. Frequency vs. Input Power
Vd = 3.3 V, Idq = 50 mA, Vc = 0.0 V, 25 °C



Noise Figure vs. Frequency
Vd = 3.3 V, Id = 50 mA, Vc = 0.0 V, 25 °C

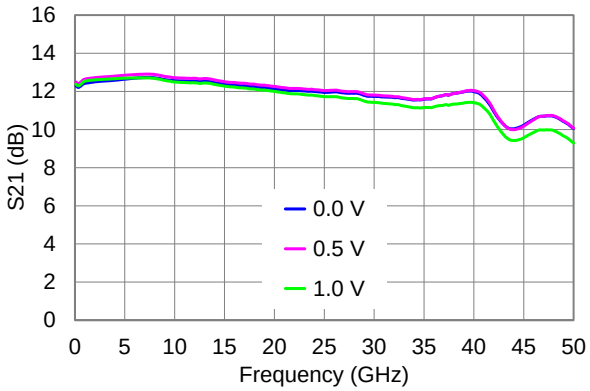


THD vs. Vout @ 1 GHz
Vd = 3.3 V, Id = 87 mA, Vc = 1.0 V

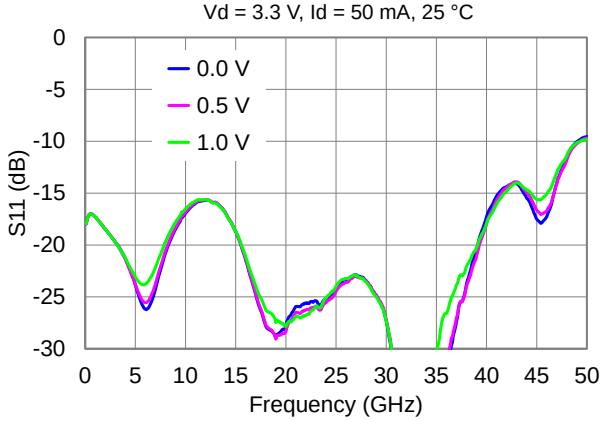


Typical Performance

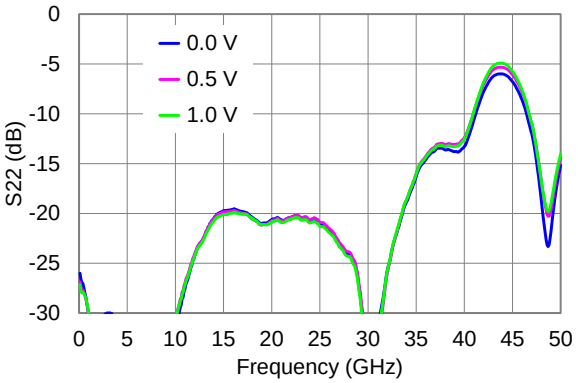
S21 vs. Frequency vs. Control Voltages
Vd = 3.3 V, Id = 50 mA, 25 °C



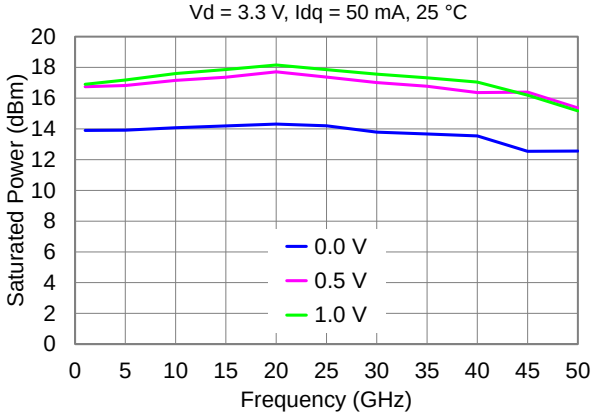
S11 vs. Frequency vs. Control Voltages
Vd = 3.3 V, Id = 50 mA, 25 °C



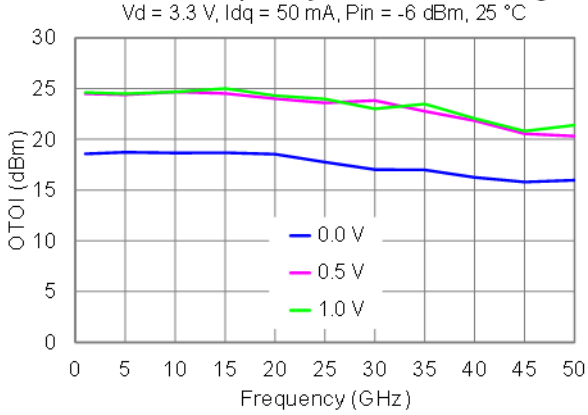
S22 vs. Frequency vs. Control Voltages
Vd = 3.3 V, Id = 50 mA, 25 °C



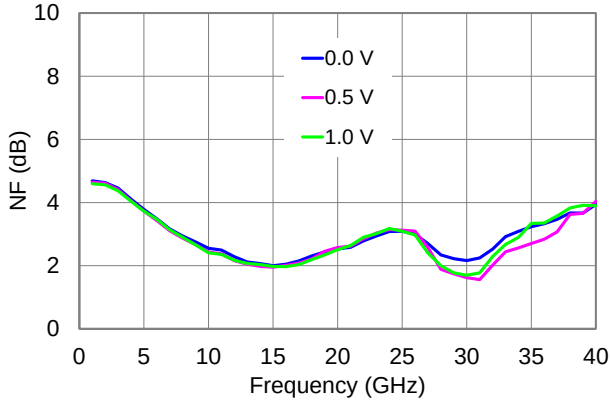
Power vs. Frequency vs. Control Voltages
Vd = 3.3 V, Idq = 50 mA, 25 °C



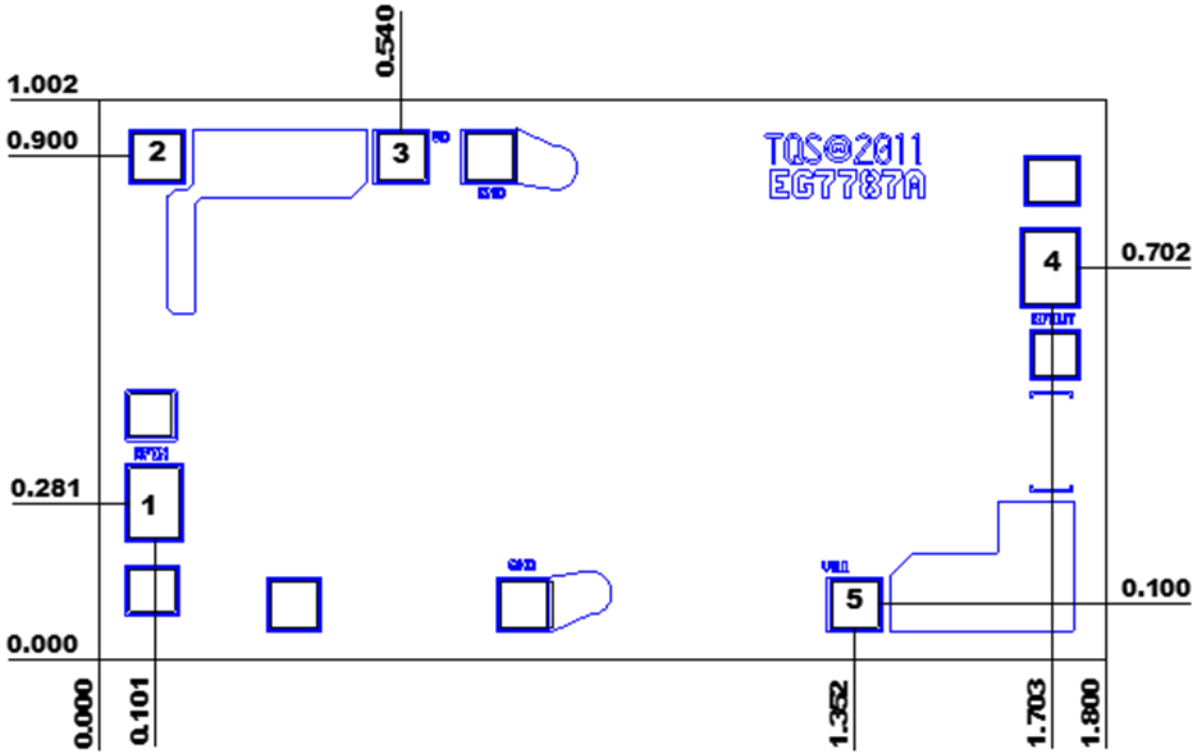
OTOI vs. Frequency vs. Control Voltages
Vd = 3.3 V, Idq = 50 mA, Pin = -6 dBm, 25 °C



NF vs. Frequency vs. Control Voltages
Vd = 3.3 V, Id = 50 mA, 25 °C



Pin Configuration



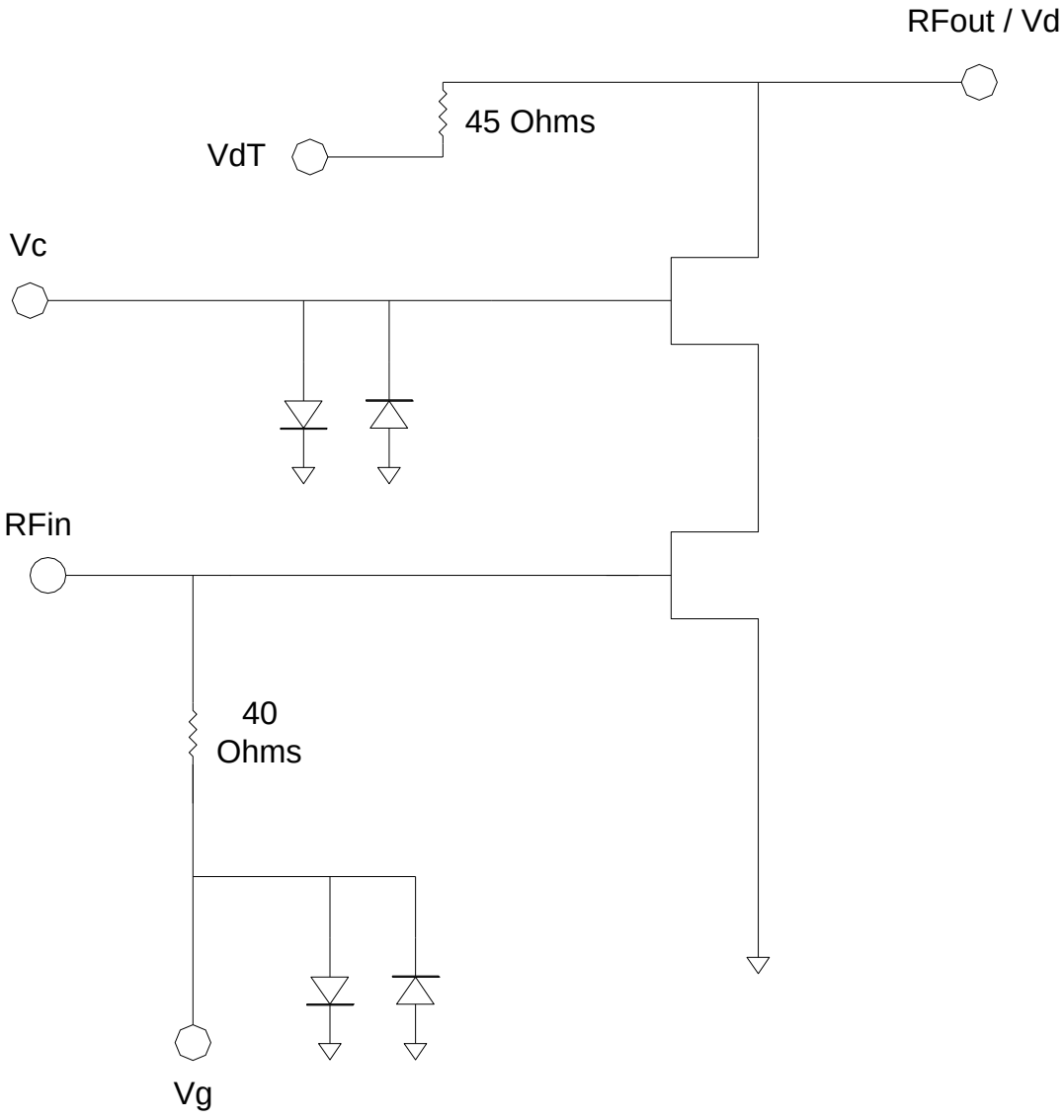
Units: millimeters
Chip edge to bond pad dimensions are shown to center of pad
Chip size tolerance: ± 0.051
Thickness: 0.100 (reference only)

Pin Description

Pin No.	Label	Description	Pad Size
1	RFin	RF Input	0.086 x 0.125
2	Vctrl	Control voltage pin	0.082 x 0.082
3	VdT	Vd pin for biasing through the termination resistor	0.082 x 0.082
4	RFout / Vd (RFout)	RF Output and/or Vd bias pin (avoids voltage drop across termination resistor)	0.092 x 0.128
5	Vg	Gate voltage pin	0.082 x 0.082

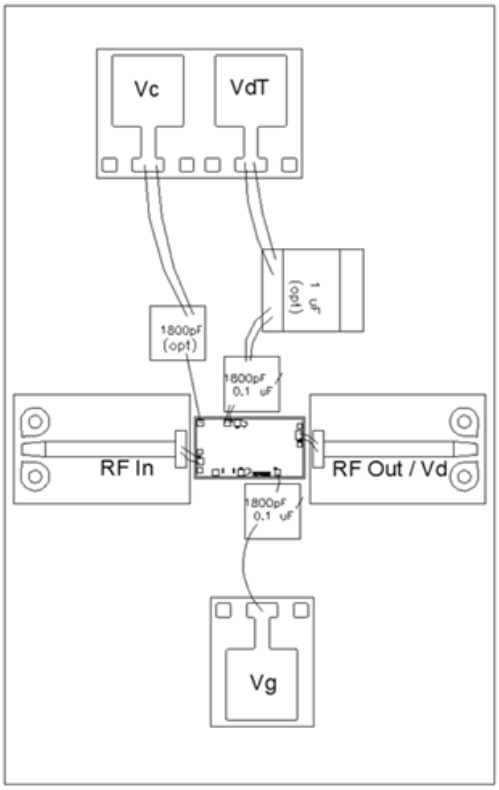
Circuit Description

DC Schematic



Application Circuit

Recommended Chip Assembly Diagram



Note: Input and Output ports are DC coupled.
If biasing Vd through the RFOut side, a bias tee is required.

Evaluation Board Bias Procedures

Laboratory Bias-up Procedure: see Note 1	Laboratory Bias-down Procedure
Set Vg to -1.5 V	Turn off RF supply. See note 2
Set Vd to 3.3 V or VdT to 5 V	Vg set to -1.5 V
Vc set to desired value	Vc set to 0 V
Adjust Vg more positive until target Id is reached.	Turn Vd to 0 V
Adjust Vc for desired Vout signal	Turn Vg to 0 V
Adjust Vg for 50% crossing	
Re-adjust Vc and Vg, if necessary	
Apply RF signal to RF Input. See note 2	

Notes:

1. Any bias procedure will not harm the device as long as the guidelines explicitly stated in the Max Ratings Table and corresponding notes section on page 2 of the Datasheet are followed. For laboratory evaluation, the following is provided as a bias procedure that will allow user to observe and set each stage's quiescent point individually.
2. RF supply can be on during power up and power down sequences.

Assembly Notes

Reflow Attachment:

- Use solder with limited exposure to temperatures at or above 300°C
- Use alloy station or conveyor furnace with reducing atmosphere
- No fluxes should be utilized
- Coefficient of thermal expansion matching is critical for long-term reliability
- Storage in dry nitrogen atmosphere

Adhesive Attachment:

- Organic attachment can be used in low-power applications
- Curing should be done in a convection oven; proper exhaust is a safety concern
- Microwave or radiant curing should not be used because of differential heating
- Coefficient of thermal expansion matching is critical

Component Pickup and Placement:

- Vacuum pencil and/or vacuum collet preferred method of pick up
- Avoidance of air bridges during placement
- Force impact critical during auto placement

Interconnect:

- Thermosonic ball bonding is the preferred interconnect technique
- Force, time, and ultrasonics are critical parameters
- Aluminum wire should not be used
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- Maximum stage temperature: 200°C

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	JEDEC Standard JESD22 A114

Caution!
ESD-Sensitive Device

Solderability

Compatible with AuSn solder

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.qorvo.com **Tel:** +1.972.994.8465
Email: info-sales@qorvo.com **Fax:** +1.972.994.8504

For technical questions and application information:

Email: info-products@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.**

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.