63 MHz Dual Programmable Filters and Variable Gain Amplifiers

ANALOG DEVICES

Preliminary Technical Data

ADRF6518

FEATURES

Matched pair of programmable filters and triple VGAs
Continuous gain control range: 72 dB
Digital gain control: 30 dB
6-pole Butterworth filter: 1 MHz to 63 MHz
in 1 MHz steps, 1 dB corner frequency
Preamplifier and postamplifier gain steps
Peak detector
Filter bypass mode, −3 dB bandwidth (BW)
VGA2 and VGA3 21 dB/12 dB gain: 350 MHz/700 MHz
IMD3: >65 dBc for 1.5 V p-p composite output
HD2, HD3: >65 dBc for 1.5 V p-p output
Differential input and output
Flexible output and input common-mode ranges
Optional dc output offset correction
SPI programmable filter corners and gain steps
Single 3.3 V supply operation with power-down feature

APPLICATIONS

Baseband I/Q receivers
Diversity receivers
ADC drivers
Point-to-point and point-to-multipoint radios
Instrumentation
Medical

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

GENERAL DESCRIPTION

The ADRF6518 is a matched pair of fully differential low noise and low distortion programmable filters and variable gain amplifiers (VGAs). Each channel is capable of rejecting large out-of-band interferers while reliably boosting the wanted signal, thus reducing the bandwidth and resolution requirements on the analog-to-digital converters (ADCs). The excellent matching between channels and their high spurious-free dynamic range over all gain and bandwidth settings make the ADRF6518 ideal for quadrature-based (IQ) communication systems with dense constellations, multiple carriers, and nearby interferers. The various amplifier gains, filter corners and other features are all programmable via a serial port interface (SPI) port.

The first VGA that precedes the filters offers 24 dB of continuous gain control with fixed gain options of 9 dB, 12 dB, and 15 dB, and sets a differential input impedance of 400 Ω. The filters provide a six-pole Butterworth response with 1 dB corner frequencies from 1 MHz to 63 MHz in 1 MHz steps. For operation beyond 63 MHz, the filter can be disabled and completely bypassed via the SPI. A wideband peak detector is available to monitor the
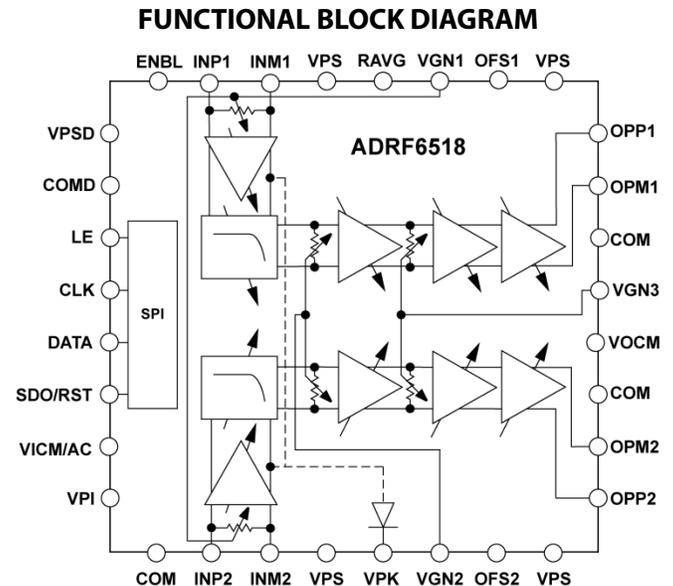
peak signal at the filter inputs. The pair of VGAs that follow the filters each provides 24 dB of continuous gain control with fixed gain options of 12 dB, 15 dB, 18 dB, and 21 dB. The output buffers offer an additional option of 3 dB or 9 dB gain and provide a differential output impedance of less than 10 Ω. They are capable of driving 3 V p-p into 1 kΩ loads at better than 65 dBc HD3. The output common-mode voltage defaults to VPS/2 and can be adjusted down to 900 mV by driving the high impedance VOCM pin. Independent, built-in dc offset correction loops for each channel can be disabled via the SPI if fully dc-coupled operation is desired. The high-pass corner frequency is deter-mined by external capacitors on the OFS1 and OFS2 pins and the postfilter VGA gain.

The ADRF6518 operates from a 3.15 V to 3.45 V supply and consumes a maximum supply current of 400 mA. When fully disabled, it consumes <10 mA. The ADRF6518 is fabricated in an advanced silicon-germanium BiCMOS process and is available in a 32-lead, exposed pad LFCSP. Performance is specified over the −40°C to +85°C temperature range.

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SPECIFICATIONS

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 1 kΩ, unless otherwise noted, VGA1 maximum gain code = 00, VGA2 maximum gain code = 00, VG3 maximum gain code = 00, postamp gain code = 1, offset compensation loop enabled, low/high power mode.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RESPONSE, FILTER BYPASS MODE					
−3 dB Bandwidth	VGA2 and VGA3 21 dB digital gain setting		350		MHz
	VGA2 and VGA3 12 dB digital gain setting		700		MHz
FREQUENCY RESPONSE					
Low-Pass Corner Frequency, f_C	6-pole Butterworth filter, 0.5 dB bandwidth	1		63	MHz
Step Size			1		MHz
Corner Frequency Absolute Accuracy	Over operating temperature range		±8		% f_C
Corner Frequency Matching	Channel A and Channel B at same gain and bandwidth settings		±0.5		% f_C
Pass-Band Ripple			0.5		dB p-p
Gain Matching	Channel A and Channel B at same gain and bandwidth settings		±0.1		dB
Group Delay Variation	From midband to peak				
Corner Frequency = 1 MHz			135		ns
Corner Frequency = 30 MHz			11		ns
Group Delay Matching	Channel A and Channel B at same gain				
Corner Frequency = 1 MHz			5		ns
Corner Frequency = 30 MHz			0.2		ns
Stop-Band Rejection					
Relative to Pass Band	2 × f_C		30		dB
	5 × f_C		75		dB
INPUT STAGE	INP1, INM1, INP2, INM2, VICM				
Maximum Input Swing	At minimum gain, VGN1 = 0 V		4.0		V p-p
Differential Input Impedance			400		Ω
Input Common-Mode Range	1.5 V p-p input voltage, HD3 > 65 dBc (VPI = 3.3 V)	1.35		1.95	V
	Input pins left floating		1.5		V
PEAK DETECTOR	VPK, RAVG				
Output scaling	Relative to peak voltage at filter input		1		V/V pk
GAIN CONTROL	VGN1, VGN2, VGN3				
Gain Range	Maximum digital gains	−6		+66	dB
	Minimum digital gains	−36		+36	dB
Voltage Attenuation Range	Each attenuator; V_{GAIN} from 0 V to 1 V	−24		0	dB
Gain Slope			30		mV/dB
Gain Error	V_{GAIN} from 300 mV to 800 mV		0.2		dB
OUTPUT STAGE	OPP1, OPM1, OPP2, OPM2, VOCM				
Maximum Output Swing	At maximum gain, R_{LOAD} = 1 kΩ		3		V p-p
	HD2 > 65 dBc, HD3 > 65 dBc		1.5		V p-p
Differential Output Impedance			<10		Ω
Output DC Offset	Inputs shorted, offset loop enabled		<20		mV
Output Common-Mode Range	1.5 V p-p output voltage	0.9		VPS − 1.2	V
	VOCM left floating		VPS/2		V
VOCM Input Impedance			23		kΩ

| Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE/DISTORTION					
Corner Frequency = 31 MHz					
Output Noise Density	Maximum gain at $f_C/2$		−105.5		dBV/Hz
	Minimum gain at $f_C/2$		−105.5		dBV/Hz
Second Harmonic, HD2	10 MHz fundamental, 1.5 V p-p at VGA1 output voltage				
	VGA2, VGA3 at minimum gain (digital and analog)		66		dBc
Third Harmonic, HD3	10 MHz fundamental, 1.5 V p-p at VGA1 output voltage				
	VGA2, VGA3 at minimum gain (digital and analog)		66		dBc
IMD3	f1 = 500 kHz, f2 = 550 kHz, 1.5 V p-p composite output voltage		65		dBc
Corner Frequency = 63 MHz					
Output Noise Density	Minimum gain		−105.5		dBV/Hz
	Maximum gain		−105.5		dBV/Hz
Second Harmonic, HD2	20 MHz fundamental, 1.5 V p-p at VGA1 output voltage				
	VGA2, VGA3 at minimum gain (digital and analog)		56		dBc
Third Harmonic, HD3	20 MHz fundamental, 1.5 V p-p at VGA1 output voltage				
	VGA2, VGA3 at minimum gain (digital and analog)		66		dBc
DIGITAL LOGIC	LE, CLK, DATA, SDO				
Input High Voltage, V_{INH}			>2		V
Input Low Voltage, V_{INL}			<0.8		V
Input Current, I_{INH}/I_{INL}			<1		µA
Input Capacitance, C_{IN}			2		pF
SPI TIMING	LE, CLK, DATA, SDO				
f_{SCLK}	$1/t_{SCLK}$		20		MHz
t_{DH}	DATA hold time		5		ns
t_{DS}	DATA setup time		5		ns
t_{LH}	LE hold time		5		ns
t_{LS}	LE setup time		5		ns
t_{PW}	CLK high pulse width		5		ns
t_D	CLK to SDO delay		5		ns
POWER AND ENABLE	VPS, VPSD, COM, COMD, ENBL				
Supply Voltage Range		3.15	3.3	3.45	V
Total Supply Current	ENBL = 5 V				
	Maximum BW setting, high power filter		400		mA
	Minimum BW setting, low power filter		360		mA
	Filter Bypassed, high power mode		260		mA
	Filter Bypassed, low power mode		230		mA
Disable Current	ENBL = 0 V		9		mA
Disable Threshold			1.6		V
Enable Response Time	Delay following ENBL low-to-high transition		20		µs
Disable Response Time	Delay following ENBL high-to-low transition		300		ns

TIMING DIAGRAMS
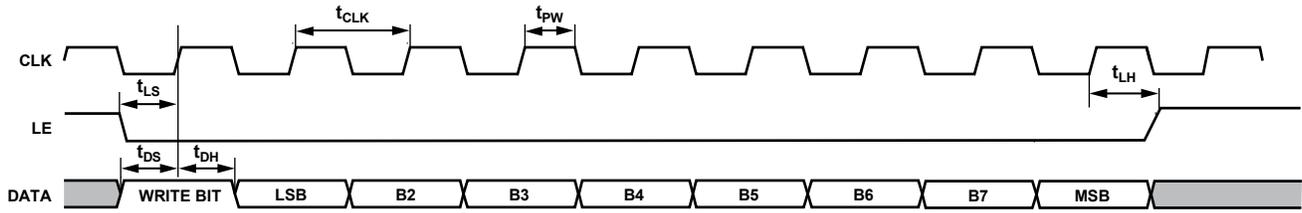
NOTES
1. THE FIRST DATA BIT DETERMINES WHETHER THE PART IS WRITING TO OR READING FROM THE INTERNAL 8-BIT REGISTER. FOR A WRITE
OPERATION, THE FIRST BIT SHOULD BE A LOGIC 1. THE 8-BIT WORD IS THEN WRITTEN TO THE DATA PIN ON CONSECUTIVE RISING
EDGES OF THE CLOCK.

Figure 2. Write Mode Timing Diagram
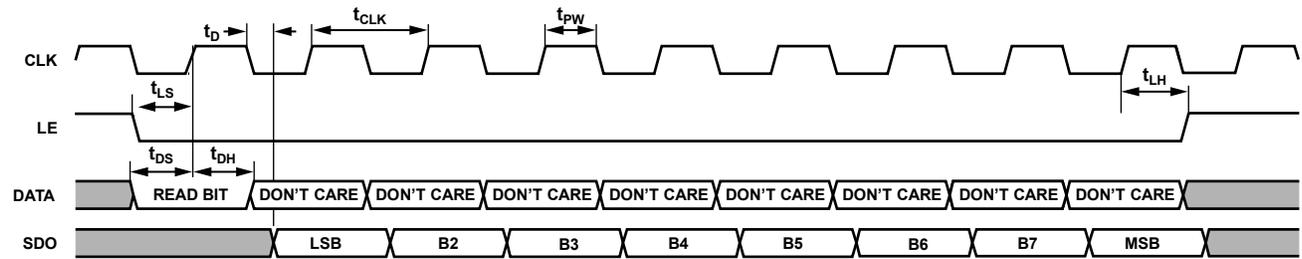
NOTES
1. THE FIRST DATA BIT DETERMINES WHETHER THE PART IS WRITING TO OR READING FROM THE INTERNAL 8-BIT REGISTER. FOR A READ
OPERATION, THE FIRST BIT SHOULD BE A LOGIC 0. THE 8-BIT WORD IS THEN REGISTERED AT THE SDO PIN ON CONSECUTIVE FALLING EDGES
OF THE CLOCK.

Figure 3. Read Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages, VPS, VPSD	3.45 V
ENBL, LE, CLK, DATA, SDO	VPSD + 0.5 V
INP1, INM1, INP2, INM2, VICM	VPS + 0.5 V
OPP1, OPM1, OPP2, OPM2, VOCM	VPS + 0.5 V
OFS1, OFS2, VPK, RAVG	VPS + 0.5 V
VGN1, VGN2, VGN3	VPS + 0.5 V
Internal Power Dissipation	1.25 W
θ$_{JA}$ (Exposed Pad Soldered to Board)	37.4°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS
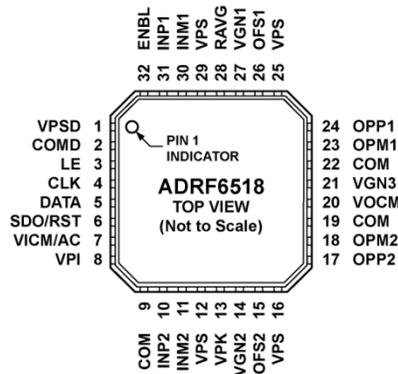
NOTES
1. CONNECT THE EXPOSED PADDLE TO
   A LOW IMPEDANCE GROUND PAD.

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPSD	Digital Positive Supply Voltage: 3.15 V to 3.45 V.
2	COMD	Digital Common. Connect to external circuit common using the lowest possible impedance.
3	LE	Latch Enable. SPI programming pin. TTL levels: $V_{LOW} < 0.8$ V, $V_{HIGH} > 2$ V.
4	CLK	SPI Port Clock. TTL levels: $V_{LOW} < 0.8$ V, $V_{HIGH} > 2$ V.
5	DATA	SPI Data Input. TTL levels: $V_{LOW} < 0.8$ V, $V_{HIGH} > 2$ V.
6	SDO/RST	SPI Data Output (SDO). TTL levels: $V_{LOW} < 0.8$ V, $V_{HIGH} > 2$ V.
		Peak Detector Reset (RST). A >25 ns high pulse is required on this pin to reset the detector.
7	VICM/AC	Input Common-Mode Reference (VICM). VPI/2 reference output for optimal common-mode level to drive the differential inputs.
		AC Coupling/Internal Bias Activation (AC). Pull this pin low for ac coupling of the inputs.
8	VPI	Input Stage Supply Voltage: 3.15 V to 5.25 V. Connect to VPS if input common-mode range is narrow (1.35 V to 1.95 V). Connect to 5 V if input common-mode up to 3.1 V is desired.
12, 16, 25, 29	VPS	Analog Positive Supply Voltage: 3.15 V to 3.45 V.
9, 19, 22	COM	Analog Common. Connect to external circuit common using the lowest possible impedance.
10, 11, 30, 31	INP2, INM2, INM1, INP1	Differential Inputs. 400 Ω input impedance.
13	VPK	Peak Detector Output. Scaling of 1 V/V pk differential at filter inputs. The bigger peak of two channels is reported.
14	VGN2	VGA2 Analog Gain Control. 0 V to 1 V, 30 mV/dB gain scaling.
15, 26	OFS2, OFS1	Offset Correction Loop Compensation Capacitors. Connect capacitors to circuit common.
17, 18, 23, 24	OPP2, OPM2, OPM1, OPP1	Differential Outputs. <10 Ω output impedance. Common-mode range is 0.9 V to VPS − 1.2 V; default is VPS/2.
20	VOCM	Output Common-Mode Setpoint. Defaults to VPS/2 if left open.
21	VGN3	VGA3 Analog Gain Control. 0 V to 1 V, 30 mV/dB gain scaling.
27	VGN1	VGA1 Analog Gain Control. 0 V to 1 V, 30 mV/dB gain scaling.
28	RAVG	Peak Detector Time-Constant Resistor. Connect this pin to VPS. Leave open for longest hold time. RAVG range is ∞ to 1 kΩ.
32	ENBL	Chip Enable. Pull high to enable.
	EP	Exposed Pad. Connect the exposed pad to a low impedance ground pad.

TYPICAL PERFORMANCE CHARACTERISTICS

FILTER MODE

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, low power mode, digital gain code B[8:2] = 1111110, and B1 = 0, unless otherwise noted.
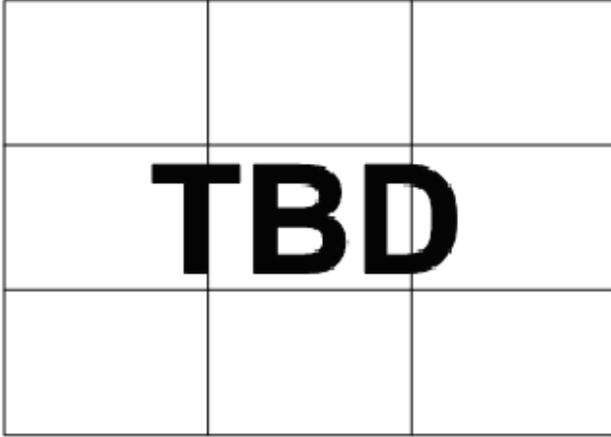

Figure 5. In-Band Gain vs. VGN1 over Supply and Temperature
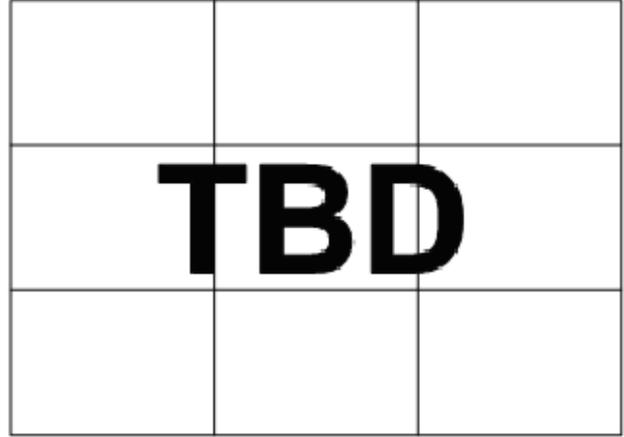*(BW Setting = 63 MHz)*

Figure 8. Gain Conformance vs. VGN1 over Supply and Temperature
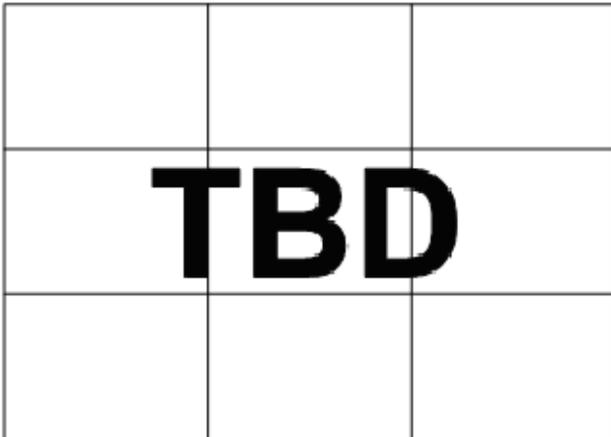*(Bandwidth Setting = 63 MHz)*

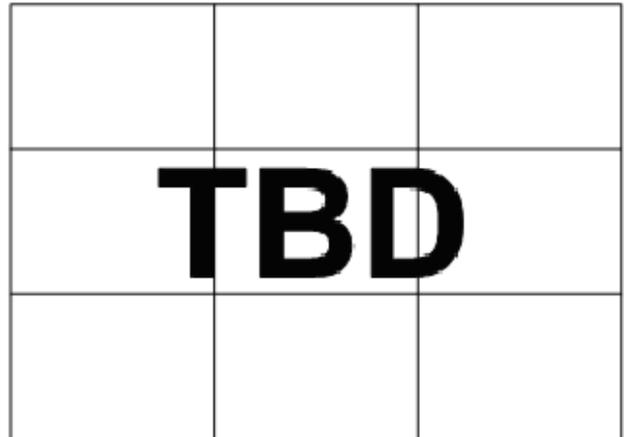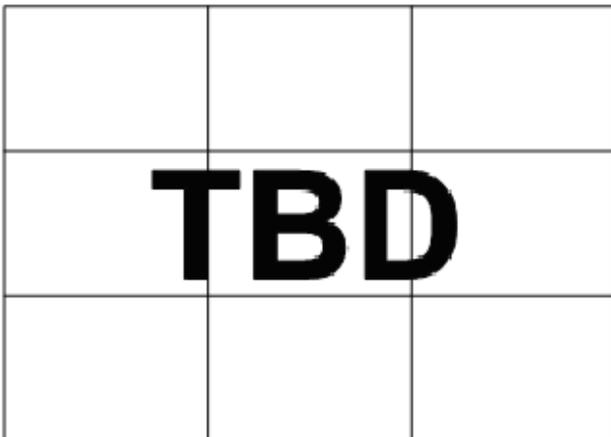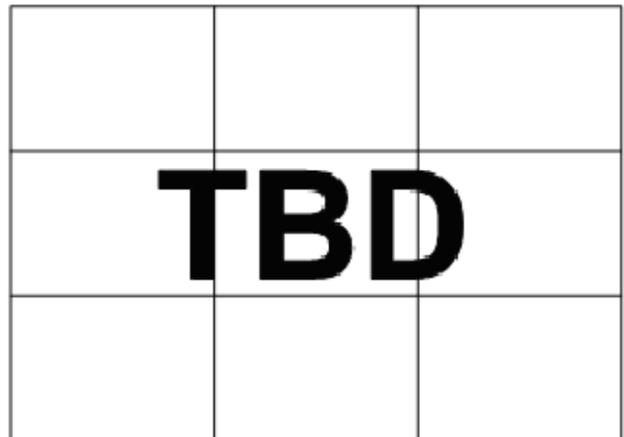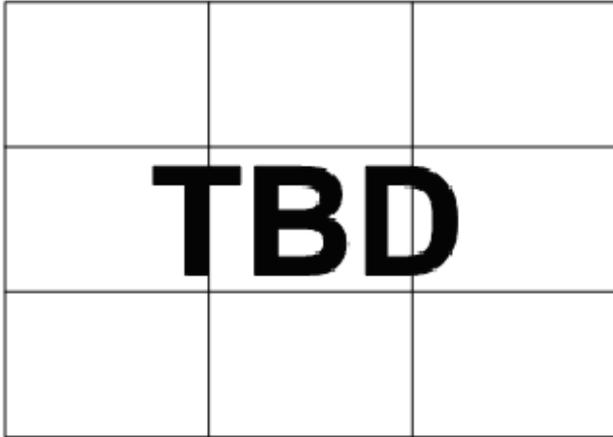*Figure 6. In-Band Gain vs. VGN2 over Supply and Temperature*
(BW Setting = 63 MHz)

Figure 9. Gain Conformance vs. VGN2 over Supply and Temperature
(Bandwidth Setting = 63 MHz)

Figure 7. In-Band Gain vs. VGN3 over Supply and Temperature
(BW Setting = 63 MHz)

Figure 10. Gain Conformance vs. VGN3 over Supply and Temperature
(Bandwidth Setting = 63 MHz)

TBD

Figure 11. Gain vs. Frequency over VGN1/VGN2/VGN3
(BW Setting = 63 MHz)

TBD

Figure 12. Digital Gain vs. Frequency; VGN1/VGN2/VGN3 = 0 V
(BW Setting = 63 MHz)

TBD

Figure 13. Gain Matching Between Channels vs. VGN1/VGN2/VGN3
(BW Setting = 63 MHz)

TBD

Figure 14. OP1dB vs. Gain
(Bandwidth Setting = 63 MHz)

TBD

Figure 15. Frequency Response over Supply and Temperature;
VGN1/VGN2/VGN3 = 0 V

TBD
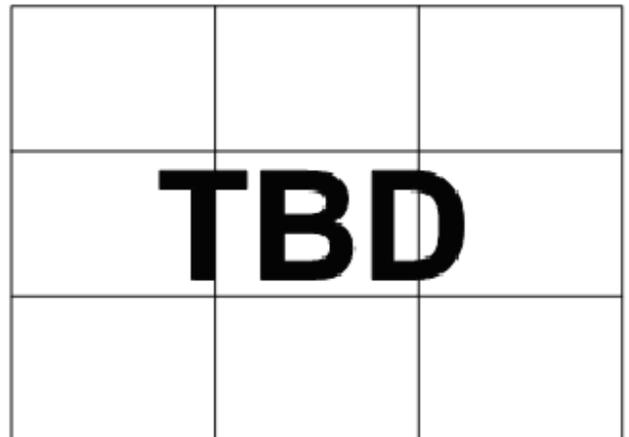
Figure 16. Frequency Response vs. BW Setting (Linear);
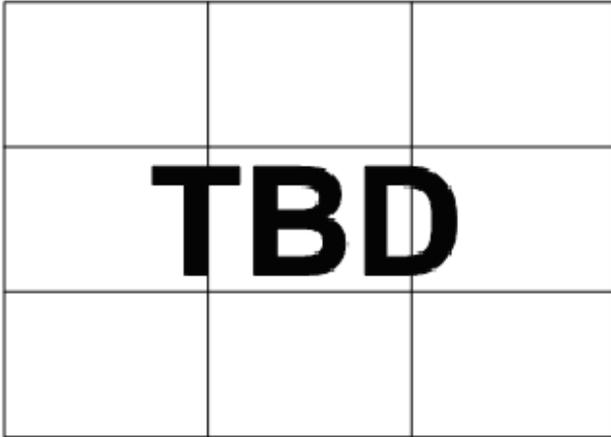*VGN1/VGN2/VGN3 = 0 V*

Figure 17. Frequency Response vs. Bandwidth Setting (Log);
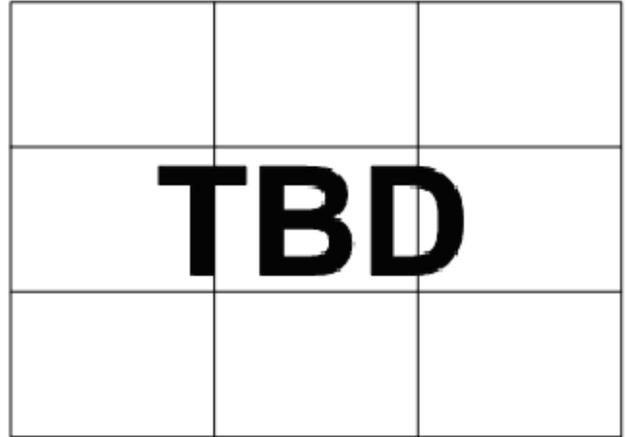*VGN1/VGN2/VGN3 = 0 V*

Figure 20. IQ Group Delay Mismatch vs. Frequency
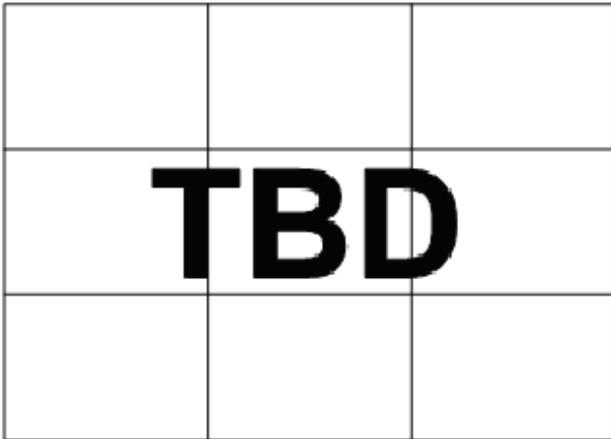*(BW = 30 MHz and 60 MHz)*

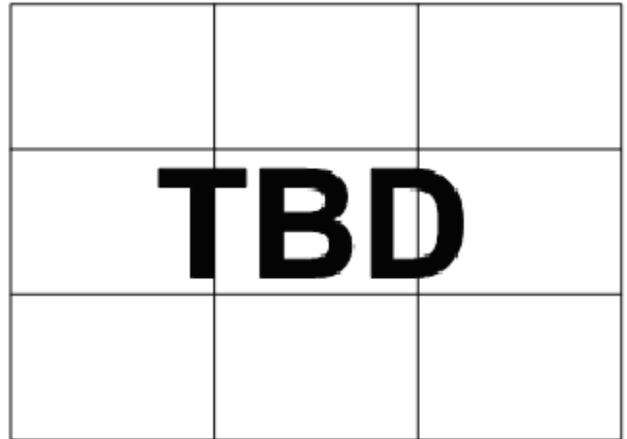*Figure 18. Group Delay vs. Frequency; VGN1/VGN2/VGN3 = 0 V*

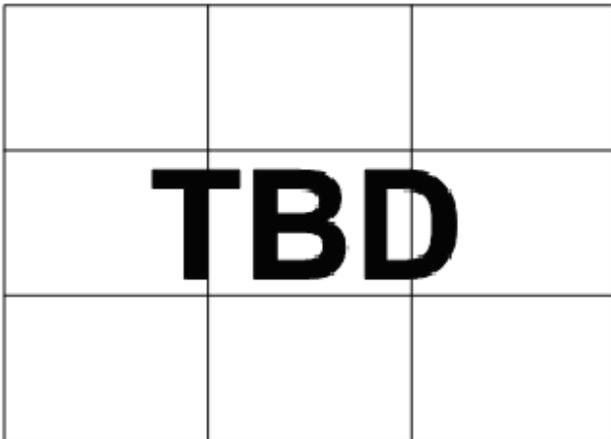*Figure 21. IQ Amplitude Mismatch vs. Frequency; VGN1/VGN2/VGN3 = 0 V*

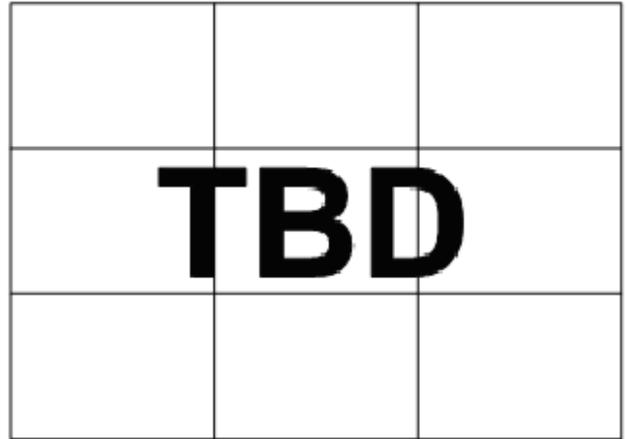*Figure 19. IQ Group Delay Mismatch vs. Frequency (BW = 7 MHz and 15 MHz)*

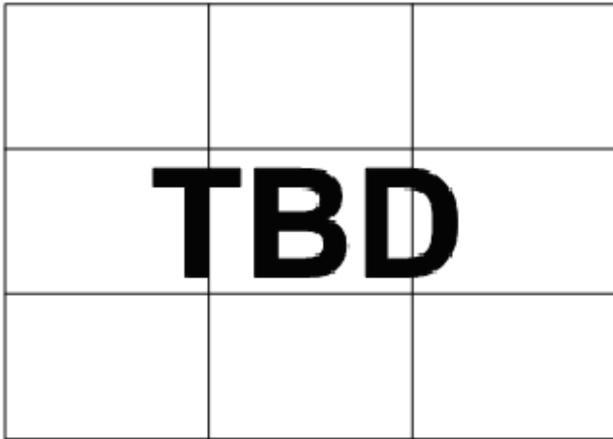*Figure 22. Noise Figure vs. Analog Gain over Digital Gain; BW = 63 MHz*

Figure 23. Noise Figure vs. Analog Gain over BW setting; Digital Gain = 0000001

Figure 26. Output Noise Density vs. Frequency; BW = 7 MHz, Digital Gain = 0000001

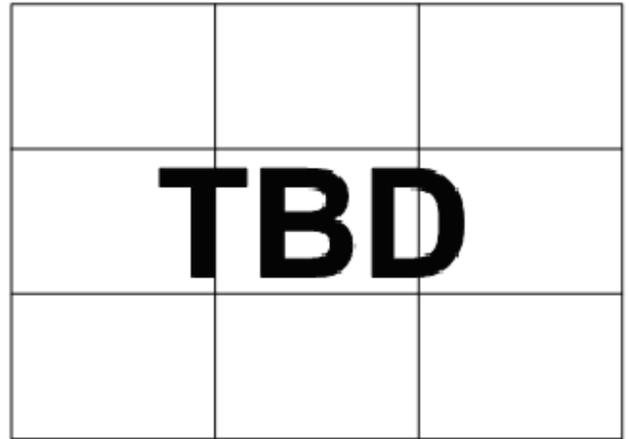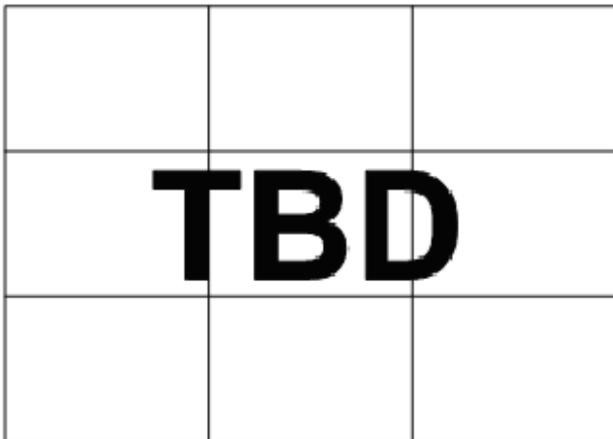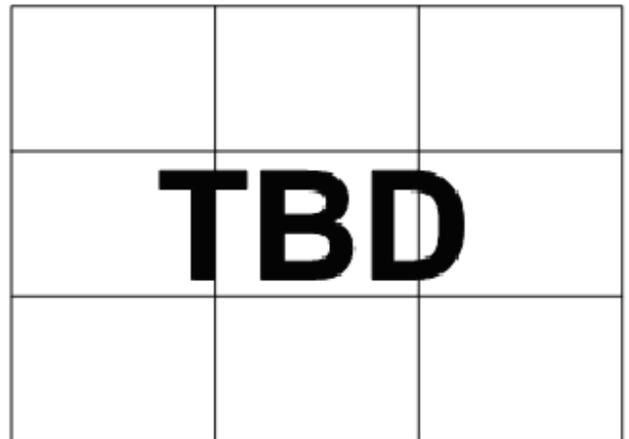Figure 24. Output Noise Density vs. Analog Gain over Digital Gain; BW = 63 MHz

Figure 27. Output Noise Density vs. Frequency; BW = 60 MHz, Digital Gain = 0000001
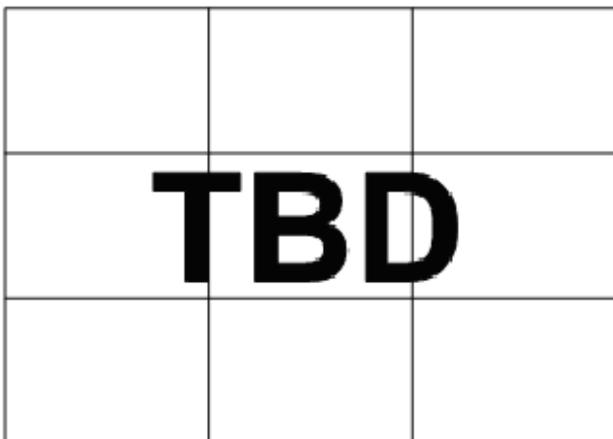
Figure 25. Output Noise Density vs. Gain over Bandwidth Setting; Digital Gain = 0000001
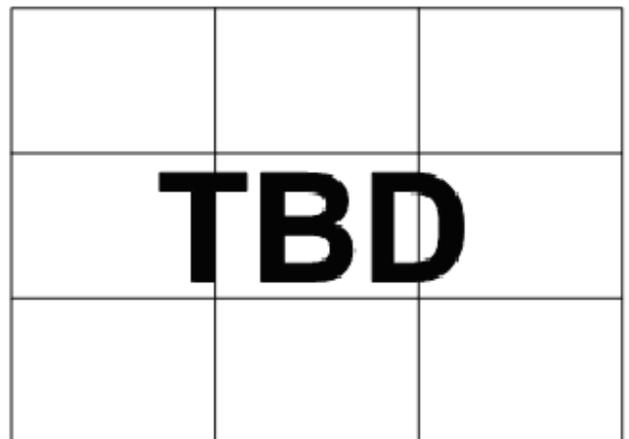
Figure 28. Output Noise Density vs. Input CW Block level; BW = 63 MHz, Digital Gain = 0000001
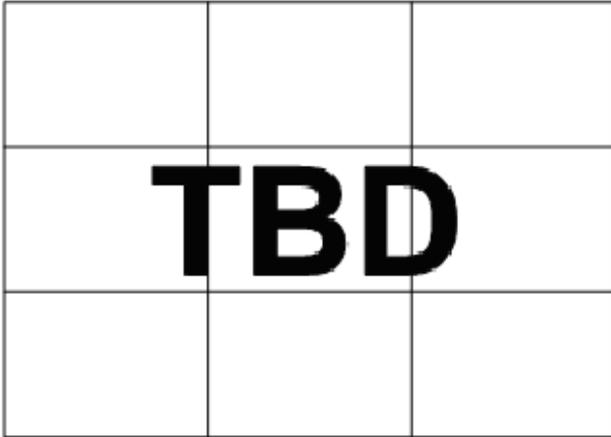
Figure 29. HD2 and HD3 vs. Gain over Supply and Temperature;
BW = 63 MHz, 16 MHz Fundamental Tone, Digital Gain = 1111110

Figure 30. HD2 and HD3 vs. Gain over Supply and Temperature;
BW = 63 MHz, 16 MHz Fundamental Tone, Digital Gain = 1111111

Figure 31. HD2 and HD3 vs. Gain over VOCM; BW = 63 MHz, 16 MHz
Fundamental Tone

Figure 32. HD2 and HD3 vs. VPK, DC-Coupled; BW = 63 MHz,
16 MHz Fundamental Tone

Figure 33. HD2 and HD3 vs. VPK, AC-Coupled; BW = 63 MHz,
16 MHz Fundamental Tone
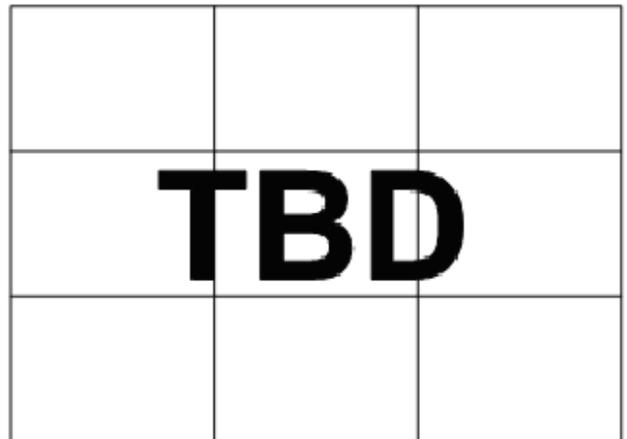
Figure 34. Input IP2 and IP3 vs.VGA1 Gain (AC-Coupled)
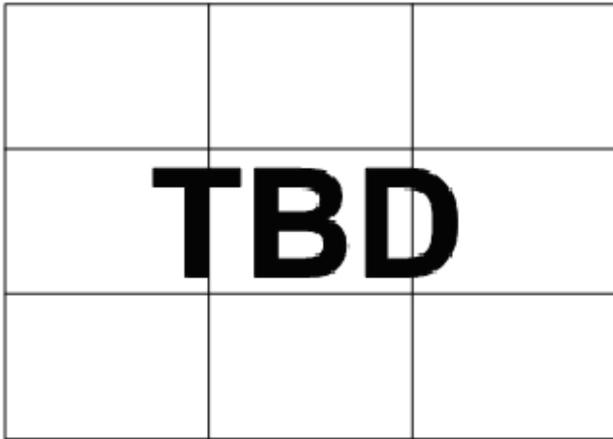
Figure 35. In-Band OIP3 vs. V$_{OUT}$ (V p-p) over Temperature; BW = 63 MHz, 30 MHz and 31 MHz tones, Digital Gain = 0000001
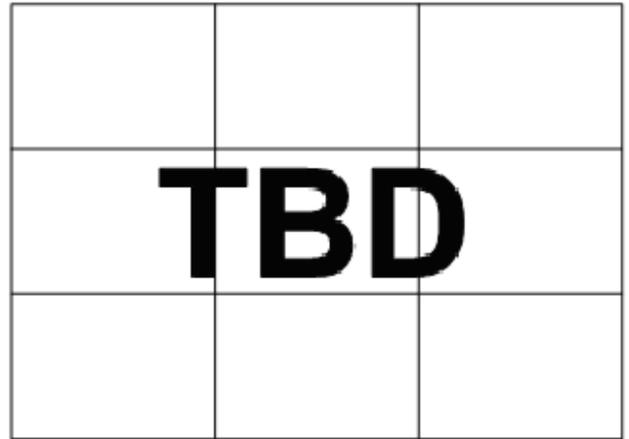
Figure 38. Out-of-Band Input IP2, IMD2 vs. Pin over Digital Gain; 115 MHz and 130 MHz Tones
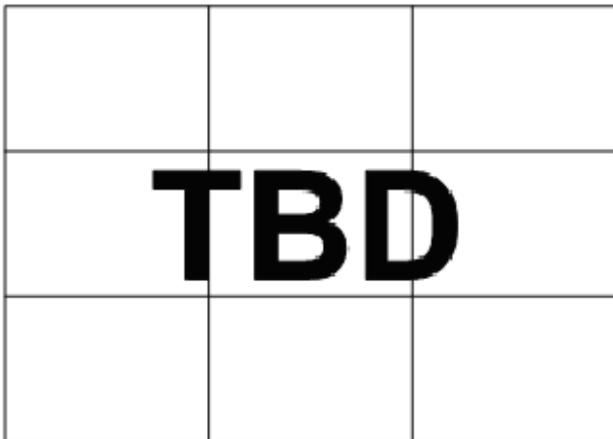
Figure 36. In-Band IMD3 vs. Composite Output Voltage over Gain; 30 MHz and 31 MHz Tones , Digital Gain = 1111110
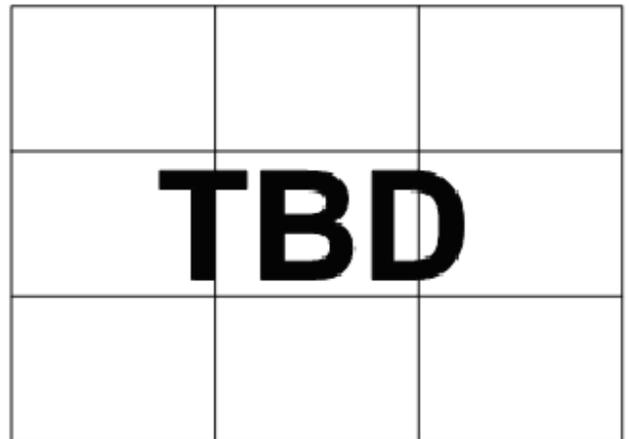
Figure 39. Out-of-Band Input IP3, IMD3 vs. Pin over Digital Gain; 115 MHz and 130 MHz Tones
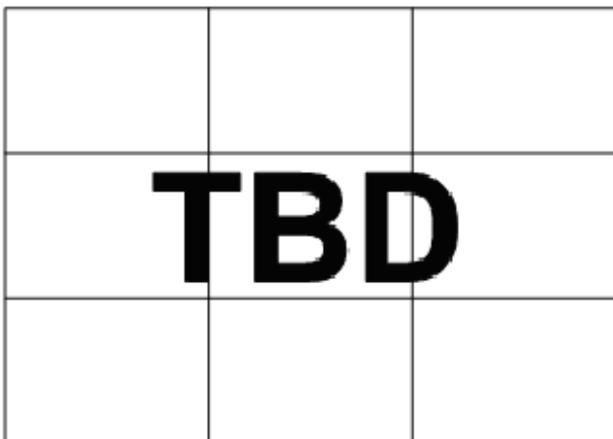
Figure 37. In-Band IMD3 vs. Composite Output Voltage over Gain; 30 MHz and 31 MHz Tones , Digital Gain = 0000001
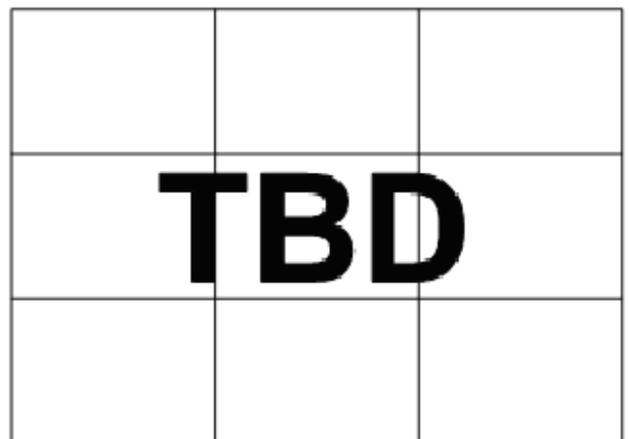
Figure 40. Current Consumption over Bandwidth over Digital Gain
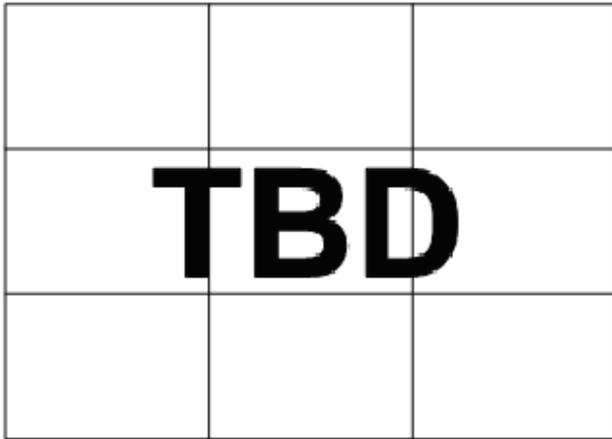
Figure 41. Current Consumption vs. Temperature over Digital Gain
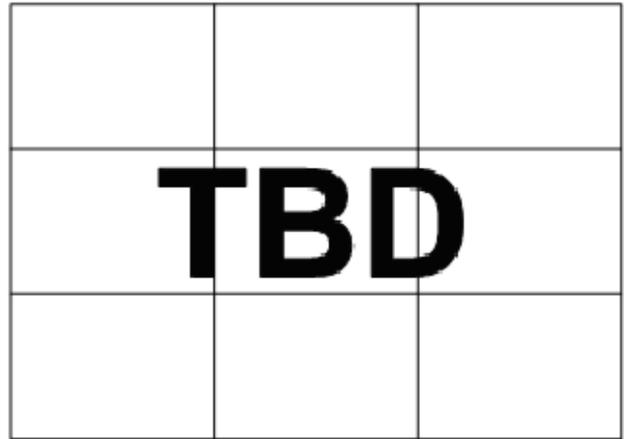
Figure 44. Gain Step Response
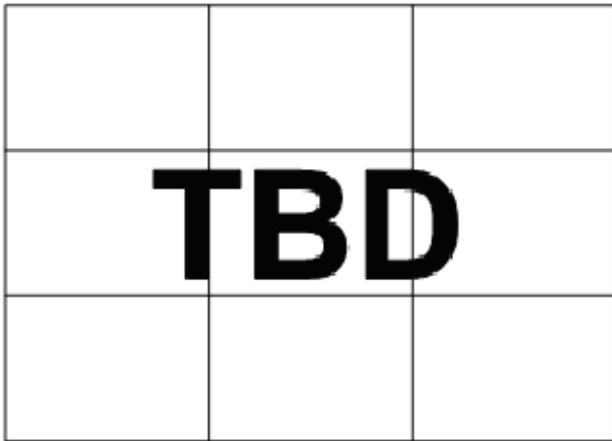
Figure 42. Common Mode Rejection Ratio vs. Frequency
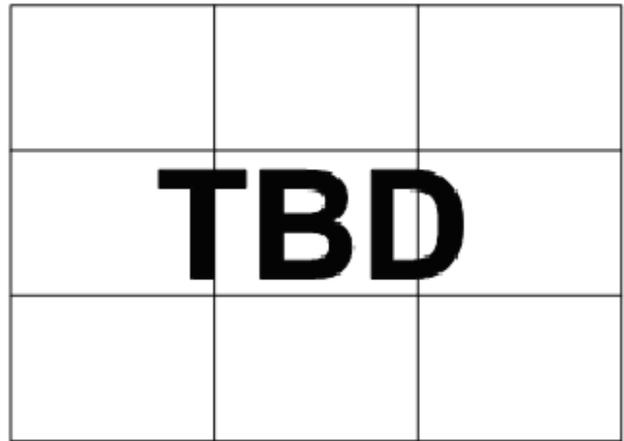
Figure 45. Detector Output vs. Pin over Temperature;
VGN1 = 0.5 V, VGN2 = VGN3 = 0 V
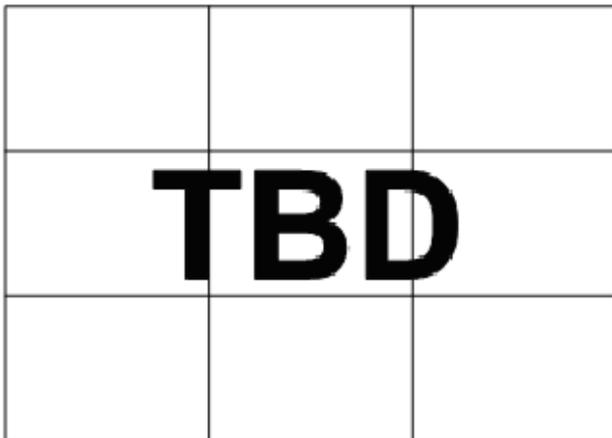
Figure 43. Detector Time Domain Response
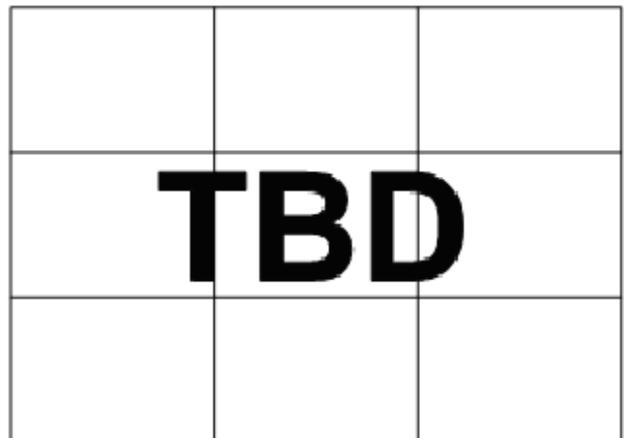
Figure 46. Detector Hold Time vs. RAVG
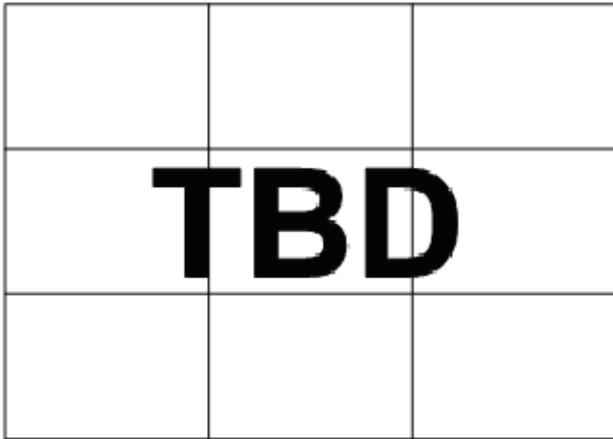
Figure 47. Detector Reset Time Domain Response

BYPASS MODE

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, High Power mode, digital gain code B8:B2 = 1111110, and B1 = 0 unless otherwise noted.
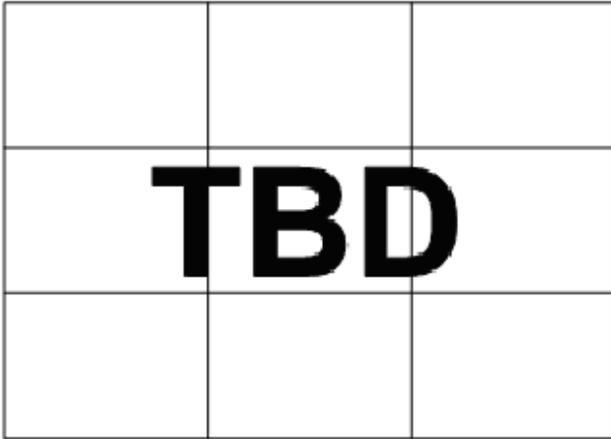
Figure 48. Frequency Response over Supply and Temperature
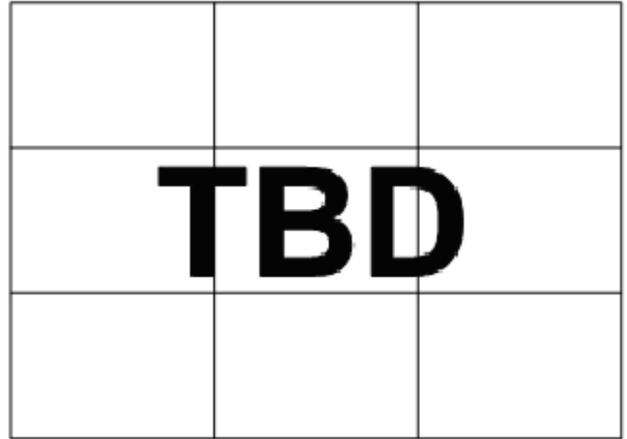
Figure 51. Channel Isolation (OUTA to OUTB) vs. Frequency
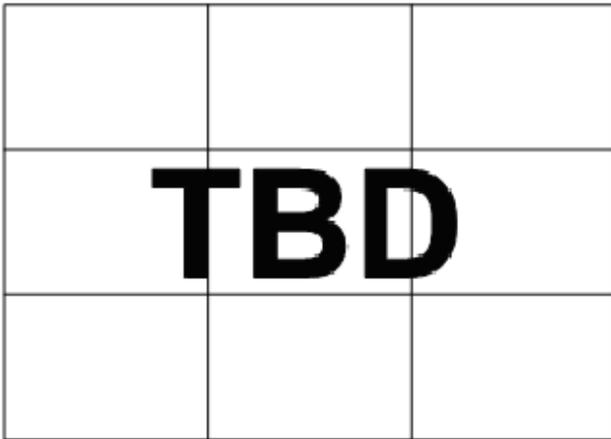
Figure 49. Group Delay vs. Frequency
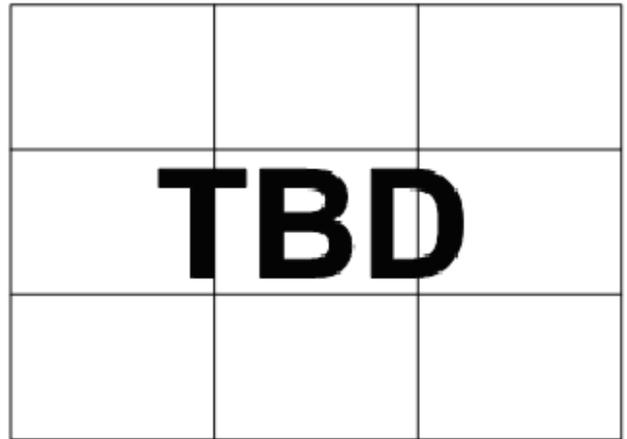
Figure 52. Noise Figure vs. Analog Gain over Digital Gain
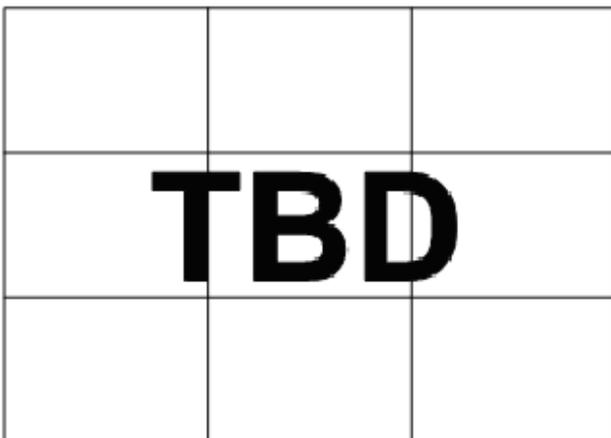
Figure 50. Output Noise Density vs. Frequency over Analog Gains;
Digital Gain = 0000001
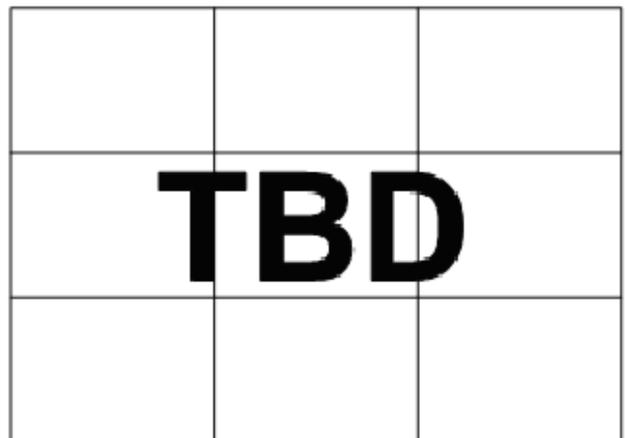
Figure 53. Output Noise Density vs. Analog Gain over Digital Gain
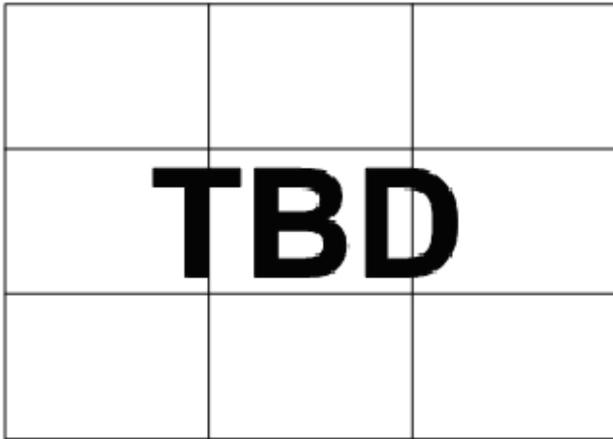
Figure 54. HD2 vs. Gain over Supply and Temperature
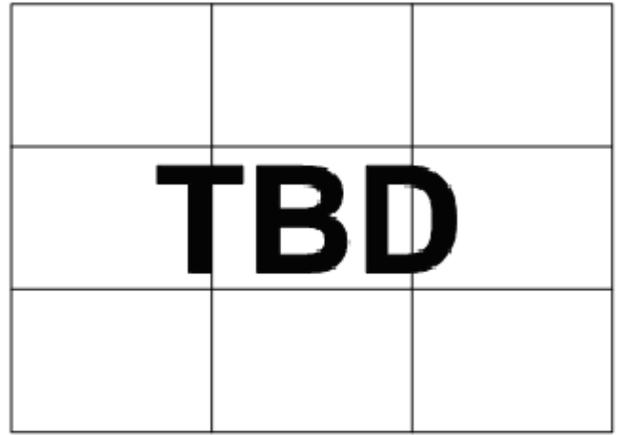
Figure 57. HD2 vs. Gain over Output Common-Mode Voltage
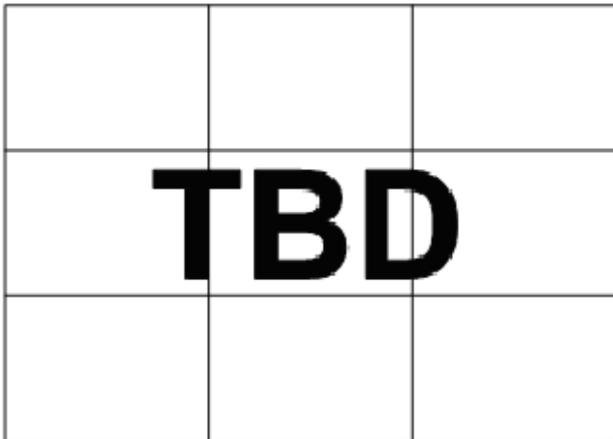
Figure 55. HD3 vs. Gain over Output Common-Mode Voltage
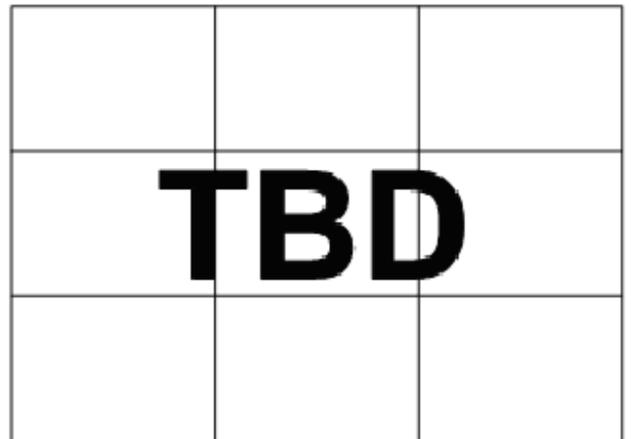
Figure 58. HD2/3 vs. Composite Output Voltage over VOCM;
VGN1/VGN2/VGN3 = 1 V, 60 MHz Fundamental
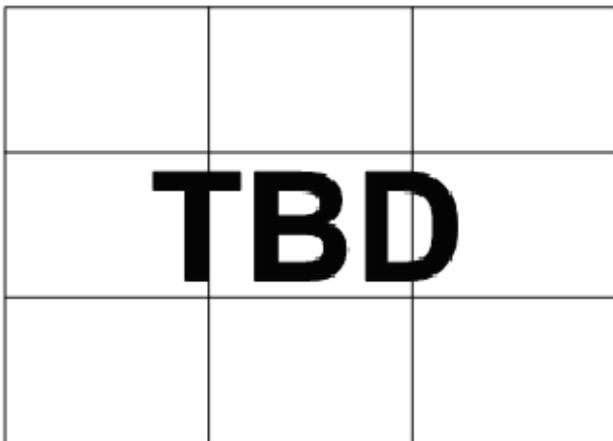
Figure 56. HD3 vs. Gain over Supply and Temperature
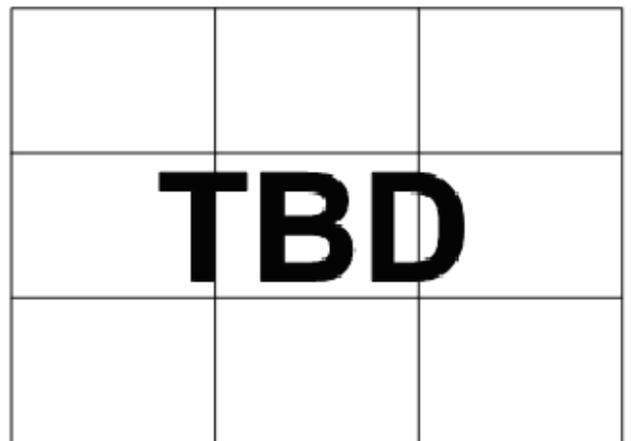
Figure 59. In=Band OIP3 vs. Gain over Temperature; Digital Gain = 0000001
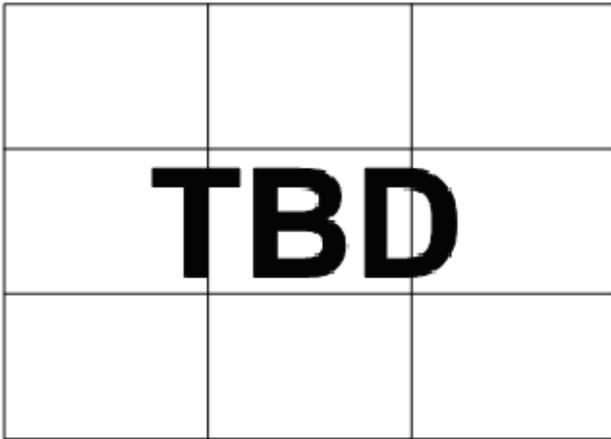
Figure 60. HD2 and HD3 vs. VPK (DC-Coupled); 60 MHz Tones
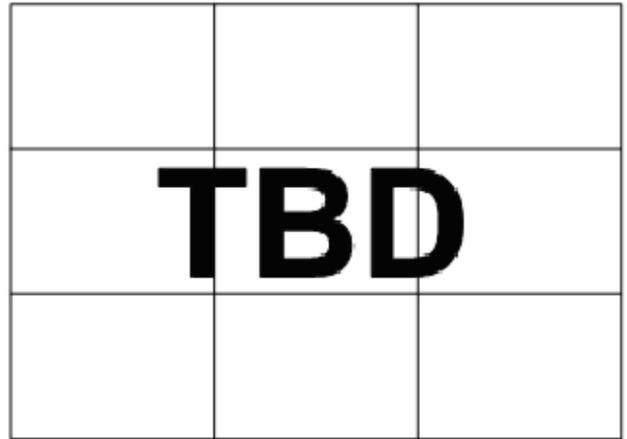
Figure 62. Bandwidth vs. Gain
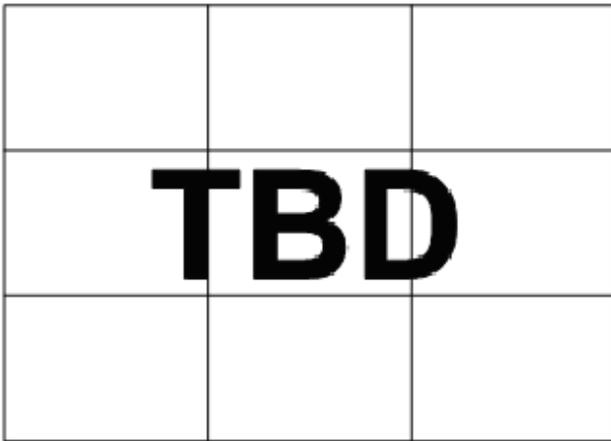
Figure 61. HD2 and HD3 vs. VPK (AC-Coupled); 60 MHz Tones
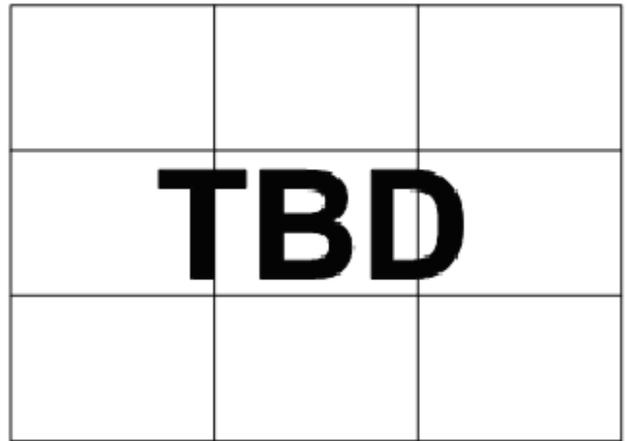
Figure 63. Detector Output vs. Pin over Temperature; VGN1 = 0.5 V, VGN2/VGN3 = 0 V

MIXED POWER AND FILTER MODES

VPS = 3.3 V, T_A = 25°C, Z_{LOAD} = 400 Ω, digital gain code B8:B2 = 1111110, and B1 = 0 unless otherwise noted.
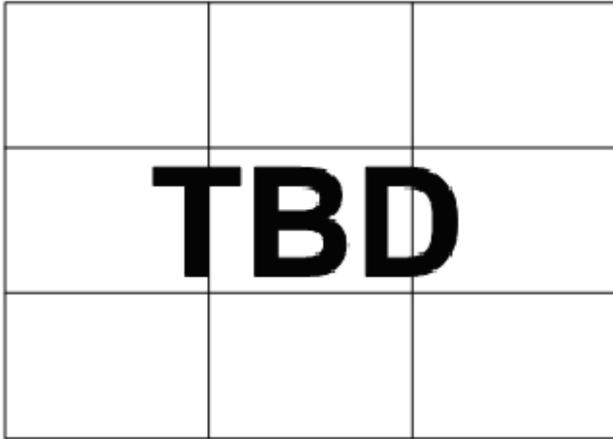
Figure 64. Input Impedance vs. Frequency, VGN1/VGN2/VGN3 = 0 V
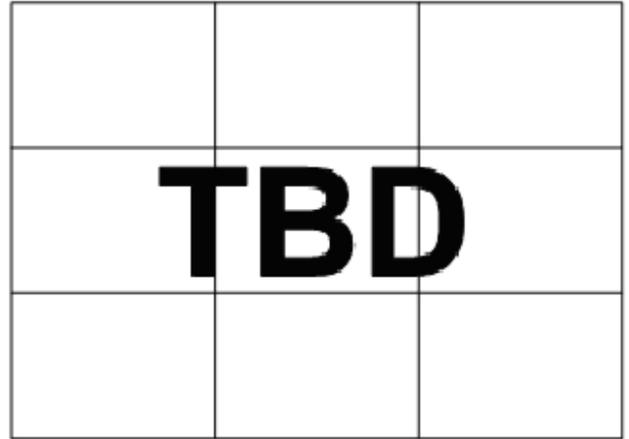
Figure 66. Common-Mode Rejection Ratio vs. Frequency
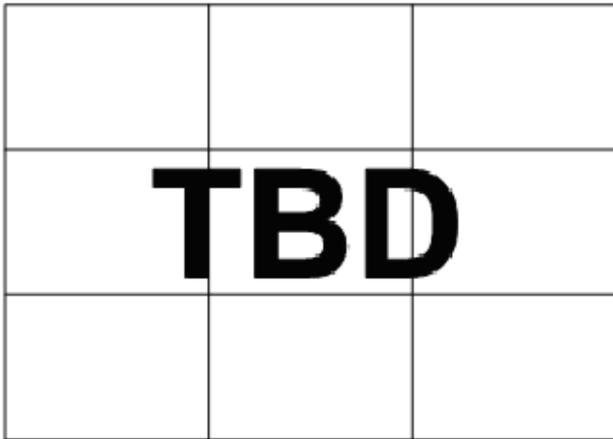
Figure 65. Output Impedance vs. Frequency; VGN1/VGN2/VGN3 = 0 V
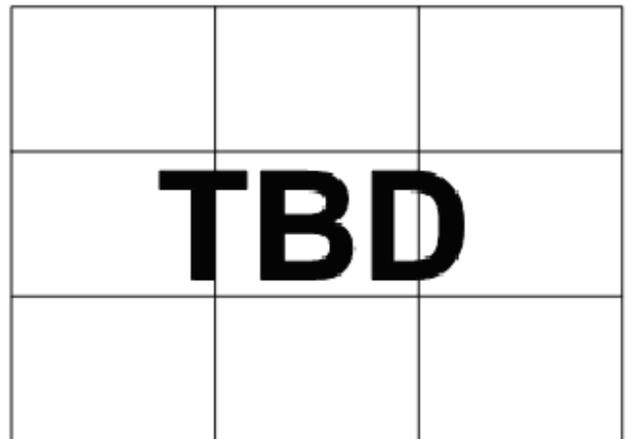
Figure 67. Channel Isolation (Output to Output) vs. Frequency

REGISTER MAP AND CODES

The filter frequency, amplifier gains, filter bypass mode, and offset correction loops can be programmed using the SPI interface. Table 5 provides the bit map for the internal 15-bit register of the ADRF6518.

Table 4. Filter Mode and Power Mode Options

| B9 | Filter | |
	Bypass	Active
0	VGA, low power; filter off	VGA, low power; filter low power
1	VGA, high power; filter off	VGA, low power; filter high power

Table 5. Register Map

MSB   LSB

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
Filter frequency code and filter bypass mode						Power mode	VGA1 gain		VGA2 gain		VGA3 gain		Postamp	Offset disable
Code = 1 dB corner in MHz For example, 31 MHz = 011111 (MSB first) Use 000000 for filter bypass mode						0: low power 1: high power Use 1 for filter BW > 31 MHz, in filter active mode Use 1 for channel BW > 60 MHz, in filter bypass mode	00: 15 dB 01: 12 dB 10: 9 dB 11: 9 dB		00: 21 dB 01: 18 dB 10: 15 dB 11: 12 dB		00: 21 dB 01: 18 dB 10: 15 dB 11: 12 dB		0: 3 dB 1: 9 dB	0: enable 1: disable

THEORY OF OPERATION

The ADRF6518 consists of a matched pair of input VGAs followed by programmable filters, and then by a cascade of two variable gain amplifiers and output ADC drivers. The filters can be bypassed and powered down through the SPI interface for operation beyond the maximum filter bandwidth. The block diagram of a single channel is shown in Figure 68.

The programmability of the filter bandwidth and of the prefiltering and postfiltering fixed gains through the SPI interface offers great flexibility when coping with signals of varying levels in the presence of noise and large, undesired signals near the desired band. The entire differential signal chain is dc-coupled with flexible interfaces at the input and output. The bandwidth and gain setting controls for the two channels are shared, ensuring close matching of their magnitude and phase responses. The ADRF6518 can be fully disabled through the ENBL pin.
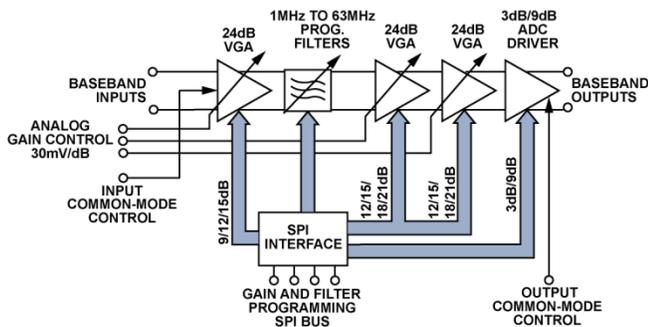
Figure 68. Signal Path Block Diagram for a Single Channel of the ADRF6518

Filtering and amplification are fundamental operations in any signal processing system. Filtering is necessary to select the intended signal while rejecting out-of-band noise and interferers. Amplification increases the level of the desired signal to overcome noise added by the system. When used together, filtering and amplification can extract a low level signal of interest in the presence of noise and out-of-band interferers. Such analog signal processing alleviates the requirements on the analog, mixed signal, and digital components that follow.

INPUT VGAs

The input VGAs provide a convenient interface to the sensitive filter sections that follow. They are designed to have a low noise figure and high linearity. The combination of analog gain control and digital gain settings allow a wide range of input signal levels to be conditioned to drive the filters at up to 2 V p-p amplitude. The VGAs set a differential input impedance of 400 Ω.

The baseband input signal can be ac-coupled or dc-coupled via Pin 7 selection. When the signal is dc-coupled, wide input common-mode voltage is supported by having an optional 5 V supply on Pin 8, VPI. The default common-mode voltage is VPI/2, which is available on the dual function Pin 7, VICM/AC, to set the output common-mode voltage of the driving circuit. However, this is optional and input common-mode can be independently set within the supported range. For a 3.3 V

supply on VPI, the input common mode can range from 1.35 V to 1.95 V, while maintaining a 5 V p-p input level at >60 dBc HD2 and HD3. For a 5 V supply on VPI, the input common-mode range extends to 1.35 V to 3.1 V. Extra current is drawn from the VPI supply to support an input common mode greater than the midvalue of the main 3.3 V supply, that is, VPS/2.

The VICM/AC voltage is not buffered and must be sensed at a high impedance point to prevent it from being loaded down. When the baseband input signal is ac-coupled, pull the VICM/AC pin low to activate the internal bias for the input stage.

The input VGAs have analog gain control of 24 dB, followed by a digital gain settings of 9 dB, 12 dB, or 15 dB, selectable through the SPI (see the Register Map and Codes section). The VGAs are based on the Analog Devices, Inc., patented X-AMP® architecture, consisting of tapped 24 dB attenuators, followed by programmable gain amplifiers. The X-AMP architecture generates a continuous linear-in-dB monotonic gain response with low ripple. The analog gain of the VGA sections are controlled through the high impedance VGN1 pin with an accurate slope of 30 mV/dB. Adjust the VGA analog gain through an AGC mechanism, such that 2 V p-p at the output of the first VGA is not exceeded. If, however, the input signal is small enough, the first VGA can be set at full gain for best noise figure (NF) performance and gain control achieved in the second or third VGA.

Driving ADRF6518 Single-Ended

The input structure of the ADRF6518 is designed for differential drive. However, with some performance degradation, it can be driven single ended, especially at low bandwidth signals. See the Applications Information section for guidance on single-ended drive.

PEAK DETECTOR

To measure the signal level at the critical interface of the VGA1 output and the programmable filter input, a peak detector has been implemented. The peak detector simultaneously measures both channels at the VGA1 output and reports the bigger of the two at the VPK pin. The on-chip holding capacitor and negligible leakage at the internal node ensure a large droop time of the order of a millisecond, which is a function of the peak voltage as well. Bigger peak voltage results in longer droop time. The droop time can be adjusted down by placing a resistor between the RAVG and VPOS pins. Typical values of RAVG can range from 1 MΩ to 1 kΩ. As the RAVG resistor value is reduced, the peak voltage, VPK, appears as an envelope output. The peak detector has the attack bandwidth of 100 MHz.

The peak detector can be used in an AGC loop to set the appropriate signal level at the filter input. For such an implementation, Filter VPK appropriately, considering that it is a peak hold output. A high pulse of 25 ns or longer duration applied to the SDO/RST dual function pin resets the VPK voltage to 0 V by discharging the internal holding capacitor.

PROGRAMMABLE FILTERS

The integrated programmable filter is the key signal processing function in the ADRF6518. The filters follow a six-pole Butterworth prototype response that provides a compromise between band rejection, ripple, and group delay. The 0.5 dB bandwidth is programmed from 1 MHz to 63 MHz in 1 MHz steps via the serial programming interface (SPI) as described in the Programming fZ\V36D\' #* section.

The filters are designed so that the Butterworth prototype filter shape and group delay responses vs. frequency are retained for any bandwidth setting. Figure 69 and Figure 70 illustrate the ideal six-pole Butterworth gain and group delay responses, respectively. The group delay, τ_g, is defined as

$$\tau_g = -\partial\varphi/\partial\omega$$

where:
φ is the phase in radians.
$\omega = 2\pi f$ is the frequency in radians per second.

Note that for a frequency scaled filter prototype, the absolute magnitude of the group delay scales inversely with the bandwidth; however, the shape is retained. For example, the peak group delay for a 28 MHz bandwidth setting is 14× less than for a 2 MHz setting.
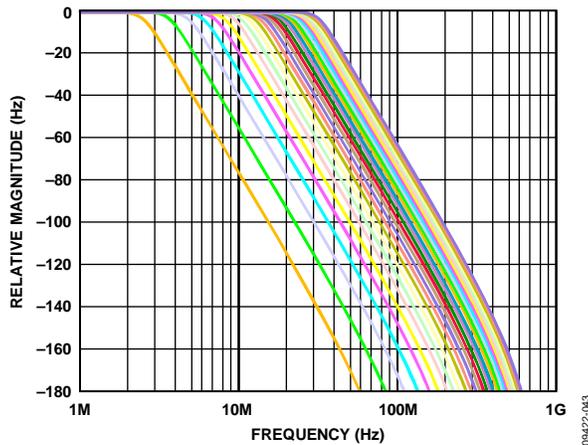
Figure 69. Sixth-Order Butterworth Magnitude Response for 0.5 dB Bandwidths Programmed from 2 MHz to 29 MHz in 1 MHz Steps
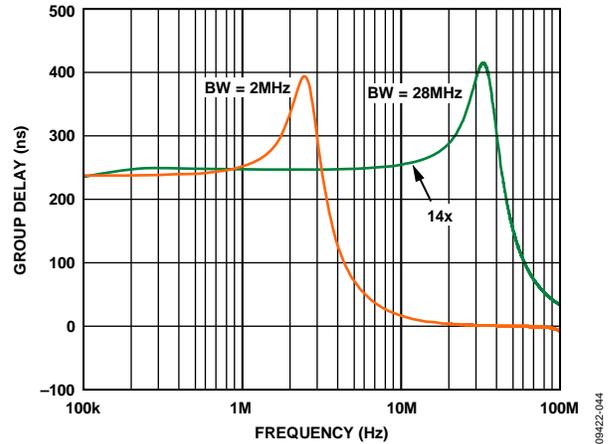
Figure 70. Sixth-Order Butterworth Group Delay Response for 0.5 dB Bandwidths Programmed to 2 MHz and 28 MHz

The corner frequency of the filters is defined by RC products, which can vary by ±30% in a typical process. Therefore, all the parts are factory calibrated for corner frequency, resulting in a residual ±7.5% corner frequency variation over the −40°C to +85°C temperature range. Although absolute accuracy requires calibration, the matching of RC products between the pair of channels is better than 1% by observing careful design and layout practices. Calibration and excellent matching ensure that the magnitude and group delay responses of both channels track together, a critical requirement for digital IQ-based communication systems.

Bypassing the Filters

For higher bandwidth applications, filters of the ADRF6518 can be bypassed via the SPI. In the bypass mode, filters are disabled and power consumption is significantly reduced. The bandwidth of cascaded VGAs, which is significantly larger than 63 MHz maximum of the filters, is fully realized in the bypass mode.

VARIABLE GAIN AMPLIFIERS (VGAs)

The cascaded VGA2 and VGA3 are also based on the X-AMP architecture, and each has 24 dB gain range with separate high impedance gain control inputs, VGN2 and VGN3. The VGA structures of the second and third VGAs are identical to that of the first VGA. However, these have slightly higher noise figure and less drive level capability. Their output is rated at 1 V p-p for >60 dBc HD2 and HD3. Depending on the input signal range, the second or third VGA or both can be used for AGC purposes. The critical level to consider while making this choice is the signal level at the output of the VGAs, which must not exceeded 1 V p-p to maintain low distortion.

The fixed gain following both of the variable gain sections can also be programmed to 12 dB, 15 dB, 18 dB, or 21 dB to maximize the dynamic range.

OUTPUT BUFFERS/ADC DRIVERS

The low impedance (<10 Ω) output buffers of the ADRF6518 are designed to drive either ADC inputs or subsequent amplifier stages. They are capable of delivering up to 4 V p-p composite two-tone signals into 1 kΩ differential loads with >60 dBc IMD3. The output common-mode voltage defaults to VPS/2, but it can be adjusted from 900 mV to 2.0 V without loss of drive capability by presenting the VOCM pin with the desired common-mode voltage. The high input impedance of VOCM allows the ADC reference output to be connected directly. Even though the output common-mode voltage is adjustable and the offset compensation loop can null the accumulated dc offsets (see the DC Offset Compensation Loop section), it may still be desirable to ac-couple the outputs by selecting the coupling capacitors according to the load impedance and desired bandwidth.

DC OFFSET COMPENSATION LOOP

In many signal processing applications, no information is carried in the dc level. In fact, dc voltages and other low frequency disturbances can often dominate the intended signal and consume precious dynamic range in the analog path and bits in the data converters. These dc voltages can be present with the desired input signal or can be generated inside the signal path by inherent dc offsets or other unintended signal-dependent processes such as self-mixing or rectification.

Because the ADRF6518 is fully dc-coupled, it may be necessary to remove these offsets to realize the maximum signal-to-noise ratio (SNR). The external offsets can be eliminated with ac-coupling capacitors at the input pins; however, that requires large value capacitors because the impedances can be fairly low, and high-pass corners may need to be <10 Hz in some cases. To address the issue of dc offsets, the ADRF6518 provides an offset correction loop that nulls the output differential dc level, as shown in Figure 71. If the correction loop is not required, it can be disabled through the SPI port.
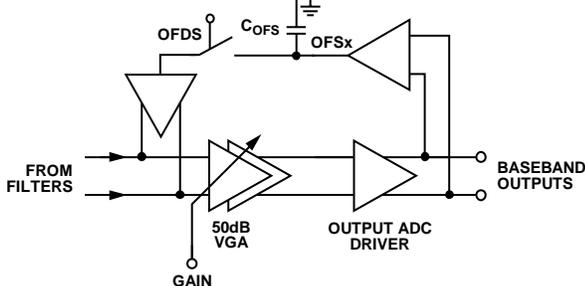
Figure 71. Offset Compensation Loop Operates Around the VGA and Output Buffer

The offset control loop creates a high-pass corner, f_{HP}, that is superimposed on the normal Butterworth filter response when filters are enabled. Typically, f_{HP} is many orders of magnitude lower than the lower programmed filter bandwidth so that there is no interaction between them. Setting f_{HP} is accomplished with capacitors, C_{OFS}, from the OFS1 and OFS2

pins to ground. Because the correction loop works around the VGA sections, f_{HP} is also dependent on the total gain of the cascaded VGAs. In general, the expression for f_{HP} is given by

$$f_{HP} \text{ (Hz)} = 6.7 \times Post\ Filter\ Linear\ Gain/C_{OFS}\ (\mu F)$$

where *Post Filter Linear Gain* is expressed in linear terms, not in decibels (dB), and is the gain following the filters, which excludes the VGA1 gain.

Note that f_{HP} increases in proportion to the gain. For this reason, C_{OFS} should be chosen at the highest operating gain to guarantee that f_{HP} is always below the maximum limit required by the system.

PROGRAMMING THE ADRF6518

The 0.5 dB corner frequencies for both filters, the digital gains of all the VGAs, and the output buffers are programmed simultaneously through the SPI port. In addition to these, enabling the dc offset compensation loop and power mode selection are also controlled through SPI port. A 16-bit register stores the 6-bit code for corner frequencies of 1 MHz through 63 MHz and filter bypass, as well as the codes for VGA gains, and the buffer gain (see Table 5). The SPI protocol not only allows these selections to be written to the DATA pin, but also allows the stored code to be read back via the SDO/RST pin.

The latch enable (LE) pin must first go to a Logic 0 for a read or write cycle to begin. On the next rising edge of the clock (CLK), a Logic 1 on the DATA pin initiates a write cycle, whereas a Logic 0 on the DATA pin initiates a read cycle. In a write cycle, the next 15 CLK rising edges latch the desired 15-bit code, LSB first. This results in 16-bit code, including the first Logic 1 to initiate a write cycle. When LE goes high, the write cycle is completed and different codes are presented various blocks that need programming. In a read cycle, the next 15 CLK falling edges present the stored 15-bit code, LSB first. When LE goes high, the read cycle is completed. Detailed timing diagrams are shown in Figure 2 and Figure 3.

NOISE CHARACTERISTICS

The output noise behavior of the ADRF6518 depends on the gain and bandwidth settings. VGA1 noise dominates in the filter bypass mode and at high filter corner settings. While at low corner settings, filter noise tends to dominate.

The filter contributes a noise spectral density profile that is flat at low frequencies, peaks near the corner frequency, and then rolls off as the filter poles roll off the gain and noise. The magnitude of the noise spectral density contributed by the filter, expressed in nV/√Hz, varies inversely with the square root of the bandwidth setting, resulting in filter noise in nV that is nearly constant with the bandwidth setting. However, with VGA1 NF being lower than the filter, VGA1 tends to dominate the overall NF. At higher frequencies, after the filter noise rolls off, the noise floor is set by the VGAs.

Each of the X-AMP VGA sections used in the ADRF6518 contributes a fixed noise spectral density to its respective output,

independent of the analog gain setting. With the digital gain change, however, VGA output noise changes, because the gain setting resistors values change. As an example, VGA1 NF corresponding to a 15 dB gain setting is 14 dB, whereas for 9 dB gain, the NF is 15.6 dB. When cascaded, the total noise contributed by the VGAs at the output of the ADRF6518 increases gradually with higher gain. This is apparent in the noise floor variation at high frequencies at different VGA gain settings. The exact relationship depends on the programmed fixed gain of the amplifiers. At lower frequencies within the filter bandwidth setting, the VGAs translate the filter noise directly to the output by a factor equal to the gain following the filter.

At low values of VGA gain, the noise at the output is the flat spectral density contributed by the last VGA. As the gain increases, more of the filter and first VGA noise appears at the output. Because the intrinsic filter noise density increases at lower bandwidth settings, it is more pronounced than it is at higher bandwidth settings. In either case, the noise density asymptotically approaches the limit set by the VGAs at the highest frequencies. For other values of VGA gain and bandwidth setting, the detailed shape of the noise spectral density changes according to the relative contributions of the filters and VGAs.

Because the noise spectral density outside the filter bandwidth is limited by the VGA output noise, it may be necessary to use an external, fixed frequency, passive filter prior to analog-to-digital conversion to prevent noise aliasing from degrading the signal-to-noise ratio. A higher sampling rate, relative to the maximum required ADRF6518 corner frequency setting, reduces the order and complexity of this external filter.

DISTORTION CHARACTERISTICS

To maintain low distortion through the cascaded VGAs and filter of the ADRF6518, consider the distortion limits of each stage. The first VGA has higher signal handling capability and bandwidth than VGA2 and VGA3, because it must cope with out-of-band signals that can be larger than the in-band signals. In the filter mode, these out-of-band signals are filtered before reaching VGA2 and VGA3. It is important to understand the signals presented to the ADRF6518 and to match these signals with the input and output characteristics of the part. It is useful to partition the ADRF651 into the front end, composed of VGA1 and the filter, and the back end, composed of VGA2 and VGA3 and the output buffers.

VGA1 can handle a maximum analog attenuation setting of 5 V p-p without experiencing appreciable distortion at the input. In most applications, VGA1 gain should be adjusted such that the maximum signal presented at the filter inputs (or VGA2 input in filter bypass mode) is <1.5 V p-p. At this level, the front end does not limit the distortion performance. The peak detector output, VPK, can be used as an indicator of the signal level present at this critical interface. Choose the second and third VGA gains such that their output level does not exceed 1 V p-p. The output buffer gain should be set to 3 dB if

the desired output is <1.4 V p-p and 9 dB for a desired output of >1.4 V p-p.

For these signal level considerations, the out-of-band signal, if larger than the desired in-band signal, should be addressed. In filter active mode, such an out-of-band signal only affects the VGA1 operation, because it is filtered out by the filter and does not affect the following stages. In this case, a high VGA2 and VGA3 gain may be needed to raise the small desired signal to a higher level at the output. In the filter bypass mode, such out-of-band signals may need to be filtered prior to the ADRF6518.

The overall distortion introduced by the part depends on the input drive level, including the out-of-band signals, and the desired output signal level. To achieve best distortion performance and the desired overall gain, keep in mind the maximum signal levels indicated previously when selecting different VGA gains.

To distinguish and quantify the distortion performance of the input section, two different IP3 specifications are presented. The first is called in-band IP3 and refers to a two-tone test where the signals are inside the filter bandwidth. This is exactly the same figure of merit familiar to communications engineers in which the third-order intermodulation level, IMD3, is measured.

To quantify the effect of out-of-band signals, a new out-of-band (OOB) IIP3 figure of merit is introduced. This test also involves a two-tone stimulus; however, the two tones are placed out-of-band so that the lower IMD3 product lands in the middle of the filter pass band. At the output, only the IMD3 product is visible because the original two tones are filtered out. To calculate the OOB IP3 at the input, the IMD3 level is referred to the input by the overall gain. The OOB IIP3 allows the user to predict the impact of out-of-band blockers or interferers at an arbitrary signal level on the in-band performance. The ratio of the desired input signal level to the input-referred IMD3 at a given blocker level represents a signal-to-distortion limit imposed by the out-of-band signals.

MAXIMIZING THE DYNAMIC RANGE

When used in the filter mode, the role of the ADRF6518 is to increase the level of a variable in-band signal while minimizing out-of-band signals. Ideally, this is achieved without degrading the SNR of the incoming signal or introducing distortion to the incoming signal.

The first goal is to maximize the output signal swing, which can be defined by the ADC input range or the input signal capacity of the next analog stage. For the complex waveforms often encountered in communication systems, the peak-to-average ratio, or crest factor, must be considered when choosing the peak-to-peak output. From the chosen output signal and the maximum gain of the ADRF6518, the minimum input level can be defined.

As the input signal level increases, the VGA3 gain is reduced from its maximum gain point to maintain the desired fixed output level. VGA2 and VGA1 can then be adjusted as the input

ADRF6518

signal level keeps increasing. This maintains the best NF for the cascaded chain. The output noise, initially dominated by the filter and VGA1 combination, follows the gain reduction, yielding a progressively better SNR. At some point, the VGA3 and VGA2 gains drop sufficiently so that their noise becomes dominant, resulting in a slower reduction in SNR from that point. From the perspective of SNR alone, the maximum input level is reached when the VGA1 reaches its minimum gain.

Distortion must also be considered when maximizing the dynamic range. At low and moderate signal levels, the output distortion is constant and assumed to be adequate for the selected output level. At some point, the input signal becomes large enough that distortion at the input limits the system. This can be kept in check by monitoring peak detector voltage, VPK.

The most challenging scenario in terms of dynamic range is the presence of a large out-of-band blocker accompanying a weaker in-band wanted signal. In this case, the maximum input level is dictated by the blocker and its inclination to cause distortion. After filtering, the weak wanted signal must be amplified to the desired output level, possibly requiring maximum gain on VGA2 and VGA3. In such a case, both the distortion limits associated with the blocker at the input and the SNR limits created by the weaker signal and higher gains are present simultaneously. Furthermore, not only does the blocker scenario degrade the dynamic range, it also reduces the range of input signals that can be handled because a larger part of the gain range is simply used to extract the weak desired signal from the stronger blocker.

KEY PARAMETERS FOR QUADRATURE-BASED RECEIVERS

The majority of digital communication receivers make use of quadrature signaling, in which bits of information are encoded onto pairs of baseband signals that then modulate in-phase (I) and quadrature (Q) sinusoidal carriers. Both the baseband and modulated signals appear quite complex in the time domain with dramatic peaks and valleys. In a typical receiver, the goal is to recover the pair of quadrature baseband signals in the presence of noise and interfering signals after quadrature demodulation. In the process of filtering out-of-band noise and unwanted interferers and restoring the levels of the wanted I and Q baseband signals, it is critical to retain their gain and phase integrity over the bandwidth.

In the filter mode, the ADRF6518 delivers flat in-band gain and group delay, consistent with a six-pole Butterworth prototype filter, as described in the Programmable Filters section. Furthermore, careful design ensures excellent matching of these parameters between the I and Q channels. Although absolute gain flatness and group delay can be corrected with digital equalization, mismatch introduces quadrature errors and intersymbol interference that degrade bit error rates in digital communication systems.

For wideband signals, filters can be bypassed and the ADRF6518 then becomes a dual cascaded chain of three VGAs, offering large gain range options, while maintaining gain and group delay match between the two channels.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 72 shows the basic connections for a typical ADRF6518 application.

SUPPLY DECOUPLING

Apply a nominal supply voltage of 3.3 V to the supply pins, VPS, VPI, and VPSD. The supply voltage must not exceed 3.45 V or drop below 3.15 V for VPS and VPSD. The supply voltage on VPI must not exceed 5.25 V. Decouple each supply pin to ground with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the ADRF6518 device.

The ADRF6518 has two separate supplies: an analog supply and a digital supply. Take care to separate the analog and digital supplies with a large surface-mount inductor of 33 µH. Each supply should then be decoupled separately to its respective ground through a 10 µF capacitor.

INPUT SIGNAL PATH

Each signal path has input buffers, accessed through the INP1, INM1, INP2, and INM2 pins, that set a differential input impedance of 400 Ω. These inputs sit at a nominal common-mode voltage around midsupply.

The inputs can be dc-coupled or ac-coupled. To ac couple the inputs, the user must pull the VICM/AC pin to ground. This provides an input common-mode voltage of VPI/2. To dc couple the inputs, let the VICM pin float. If using direct dc

coupling, the common-mode voltage, V_{CM}, can range from 1.35 V to 2.0 V while VPI = 3.3 V. The user has the option of tying VPI to a voltage up to 5 V. This provides a common-mode range of 1.35 V to 3.1 V. In general, the minimum input common-mode voltage is always 1.35 V, but the maximum common-mode voltage is $V_{CM\_MAX} = 0.64\ V \times VPI - 0.135\ V$. The VICM pin can be used as a reference common-mode voltage for driving a high impedance sensing node of the preceding cascaded part (VICM has a 7 kΩ impedance).

OUTPUT SIGNAL PATH

The low impedance (10 Ω) output buffers are designed to drive a high impedance load, such as an ADC input or another amplifier stage. The output pins—OPP1, OPM1, OPP2, and OPM2—sit at a nominal output common-mode voltage of VPS/2, but can be driven to a voltage of 0.9 V to 2.1 V by applying the desired common-mode voltage to the high impedance VOCM pin.

DC OFFSET COMPENSATION LOOP ENABLED

When the dc offset compensation loop is enabled via B1 of the SPI register, the ADRF6518 can null the output differential dc level. The loop is enabled by setting B1 = 0. The offset compensation loop creates a high-pass corner frequency, which is proportional to the value of the capacitors that are connected from the OFS1 and OFS2 pins to ground. For more information about setting the high-pass corner frequency, see the DC Offset Compensation Loop section.
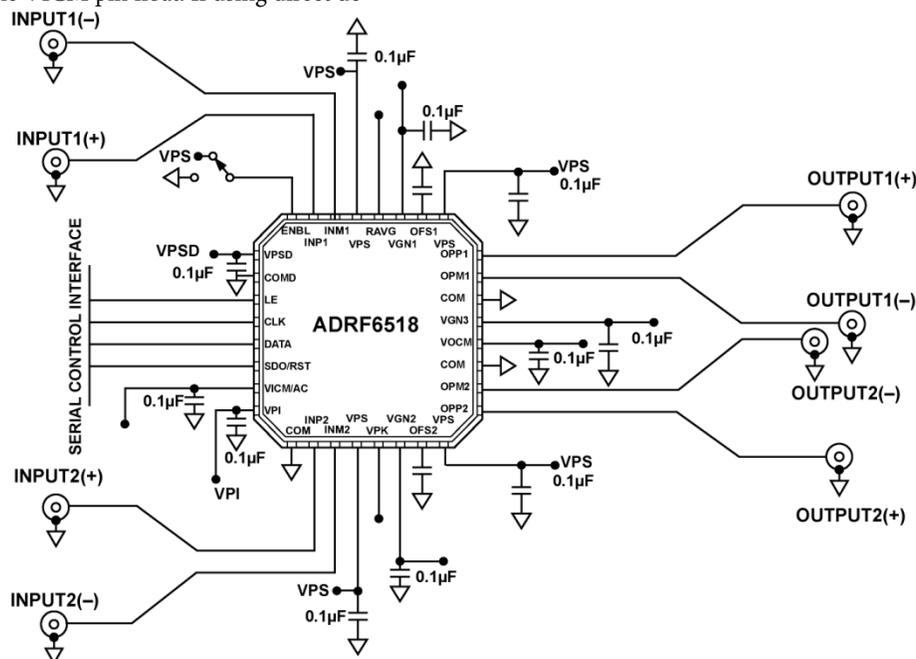

Figure 72. Basic Connections

COMMON-MODE BYPASSING

The ADRF6518 common-mode pins, VICM/AC and VOCM, must be decoupled to ground. At least one low inductance, surface-mount ceramic capacitor with a value of 0.1 µF must be used to decouple the common-mode pins.

SERIAL PORT CONNECTIONS

The ADRF6518 has a SPI port to control the gain and filter bandwidth settings. Data can be written to the internal 15-bit register and read from the register. It is recommended that low-pass RC filtering be placed on the SPI lines to filter out any high frequency glitches. See Figure 74, the evaluation board schematic, for an example of a low-pass RC filter.

ENABLE/DISABLE FUNCTION

To enable the ADRF6518, the ENBL pin must be pulled high. Driving the ENBL pin low disables the device, reducing current consumption to approximately 9 mA at room temperature.

GAIN PIN DECOUPLING

The ADRF6518 has three analog gain control pins: VGN1, VGN2, and VGN3. Use at least one low inductance, surface-mount ceramic capacitor with a value of 0.1 µF to decouple each gain control pin to ground.

PEAK DETECTOR CONNECTIONS

The ADRF6518 has peak detector output on the VPK pin, with a scaling of 1 V/V pk differential at filter inputs. The bigger peak of the two channels reported. The peak detector time-constant can be changed with a resistor from the RAVG pin to VPS. Leave the RAVG pin open for the longest time-constant (hold time). RAVG resistor range is ∞ to 1 kΩ.

To reset the peak detector, pull the SDO/RST pin high for 25 ns or longer. Logic levels are $V_{LOW} < 0.8$ V, $V_{HIGH} > 2$ V.

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

Error vector magnitude (EVM) is a measure used to quantify the performance of a digital radio transmitter or receiver by measuring the fidelity of the digital signal transmitted or received. Various imperfections in the link, such as magnitude and phase imbalance, noise, and distortion, cause the constellation points to deviate from their ideal locations.

In general, a receiver exhibits three distinct EVM limitations vs. received input signal power. As signal power increases, the distortion components increase.

- At large enough signal levels, where the distortion components due to the harmonic nonlinearities in the device are falling in-band, EVM degrades as signal levels increase.
- At medium signal levels, where the signal chain behaves in a linear manner and the signal is well above any notable noise contributions, EVM has a tendency to reach an optimal level determined dominantly by either the quadrature accuracy and IQ gain match of the signal chain or the precision of the test equipment.
- As signal levels decrease, such that noise is a major contributor, EVM performance vs. the signal level exhibits a decibel-for-decibel degradation with decreasing signal level. At these lower signal levels, where noise is the dominant limitation, decibel EVM is directly proportional to the SNR.

EVM TEST SETUP

The basic setup to test EVM for the ADRF6518 consisted of an Agilent MXG M5182B Vector Signal Generator used as a signal source and a Agilent DSO7104B oscilloscope used to sample the signal while connected to a computer running Agilent 89600 VSA software to calculate the EVM of the signal. The M5182B IQ baseband differential outputs drove the ADRF6518 inputs. The I and Q outputs of the ADRF6518 were loaded with 400 Ω differential impedances and connected differentially to two AD8130 differential amplifiers to convert the signals into single-ended signals. The single-ended signals were connected to the input channels of the VSA.

EVALUATION BOARD

An evaluation board is available for testing the ADRF6518.

EVALUATION BOARD CONTROL SOFTWARE

The ADRF6518 evaluation board is controlled through the parallel port on a PC. The parallel port is programmed via the ADRF6518 evaluation software. This software enables/disables the dc offset compensation loop and controls the filter corner frequency, the high and low power modes, and the minimum and maximum gains for each amplifier in the ADRF6518. For information about the register map, see Table 5. For information about SPI port timing and control, see Figure 2 and Figure 3.

After the software is downloaded and installed, start the basic user interface to program the filter corner and gain values (see Figure 73).

To program the filter corner, perform one of the following:

- Click the arrow in the **Frequency Corner MHz** section of the window, select the desired corner frequency from the menu, and click **Write Selected Cutoff Frequency to Device**.
- Click **Frequency +1 MHz** or **Frequency −1 MHz** to increment or decrement the frequency corner in 1 MHz steps from the current frequency corner.

To program the filter mode, offset correction, and power mode, move the respective slider switch in the upper right corner of the window.

To program the maximum gains of VGA1, VGA2, VGA3, and the postamplifier, click the **VGA1 Gain dB**, **VGA2 Gain dB**, **VGA3 Gain dB**, and **Post Amp Gain dB** drop-down boxes and select the desired gain.

- The VGA1 maximum gain can be set to 9 dB, 12 dB, or 15 dB.
- The VGA2 and VGA3 maximum gain can be set to 12 dB, 15 dB, 18 dB, or 21 dB.
- The postamplifier maximum gain can be set to 3 dB or 9 dB.

When the user clicks the **Write Selected Cutoff Frequency to Device** button, a write operation is executed, immediately followed by a read operation. The updated information is displayed in the **VGA1 Gain dB**, **Filter Corner MHz**, **VGA2 Gain dB**, **VGA3 Gain dB**, and **Post Amp Gain dB** fields.
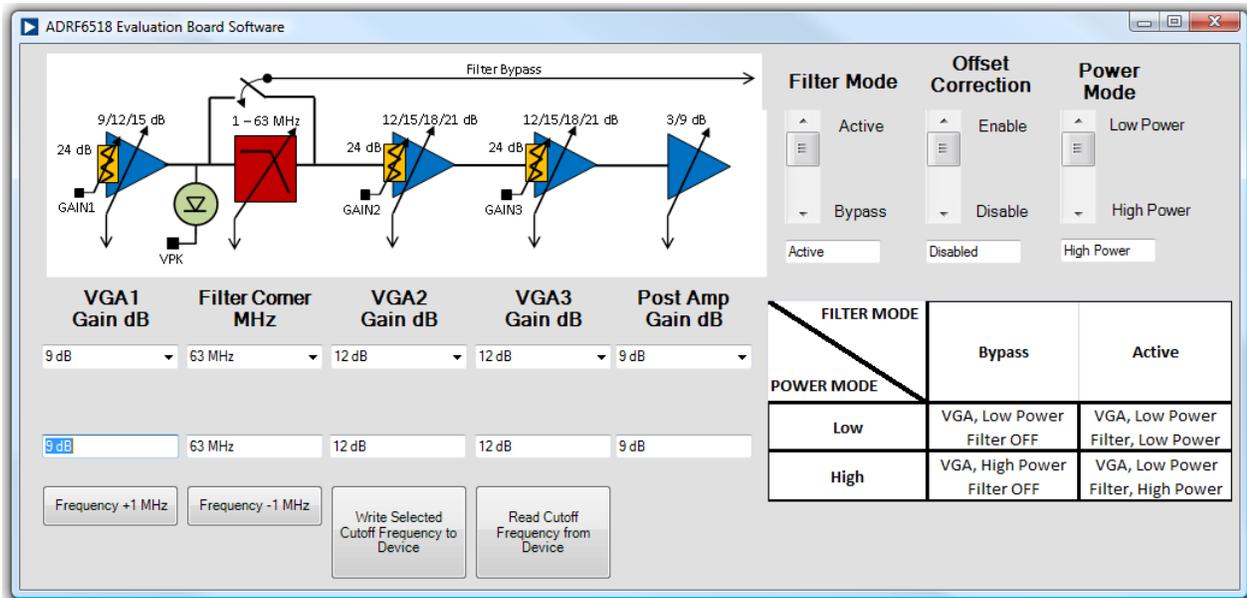

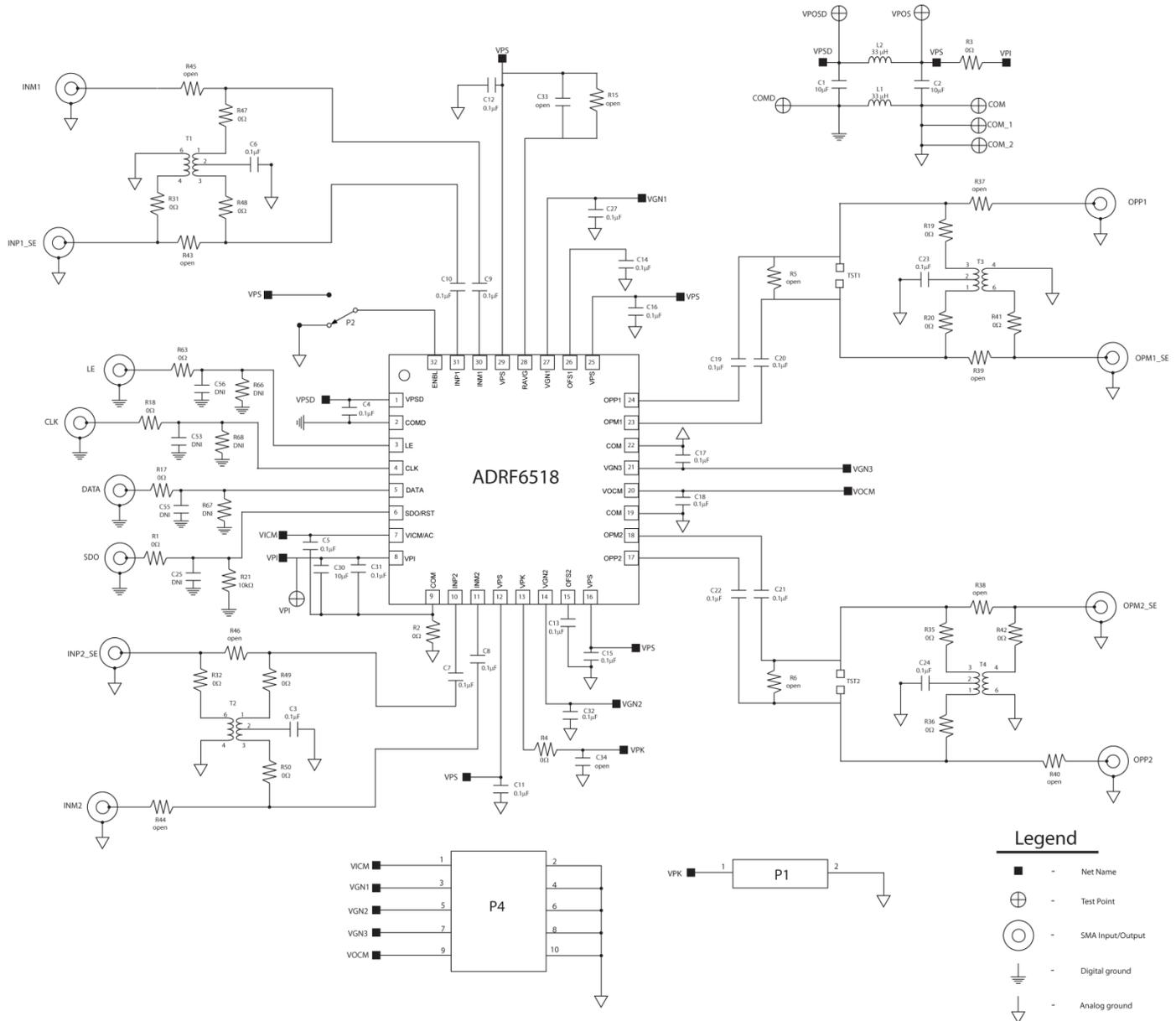Figure 73. Analog Devices ADRF6518 Evaluation Software

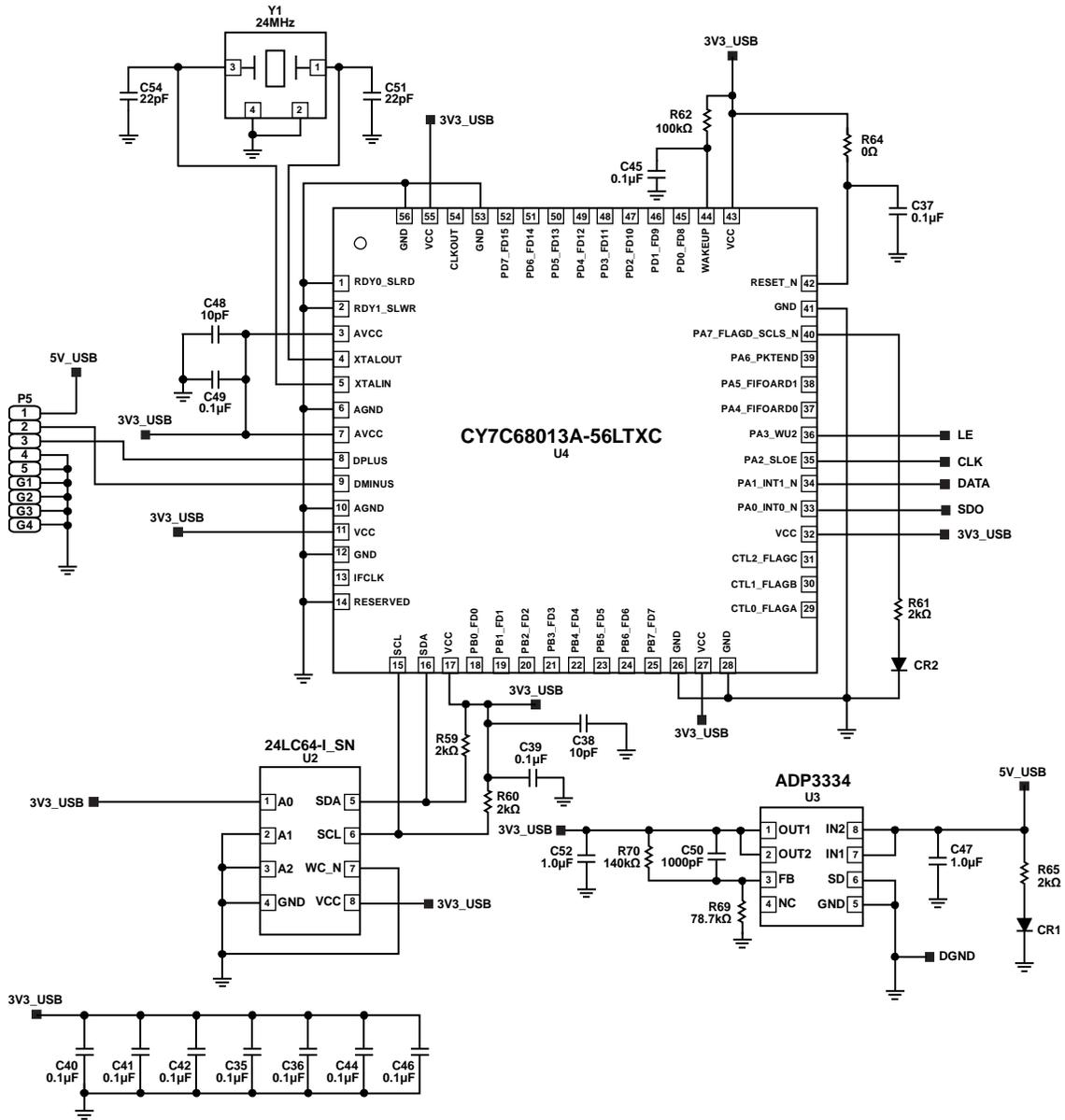## SCHEMATICS AND ARTWORK

Figure 74. Evaluation Board Schematic
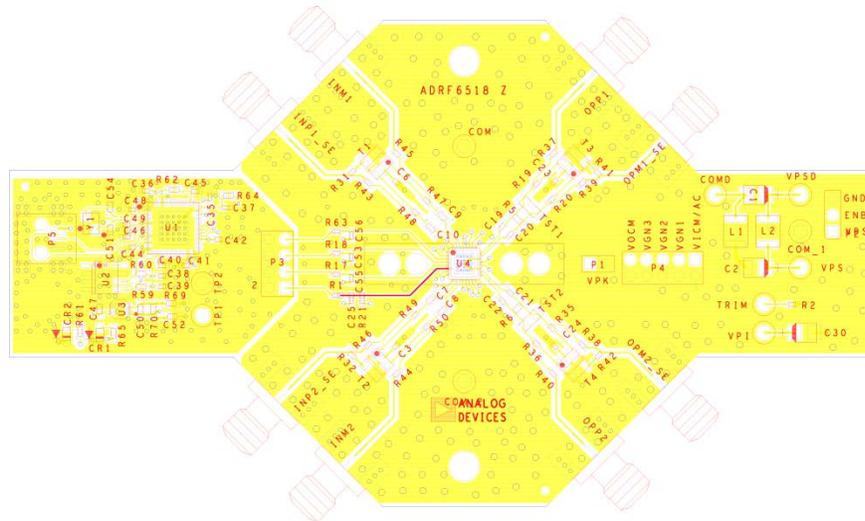
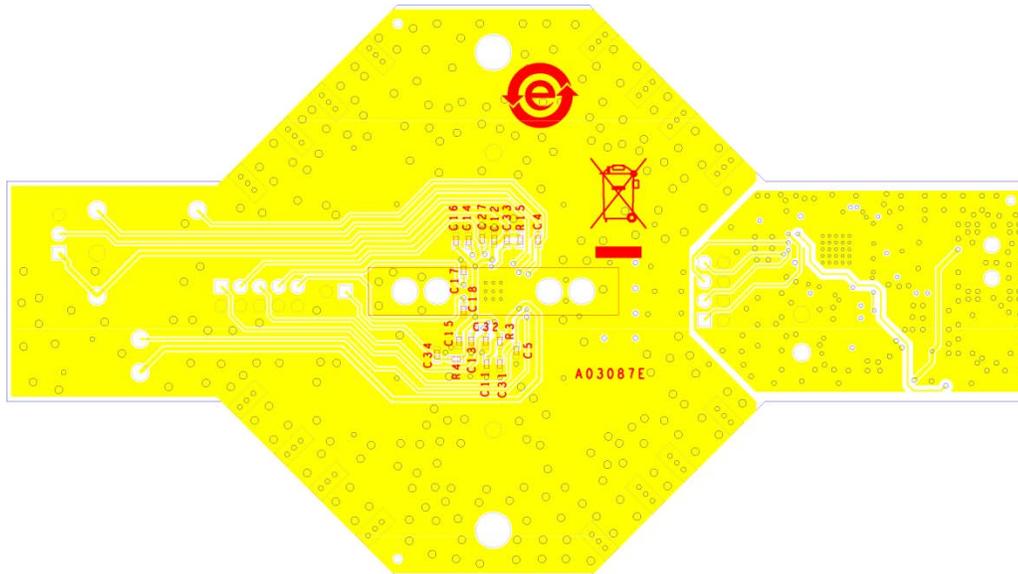*Figure 75. USB Evaluation Board Schematic*

Figure 76. Top Layer Silkscreen

Figure 77. Component Side Layout

Table 6. Evaluation Board Configuration Options

Components	Function	Default Conditions
C1, C2, C4, C11, C12, C15, C16, C30, C31, L1, L2, R2, R3, P4	Power supply and ground decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground.	C1, C2, C30 = 10 µF (Size 1210) C4, C11, C12, C15, C16, C31 = 0.1 µF (Size 0402) L1, L2 = 33 µH (Size 1812) R2, R3 = 0 Ω (Size 0402) P4 = installed
T1, T2, C3, C6, C7 to C10, R31, R32, R43, R44, R45, R46, R47, R48, R49, R50	Input interface. The INP1_SE, INM1, INP2_SE, and INM2 input SMAs are used to drive the part differentially by bypassing the baluns. Using only INP1_SE and INP2_SE in conjunction with the baluns enables single-ended operation. The default configuration of the evaluation board is for single-ended operation. T1 and T2 are 8:1 impedance ratio baluns that transform a single-ended signal in a 50 Ω system into a balanced differential signal in a 400 Ω system. R31, R32, R47, R48, R49, and R50 are populated for appropriate balun interface	T1, T2 = Pulse Electronics CX2049LNL C3, C6 = 0.1 µF (Size 0402) C7 to C10 = 0.1 µF (Size 0602) R31, R32, R47 to R50 = 0 Ω (Size 0402) R43 to R46 = open (Size 0402)

Components	Function	Default Conditions
	To bypass the T1 and T2 baluns for differential interfacing, remove the balun interfacing resistors, R31, R32, R47, R48, R49, and R50, and populate R43, R44, R45, and R46 with 0 Ω resistors.	
T3, T4, C19 to C24, R5, R6 R19, R20, R35 to R42	Output interface. The OPP1, OPM1_SE, OPP2, and OPM2_SE output SMAs are used to obtain differential signals from the part when the output baluns are bypassed. Using OPM1_SE, OPM2_SE, and the baluns, the user can obtain single-ended output signals. The default configuration of the evaluation board is for single-ended operation. T3 and T4 are 8:1 impedance ratio baluns that transform a differential signal in a 400 Ω system into a single-ended signal in a 50 Ω system. To bypass the T3 and T4 baluns for differential interfacing, remove the balun interfacing resistors, R19, R20, R35, R36, R41, and R42, and populate R37, R38, R39, and R40 with 0 Ω resistors. R5 and R6 can be populated with an impedance of at least 400 Ω to terminate the output in differential applications.	T3, T4 = Pulse Electronics CX2049LNL C19 to C24 = 0.1 µF (Size 0402) R5, R6 = open (size 0402) R19, R20, R35, R36, R41, R42 = 0 Ω (Size 0402) R37 to R40 = open (Size 0402)
P2	Enable interface. The ADRF6518 is powered up by applying a logic high voltage to the ENBL pin (Jumper P2 is connected to VPS).	P2 = installed for enable
P3, R1, R17, R18, R21, R63, C25, C53, C55, C56	Serial control interface. The digital interface sets the corner frequency, VGA1/VGA2/VGA3 maximum gains, and the postamplifier maximum gain using the serial interface via the LE, CLK, DATA, and SDO pins. RC filter networks can be populated on the CLK, LE, and DATA lines to filter the SPI signals. CLK, DATA, and LE signals can be observed via P3 for debug purposes. Setting C25, C53, and C56 = 330 pF is recommending for filtering.	P3 = installed R1 = 0 Ω (Size 0402) R21 = 10 kΩ (Size 0402) C25, C53, C55, C56 = open (Size 0402) R17, R18, R63 = 1 kΩ (Size 0402)
C13, C14	DC offset compensation loop. The dc offset compensation loop is enabled via the SPI port. When enabled, the C13 and C14 capacitors are connected to circuit common. The high-pass corner frequency is expressed as follows: f_{HP} (Hz) = 6.7 × (*Post Filter Linear Gain*/C_{OFS} (µF))	C13, C14 = 0.1 µF (Size 0402)
C5	Input common-mode reference. The input common-mode voltage can be monitored at the VICM pin. If the VICM pin is left open, an input common-mode voltage must be supplied externally (DC coupling mode). If VICM pin is connected to ground, the input common-mode defaults to VPI/2 (ac coupling mode).	C5 = 0.1 µF (Size 0402)
C18	Output common-mode setpoint. The output common-mode voltage can be set externally when applied to the VOCM pin. If the VOCM pin is left open, the output common-mode voltage defaults to VPS/2.	C18 = 0.1 µF (Size 0402)
C17, C27, C32	Analog gain control. The range of the analog gain pins, VGN1, VGN2, and VGN3, is from 0 V to 1 V, creating a gain scaling of 30 mV/dB.	C17, C27, C32 = 0.1 µF (Size 0402)
P1, R4, R15, C33, C34	Peak Detector.	P1 = installed R4 = 0 Ω (Size 0402) R15, C33, C34 = open (Size 0402)
U1, U2, U3, P5	Cypress Microcontroller, EEPROM, and LDO	U2 = Microchip MICRO24LC64 U3 = Analog Devices ADP3334ACPZ U4 = Cypress Semiconductor CY7C68013A-56LTXC P5 = Mini USB connector
C35, C36, C40, C41, C42, C44, C46	3.3 V supply decoupling. Several capacitors are used for decoupling on the 3.3 V supply.	C35, C36, C40, C41, C42, C44, C46 = 0.1 µF (0402)
C37, C38, C39, C45, C48, C49, R59, R60, R61, R62, R64, CR2	Cypress and EEPROM components.	C38, C48 = 10 pF (0402) C37, C39, C45, C49 = 0.1 µF (0402) R59, R60, R61 = 2 kΩ (0402) R62, R64 = 100 kΩ (0402) CR2 = ROHM SML-21OMTT86

Components	Function	Default Conditions
C47, C50, C52, R65, R69, R70, CR1	LDO components.	C47, C52 = 1 µF (0402) C50 = 1000 pF (0402) R65 = 2 kΩ (0402) R69 = 78.7 kΩ (0402) R70 = 140 kΩ (0402) CR1 = ROHM SML-21OMTT86
Y1, C51, C54	Crystal oscillator and components. 24 MHz crystal oscillator.	Y1 = NDK NX3225SA-24MHz C51, C54 = 22 pF (0402)

OUTLINE DIMENSIONS
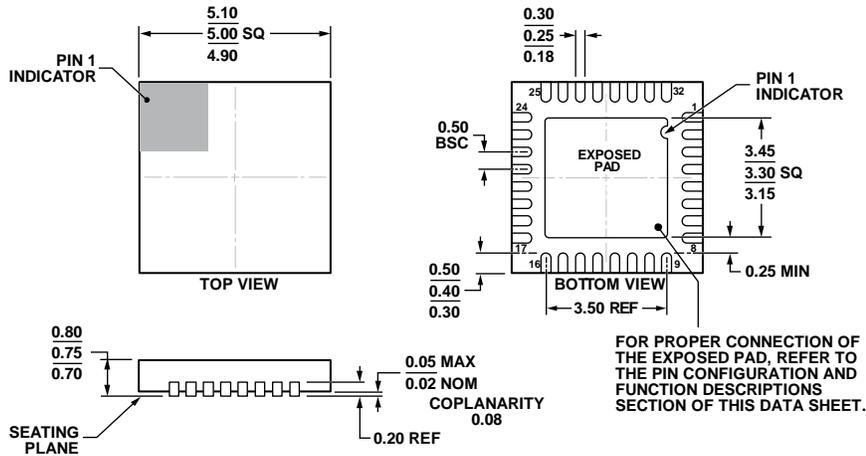
COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 78. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6518ACPZ-R7	−40°C to +85°C	32-Lead LFCSP_WQ, 7" Tape and Reel	CP-32-13
ADRF6518ACPZ-WP	−40°C to +85°C	32-Lead LFCSP_WQ, Waffle Pack	CP-32-13
ADRF6518-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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