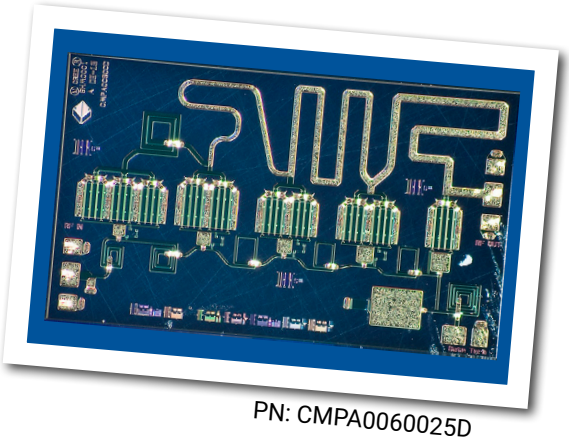
CMPA0060025D

25 W, 20 MHz - 6.0 GHz, GaN MMIC, Power Amplifier

Cree's CMPA0060025D is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC). GaN has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to Si and GaAs transistors. This MMIC enables very wide bandwidths.



PN: CMPA0060025D

Typical Performance Over 1.0-6.0 GHz (T_c = 25°C)

Parameter	1.0 GHz	2.0 GHz	3.0 GHz	4.0 GHz	5.0 GHz	6.0 GHz	Units
Gain	18.0	18.0	18.5	18.0	17.0	17.0	dB
Output Power @ P_{IN} 32 dBm	34	38	42	29	30	31	W
Associated Gain @ P_{IN} 32 dBm	13.3	13.9	14.2	12.6	13.1	12.9	dB
PAE @ P_{IN} 32 dBm	54	45	46	33	34	33	%

Note: V_{DD} = 50 V, I_D = 500 mA

Features

- 18 dB Small Signal Gain
- 30 W Typical P_{SAT}
- Operation up to 50 V
- High Breakdown Voltage
- High Temperature Operation
- Size 0.157 x 0.094 x 0.004 inches

Applications

- Ultra Broadband Amplifiers
- Test Instrumentation
- EMC Amplifier Drivers

Rev 2.0 – May 201

Absolute Maximum Ratings (not simultaneous) at 25˚C

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	84	VDC	
Gate-source Voltage	V_{GS}	-10, +2	VDC	
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	12	mA	
Thermal Resistance, Junction to Case (packaged)[1]	$R_{\theta JC}$	2.32	˚C/W	85˚C
Thermal Resistance (die only) [1]	$R_{\theta JC}$	1.40	˚C/W	85˚C
Input Power[2]	P_{IN}	36	dBm	

Note[1] Eutectic die attach using 80/20 AuSn solder mounted to a 10 mil thick CuMo carrier.
Note[2] Limit for internal resistor only. Thermal dissipation may be exceeded at this level.

Electrical Characteristics (Frequency = 20 MHz to 6.0 GHz unless otherwise stated; T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics						
Gate Threshold Voltage[1]	$V_{(GS)TH}$	-3.8	-3.0	-2.7	V	V_{DS} = 20 V, ΔI_D = 6 mA
Gate Quiescent Voltage	$V_{(GS)Q}$	–	-2.7	–	VDC	V_{DD} = 50 V, I_{DQ} = 500 mA
Saturated Drain Current[2]	I_{DS}	–	12	–	A	V_{DS} = 12.0 V, V_{GS} = 2.0 V
RF Characteristics						
Small Signal Gain	S21	–	18	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA
Input Return Loss	S11	–	9	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA
Output Return Loss	S22	–	7	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA
Output Power, 1	P_{OUT1}	17	29	–	W	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 4.0 GHz
Output Power, 2	P_{OUT2}	23	30	–	W	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 5.0 GHz
Output Power, 3	P_{OUT3}	23	31	–	W	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 6.0 GHz
Power Added Efficiency, 1	PAE1	18	33	–	%	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 4.0 GHz
Power Added Efficiency, 2	PAE2	23	34	–	%	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 5.0 GHz
Power Added Efficiency, 3	PAE3	22	33	–	%	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm, Freq = 6.0 GHz
Power Gain	G_P	–	13	–	dB	V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm
Output Mismatch Stress	VSWR	–	–	5 : 1	Ψ	No damage at all phase angles, V_{DD} = 50 V, I_{DQ} = 500 mA, P_{IN} = 32 dBm

Notes:
[1] The device will draw approximately 55-70 mA at pinch off due to the internal circuit structure.
[2] Scaled from PCM data.
[3] All data pulsed with Pulse Width at 10µS, 1% Duty Cycle
[3] Data measured into a 15 dB output load with a maximum return loss.

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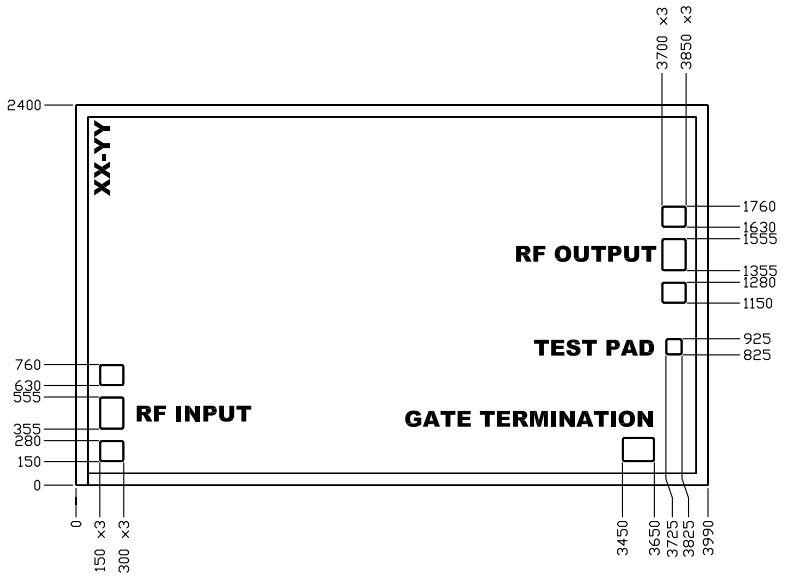
Die Dimensions (units in microns)



Overall die size 3990 x 2400 (+0/-50) microns, die thickness 100 (+/-10) micron.
All Gate and Drain pads must be wire bonded for electrical connection.

Pad Number	Function	Description	Pad Size (microns)
1	RF IN[1]	RF-Input pad. Matched to 50 ohm. Requires gate control from an external bias –T from -2.3 V to -3.8 V.	150 x 200
2	Gate Termination	Off Chip termination for the Gate. It needs to be DC-blocked .	200 x 150
3	RF OUT[1]	RF-Output pad. Matched to 50 ohm. Requires Drain supply from an external bias –T up to 50 V , 2.0 A	150 x 200

Notes:
[1] The RF In and Out pads have a ground-signal-ground configuration with a pitch of 75 microns.

Die Assembly Notes:

- Recommended solder is AuSn (80/20) solder. Refer to Cree's website for the Eutectic Die Bond Procedure application note at www.cree.com/RF/Document-Library
- Vacuum collet is the preferred method of pick-up.
- The backside of the die is the Source (ground) contact.
- Die back side gold plating is 5 microns thick minimum.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- Gold wire must be used for connections.
- Test pad must be bonded to Ground.
- Use the die label (XX-YY) for correct orientation.

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Functional Block Diagram

This device employs a wideband amplifier topology. It has an internal termination for the Gate, which works well over 1.0-6.0 GHz. For operation below 1.0 GHz an external termination is required. This termination needs to be DC-blocked and suitable to withstand up to 2 W of RF power. (Refer to the reference design section for the LF-termination in this data sheet for more details). The circuits also require external wideband Bias –T's to supply voltage to the Gate and Drain. The Bias-T at the Drain needs to be designed to handle 50 V and up to 2.0 A.

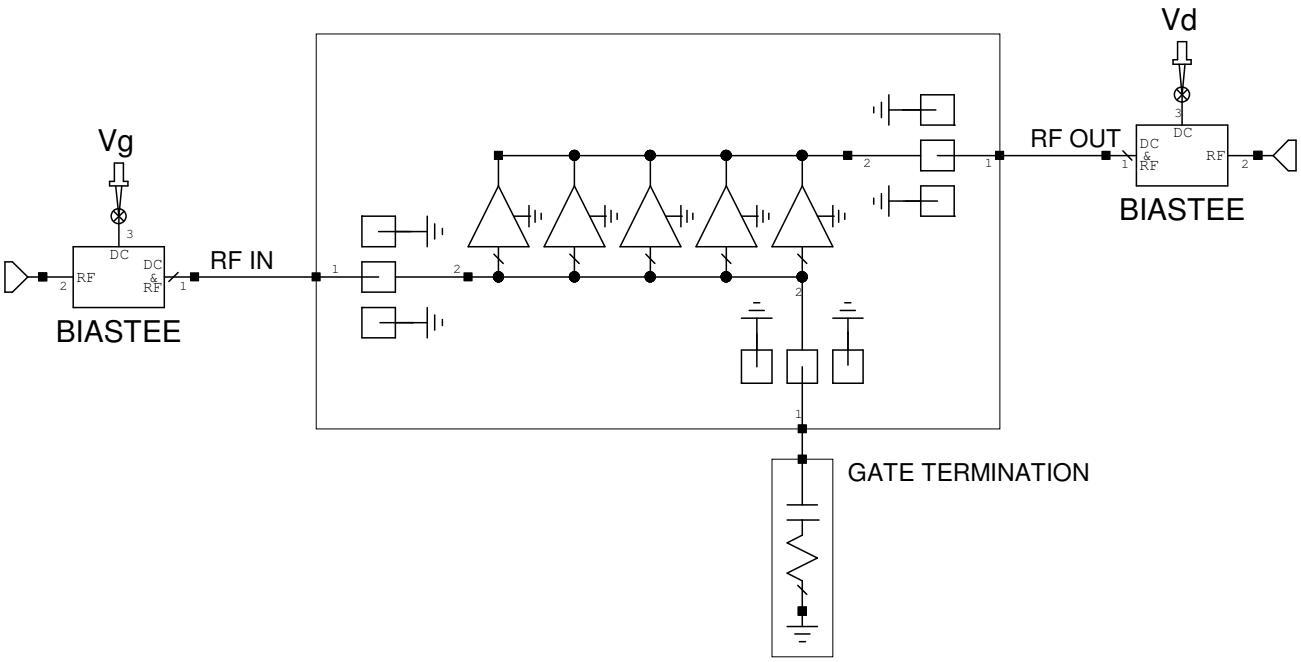

Figure 1.

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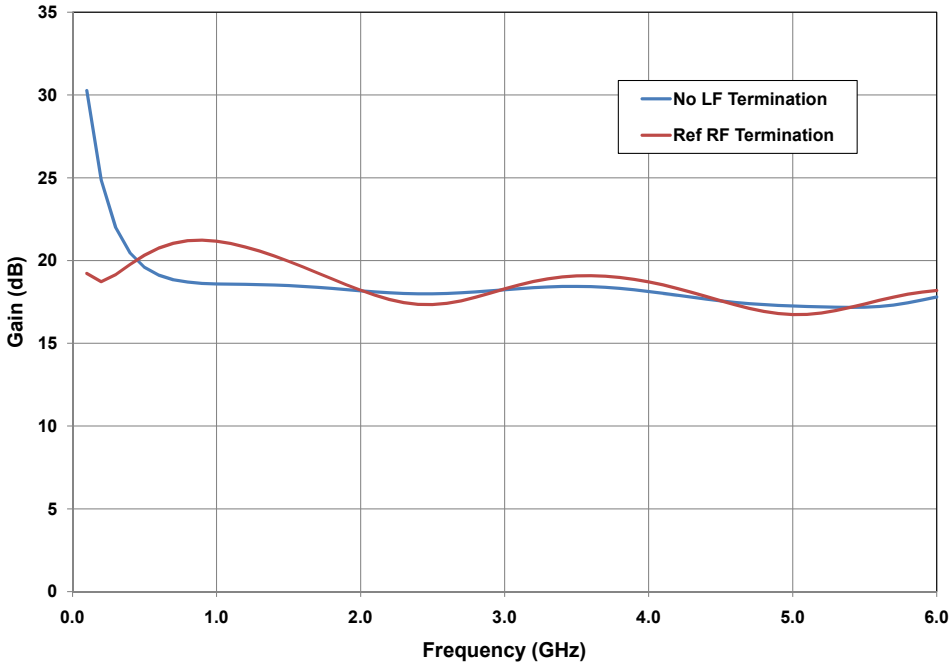
External Termination Reference Design

The following is a plot of the gain of the die with and without an RC reference circuit.



Notes:

[1] An off chip termination is needed to reduce the high gain peak at low frequencies.

[2] The off chip termination should be designed to minimize the impact on the MMIC's performance at higher frequencies.

RC Reference Circuit

The reference circuit is a series capacitor and resistor as shown below.

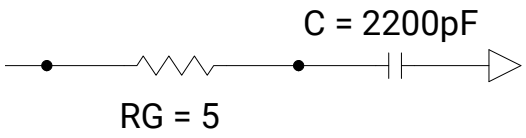


Figure 2.

The resistor needs to handle 2.0 W.

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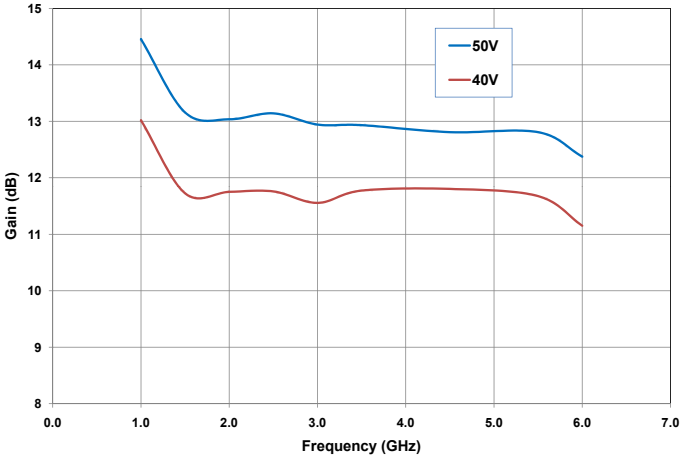
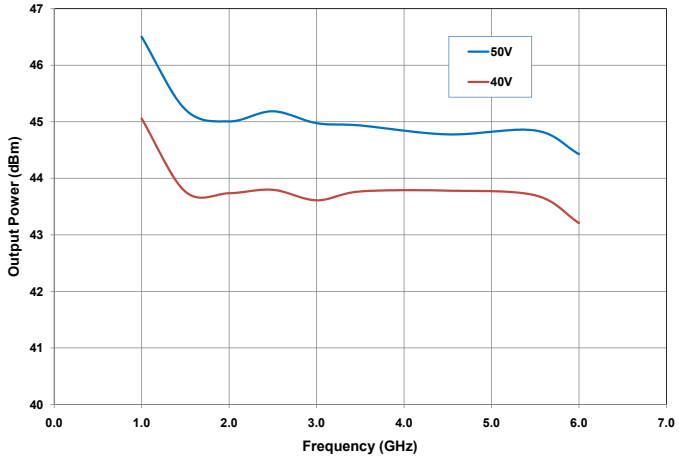
Typical Performance

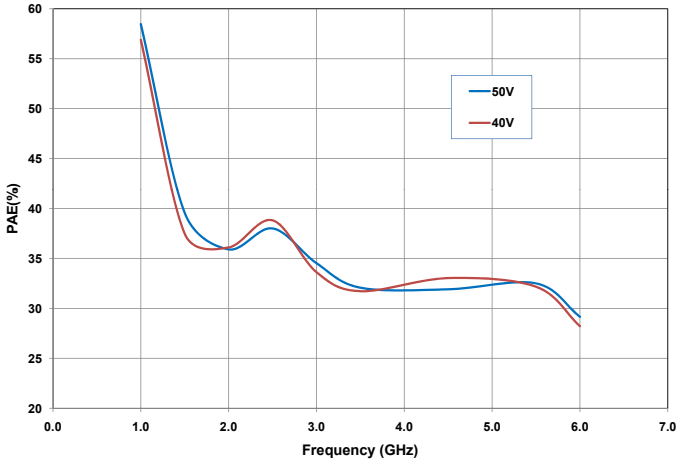
Power Gain vs Frequency
P_{IN} = 32 dBm



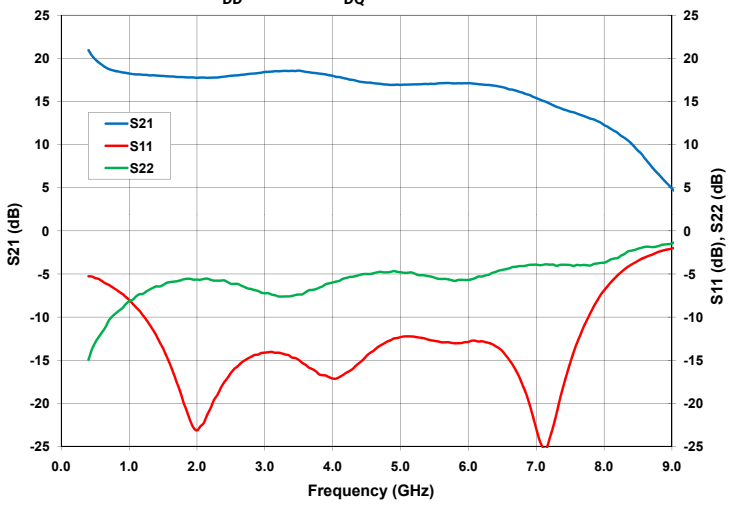
Power Output vs Frequency
P_{IN} = 32 dBm



Power Added Efficiency vs Frequency
P_{IN} = 32 dBm



Gain and Return Losses vs Frequency
V_{DD} = 50 V, I_{DQ} = 500 mA



Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Test Methodology
Human Body Model	HBM	1A (> 250 V)	JEDEC JESD22 A114-D
Charge Device Model	CDM	II (200 < 500 V)	JEDEC JESD22 C101-C

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Product Ordering Information

Order Number	Description	Unit of Measure
CMPA0060025D	GaN MMIC Power Amplifier Bare Die	Each

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