

**DATA SHEET**

# SKY65127-11: 700-800 MHz High Linearity, 2 W Power Amplifier

## Applications

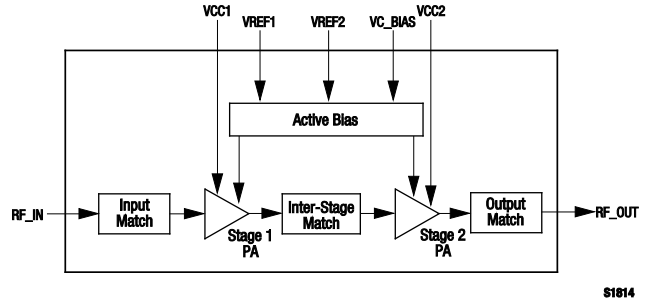
- WCDMA, CDMA, TDMA, GSM, LTE systems
- Repeaters
- WLL and ISM band transmitters
- Mobile radios
- Femtocell base stations

## Features

- High linearity: OIP3 > +47 dBm
- OP1dB = +32.5 dBm
- ACLR = -45 dBc for P<sub>OUT</sub> = +25 dBm
- High efficiency: PAE = 38%
- High gain = 36.5 dB
- Internal RF match and bias circuits
- Single DC supply: 5 V
- MCM (20-pin, 6 x 6 mm) package (MSL3, 260 °C per JEDEC J-STD-020)



Skyworks Pb-free products are compliant with all applicable legislation. For additional information, refer to *Skyworks Definition of Lead (Pb)-Free*, document number SQ04-0073.



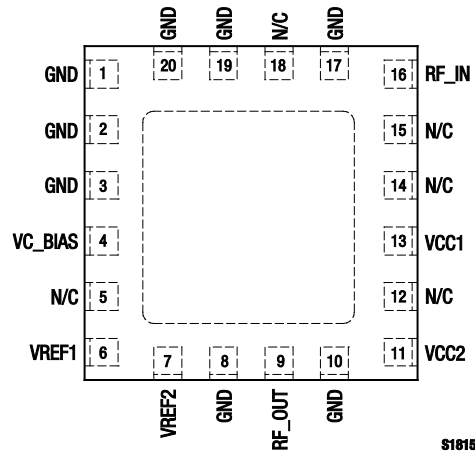
**Figure 1. SKY65127-11 Block Diagram**

## Description

Skyworks SKY65127-11 is a fully-matched, surface mount Power Amplifier (PA) designed for WCDMA, CDMA, TDMA, GSM, and LTE radio, repeaters, transmitters, mobile radios, and femtocell base station applications operating in the 700 to 800 MHz bandwidth.

All active circuitry in the module is contained in a single GaAs Microwave Monolithic Integrated Circuit (MMIC). The device is manufactured using Skyworks AlGaAs Heterojunction Bipolar Transistor (HBT) process, which allows for single supply operation while maintaining high efficiency and good linearity.

A block diagram of the SKY65127-11 is shown in Figure 1. The device package and pinout for the 20-pin MCM are shown in Figure 2.



**Figure 2. SKY65127-11 Pinout – 20-Pin MCM (Top View)**

**Table 1. SKY65127-11 Signal Descriptions**

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	11	VCC2	Stage 2 collector voltage
2	GND	Ground	12	N/C	No connection
3	GND	Ground	13	VCC1	Stage 1 collector voltage
4	VC_BIAS	Bias voltage	14	N/C	No connection
5	N/C	No connection	15	N/C	No connection
6	VREF1	Bias reference voltage 1	16	RF_IN	RF input
7	VREF2	Bias reference voltage 2	17	GND	Ground
8	GND	Ground	18	N/C	No connection
9	RF_OUT	RF output	19	GND	Ground
10	GND	Ground	20	GND	Ground

**Note:** The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

**Table 2. SKY65127-11 Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Units
RF input power	P <sub>IN</sub>		0	dBm
Supply voltage (VCC1, VCC2, VC_BIAS, VREF1, VREF2)	V <sub>CC</sub>		6	V
Operating temperature	T <sub>C</sub>	-40	+85	°C
Storage temperature	T <sub>ST</sub>	-55	+125	°C
Junction temperature	T <sub>J</sub>		+150	°C
Power dissipation	P <sub>D</sub>		3	W
Thermal resistance	Θ <sub>JC</sub>		17	°C/W

**Note:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

## Technical Description

The SKY65127-11 PA contains two amplifier stages. The matching circuits for the input stage, interstage, and output stage are contained within the device. An on-chip active bias circuit is included within the device for both input and output stages, which provides excellent gain tracking over temperature and voltage variations.

The SKY65127-11 is internally matched for optimum linearity and efficiency. The input and output stages are independently supplied using the VCC1 and VCC2 supply lines (pins 13 and 11, respectively). The bias reference voltages for stages 1 and 2 are supplied using common lines VREF1 and VREF2 (pins 6 and 7,

respectively). The DC control voltage that sets the bias to stages 1 and 2 is supplied by the VC\_BIAS signal (pin 4).

## Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY65127-11 are provided in Table 2. Recommended operating conditions are specified in Table 3 and electrical specifications are provided in Table 4.

Typical performance characteristics are shown in Figures 3 through 14.

**Table 3. SKY65127-11 Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage (VCC1, VCC2, VC_BIAS, VREF1, VREF2)	Vcc		5		V
Operating frequency	f	730		770	MHz
Operating temperature	Tc	-40	+25	+85	°C

**Table 4. SKY65127-11 Electrical Specifications (Note 1)****(VCC1 = VCC2 = VREF1 = VREF2 = VC\_BIAS = 5 V, f = 750 MHz, Tc = +25 °C, Unless Otherwise Noted)**

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Frequency	f		730		770	MHz
Small signal gain	IS21I	P <sub>IN</sub> = -15 dBm	35.0	36.5		dB
Input return loss	IS11I	P <sub>IN</sub> = -15 dBm	8.5	9.6		dB
Output return loss	IS22I	P <sub>IN</sub> = -15 dBm	9	12		dB
1 dB Output Compression Point	OP1dB	CW		+32.5		dBm
3 <sup>rd</sup> Order Output Intercept Point	OIP3	P <sub>OUT</sub> /tone = +25 dBm, tone spacing = 1 MHz	+47	+48		dBm
Noise Figure	NF	CW		4.4	6.0	dB
Adjacent Channel Leakage Ratio @ P <sub>OUT</sub> = +25 dBm	ACLR1	WCDMA test model #1: 64 DPCH, 5 MHz offset		-46.0	-45.0	dBc
Adjacent Channel Leakage Ratio @ P <sub>OUT</sub> = +25 dBm	ACLR2	WCDMA test model #1: 64 DPCH, 10 MHz offset		-63.5	-55.0	dBc
Power Added Efficiency	PAE	CW, P <sub>OUT</sub> @ OP1dB	35	38		%
Quiescent Current	I <sub>CCQ</sub>	No RF signal		270		mA

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Typical Performance Characteristics**

(VCC1 = VCC2 = VREF1 = VREF2 = VC\_BIAS = 5 V, f = 750 MHz, Tc = +25 °C, Unless Otherwise Noted)

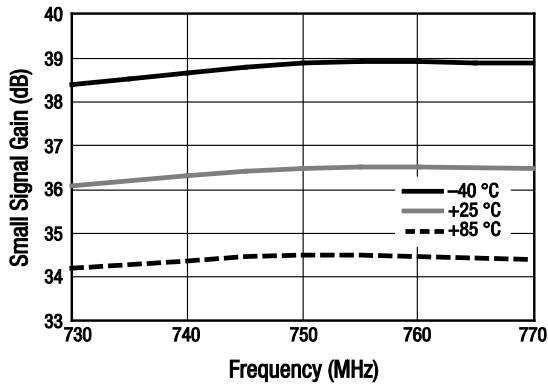


Figure 3. Small Signal Gain vs Frequency Over Temperature

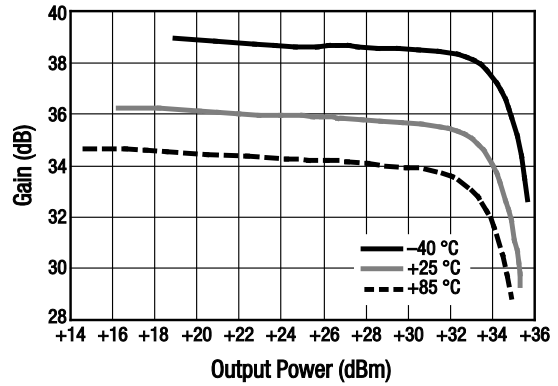


Figure 4. Gain vs Output Power Over Temperature (f = 750 MHz)

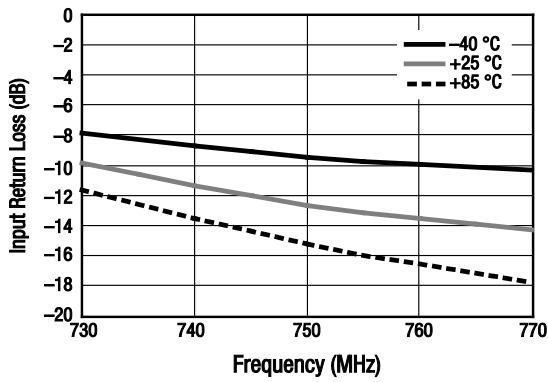


Figure 5. Input Return Loss vs Frequency Over Temperature

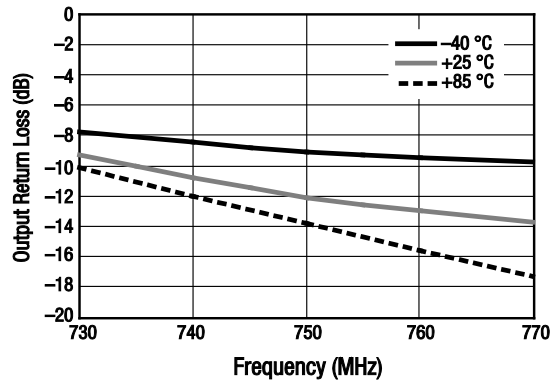


Figure 6. Output Return Loss vs Frequency Over Temperature

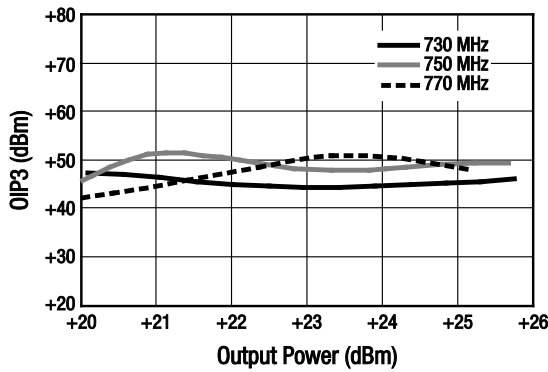


Figure 7. OIP3 vs Output Power Over Frequency (Δf = 1 MHz Spacing)

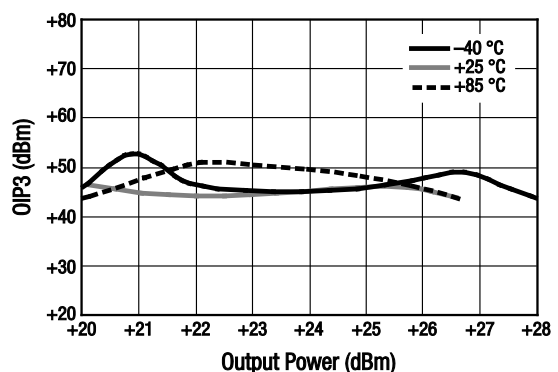
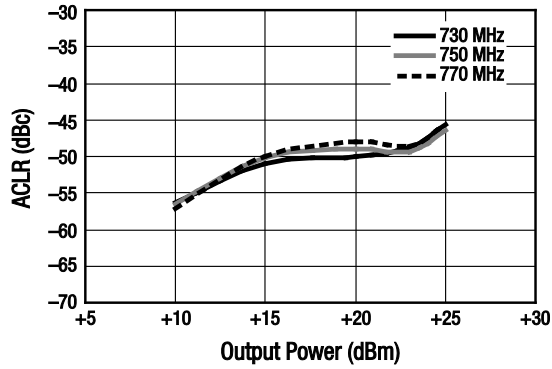
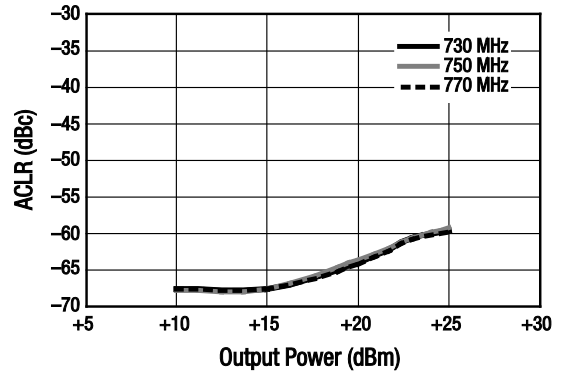


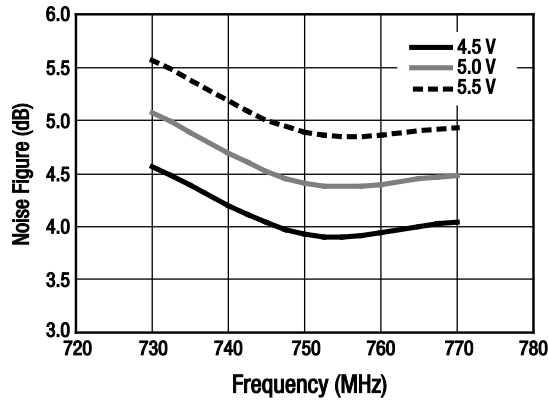
Figure 8. OIP3 vs Output Power Over Temperature (Δf = 1 MHz Spacing)



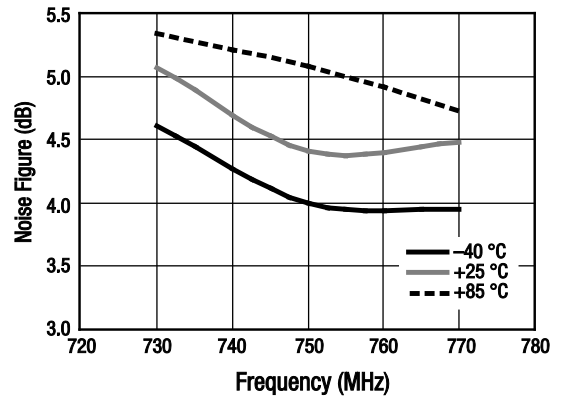
**Figure 9. ACLR vs Output Power Over Frequency (WCDMA Test Model 1 w/64 DPCH @ 5 MHz Offset)**



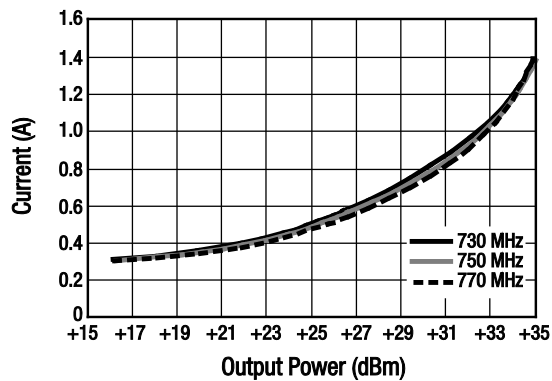
**Figure 10. ACLR vs Output power Over Frequency (WCDMA Test Model 1 w/64 DPCH @ 10 MHz Offset)**



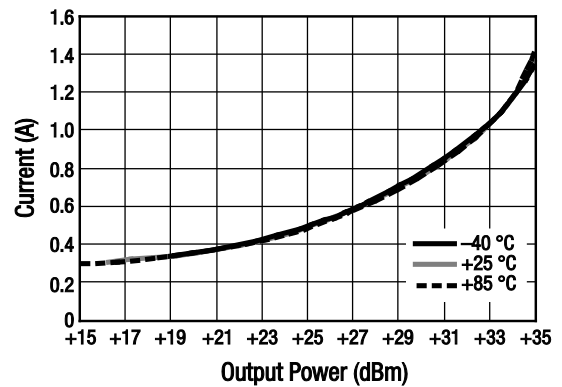
**Figure 11. Noise Filter vs Frequency Over Voltage**



**Figure 12. Noise Figure vs Frequency Over Temperature**



**Figure 13. Current vs Output Power Over Frequency**



**Figure 14. Current vs Output Power Over Temperature**

### Evaluation Board Description

The SKY65127-11 Evaluation Board is used to test the performance of the SKY65127-11 PA. An Evaluation Board schematic diagram is provided in Figure 15. Table 5 provides the Bill of Materials (BOM) list for Evaluation Board components.

An assembly drawing for the Evaluation Board is shown in Figure 16. An Evaluation Board layer detail drawing is shown in Figure 17. Layer detail physical characteristics are noted in Figure 18.

### Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

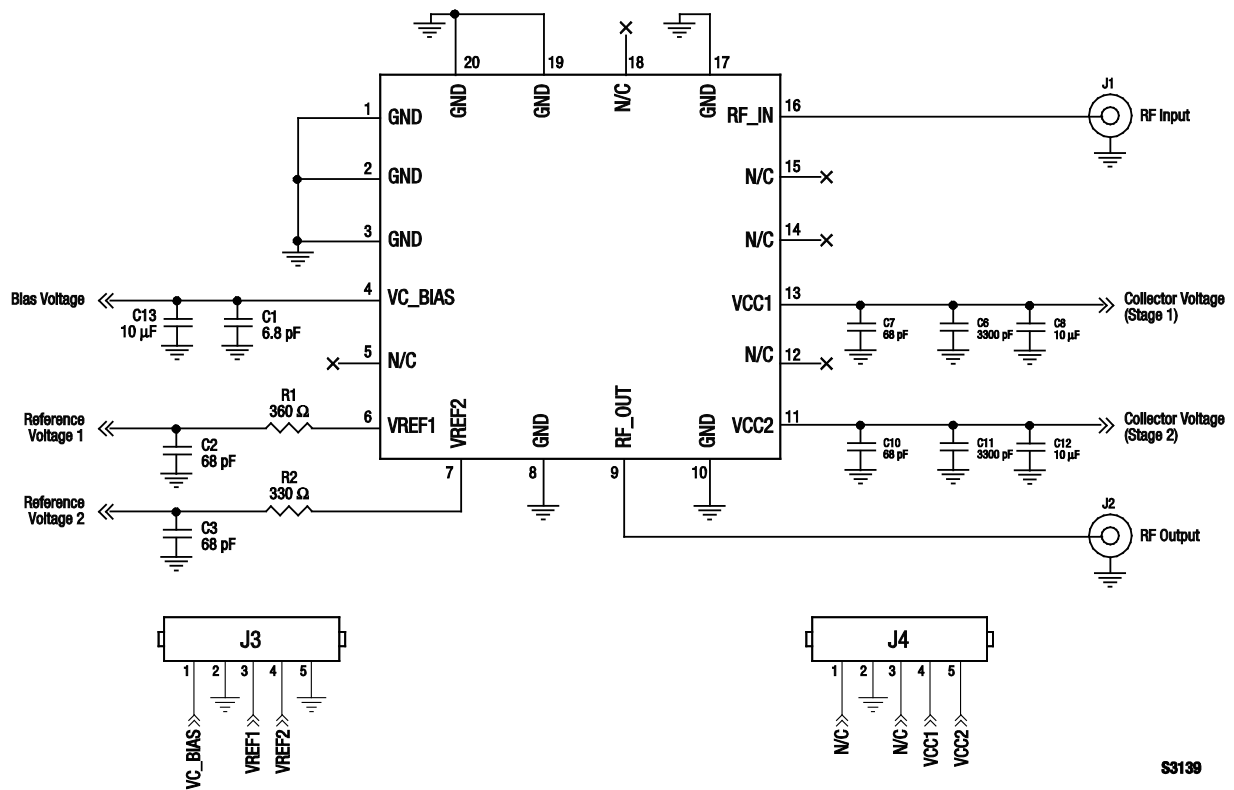
1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY65127-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

**NOTE:** A poor connection between the slug and ground increases junction temperature ( $T_J$ ), which reduces the lifetime of the device.

### Evaluation Board Test Procedure

- Step 1: Connect RF test equipment to the input/output SMA connectors.
- Step 2: Connect DC ground.
- Step 3: Connect all VCC, VREF, and VC\_BIAS lines to a +5 V supply. Verify that the  $I_{CCQ}$  current is approximately 270 mA.
- Step 4: Apply RF signal data at -20 dBm and observe that the output level is approximately +16.5 dBm or that the gain of the device is approximately 36.5 dB.

**NOTE:** It is important to adjust the VCC1 and VCC2 voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

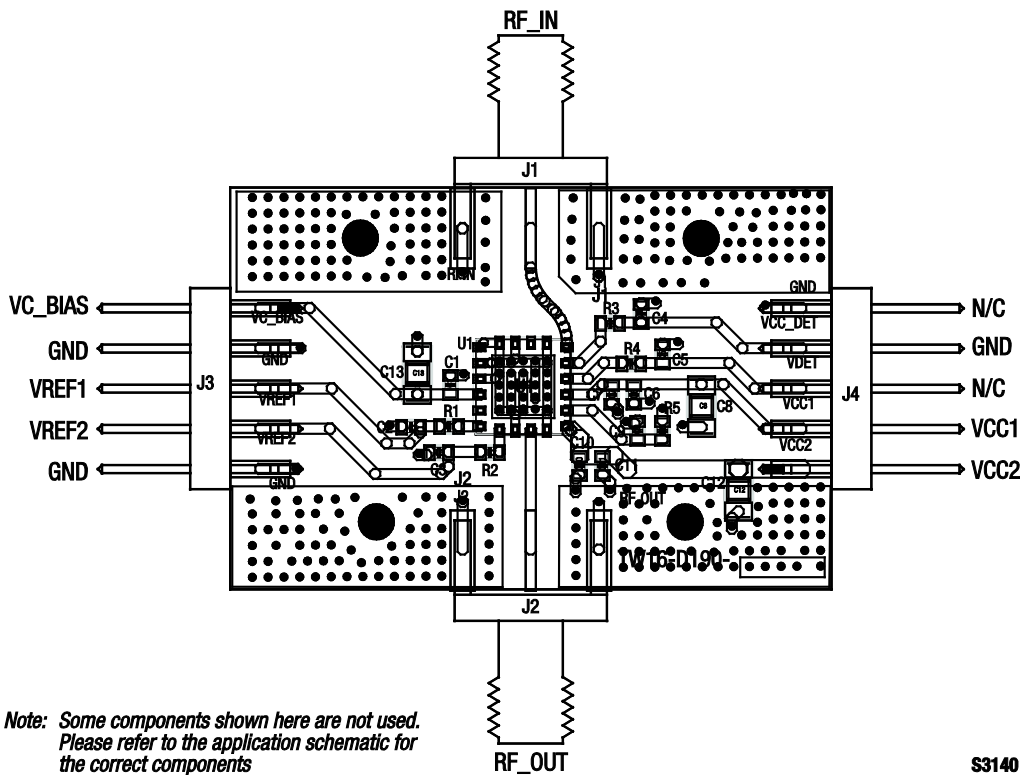


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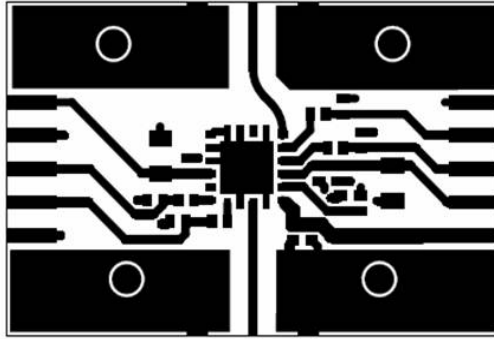
Figure 15. SKY65127-11 Evaluation Board Schematic

**Table 5. SKY65127-11 Evaluation Board Bill of Materials (BOM)**

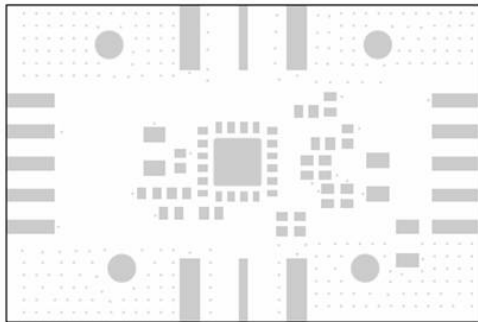
Component	Value	Size	Product #	Manufacturer	Manufacturer's Part #	Characteristics
C1, C6, C11	3300 pF	0603	SK204-000-007	Murata	GRM188R71H332KA01D	X7R, 50 V, ±10%
C2, C3, C7, C10	68 pF	0603	540R23-023	Murata	GRM1885C1H680JA01D	COG, 50 V, ±5%
C8, C12, C13	10 μF	1206	5404R91-005	TDK	C3216X5R0J106KT	X5R, 6 V, ±10%
R1	360 Ω	0603	5424R20-038	Rohm	MCR03EZHUJ360	50 V, 0.063 W, ±5%
R2	330 Ω	0603	5424R20-037	Rohm	MCR03EZHUJ330	50 V, 0.063 W, ±5%



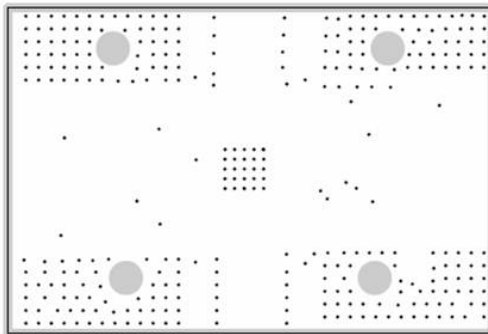
**Figure 16. Evaluation Board Assembly Drawing**



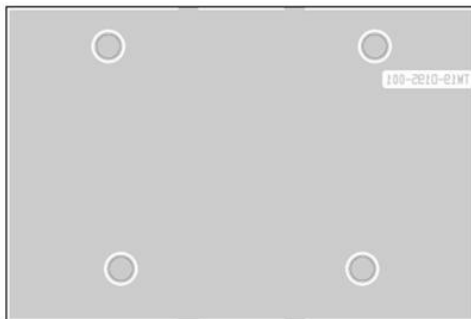
Layer 1: Top Metal



Layer 2: Solder Mask



Layer 3: Ground





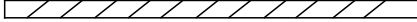

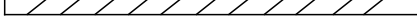


Layer 4: Solid Ground Plane

S3141

Figure 17. Evaluation Board Layer Detail



Cross Section	Name	Thickness (mils)	Material	$\epsilon_r$
	L1	1.4	Cu, 1 oz.	–
	Lam1	12	Rogers 4003-12	3.38
	L2	1.4	Cu, 1 oz.	–
	Lam2	4	FR4-4	4.35
	L3	1.4	Cu, 1 oz.	–
	Lam3	12	FR4-12	4.35
	L4	1.4	Cu, 1 oz.	–

9573

Figure 18. Layer Detail Physical Characteristics

### Application Circuit Notes

**Center Ground.** It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

**GND (pins 1, 2, 3, 8, 10, 17, 19, and 20).** Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.

**N/C (pins 5, 12, 14, 15, and 18).** These pins are open and may or may not be connected to ground.

**VC\_BIAS (pin 4).** The bias supply voltage for stages 1 and 2, typically set to +5 V.

**VREF1 (pin 6).** Bias reference voltage for amplifier stage 1. This signal should be operated over the same voltage range as VCC with a nominal voltage of +5 V.

**VREF2 (pin 7).** Bias reference voltage for amplifier stage 2. This signal should be operated over the same voltage range as VCC with a nominal voltage of +5 V.

**RF\_OUT (pin 9).** Amplifier RF output pin ( $Z_0 = 50 \Omega$ ). The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

**VCC2 (pin 11).** Supply voltage for the output (final) stage collector bias (typically +5 V). To bypass VCC2, capacitors C10, C11, and C12 (see Figure 15) should be placed in the approximate location shown on the Evaluation Board, although exact placement is not critical.

**VCC1 (pin 13).** Supply voltage for the first stage collector bias (typically +5 V). To bypass VCC1, capacitors C6, C7, and C8 (see

Figure 15) should be placed in the approximate location shown on the Evaluation Board, although exact placement is not critical.

**RF\_IN (pin 16).** Amplifier RF input pin ( $Z_0 = 50 \Omega$ ). The module includes an onboard internal DC blocking capacitor. All impedance matching is provided internal to the module.

### Package Dimensions

The PCB layout footprint for the SKY65152-11 is shown in Figure 35. Typical case markings are shown in Figure 36. Package dimensions for the 20-pin MCM are shown in Figure 37, and tape and reel dimensions are provided in Figure 38.

### Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY65127-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 250 °C. It can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

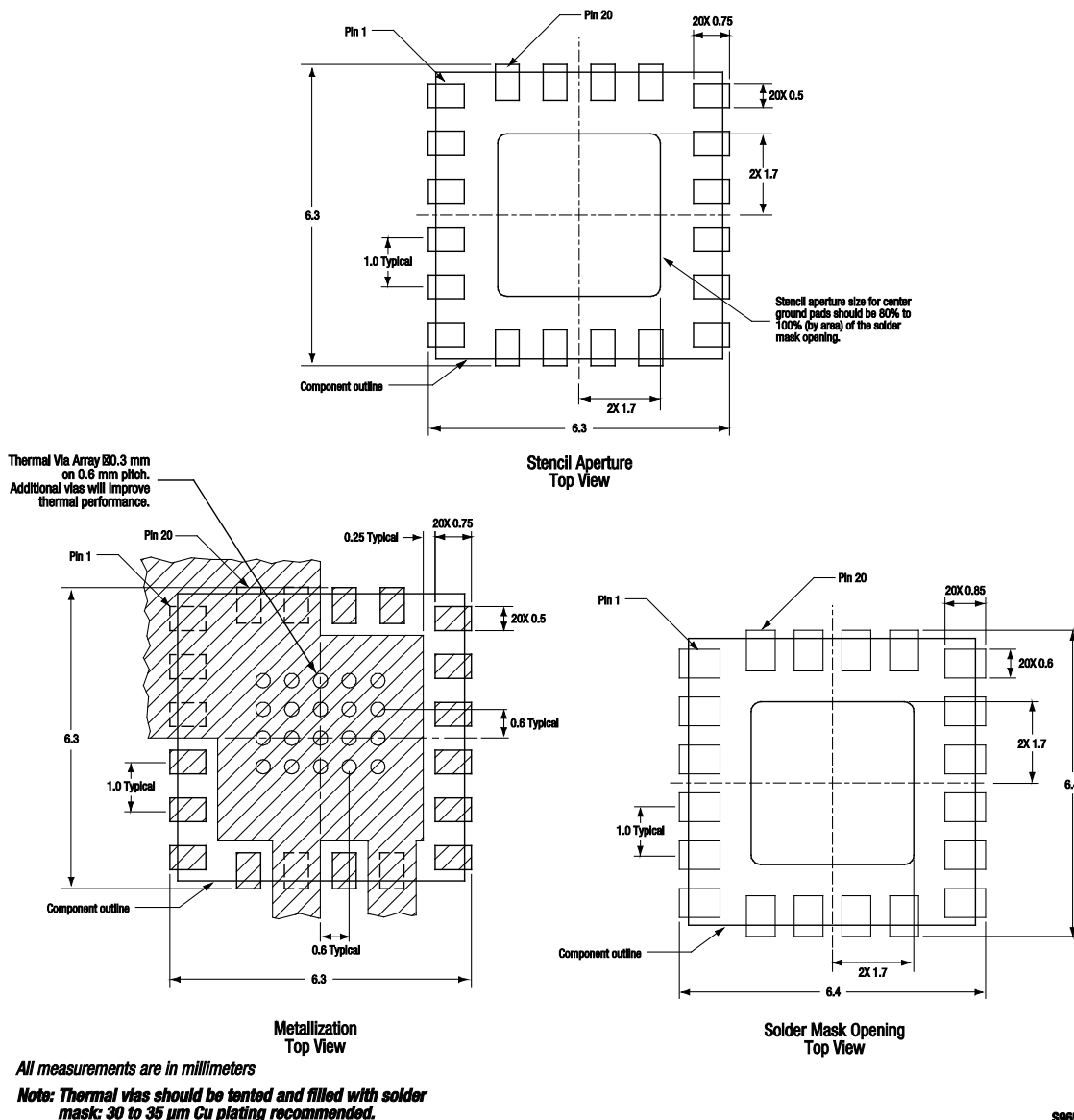


Figure 19. SKY65127-11 PCB Layout Footprint

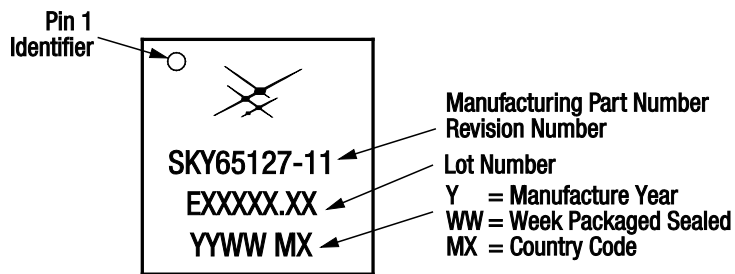


Figure 20. SKY65127-11 Typical Case Markings

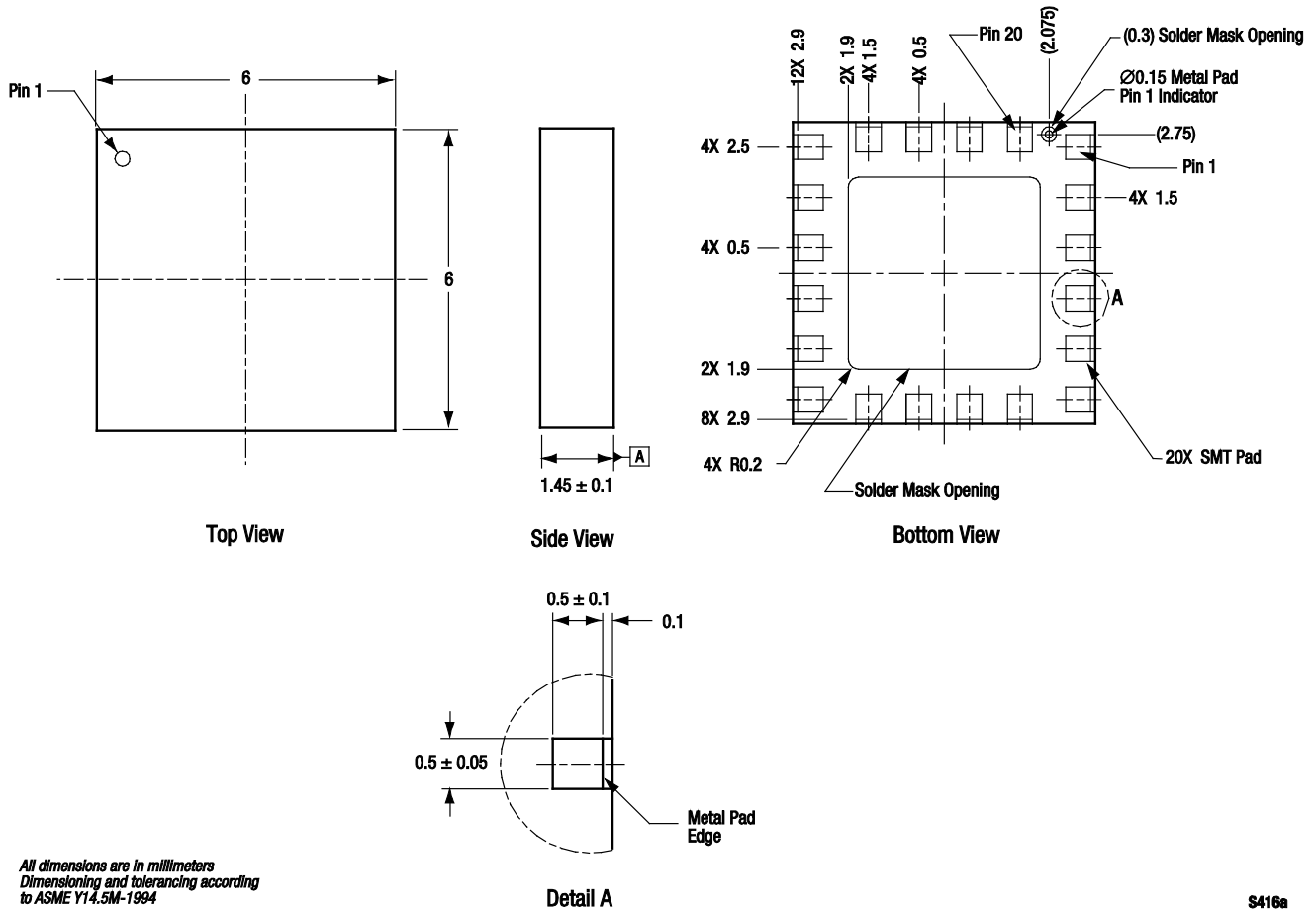
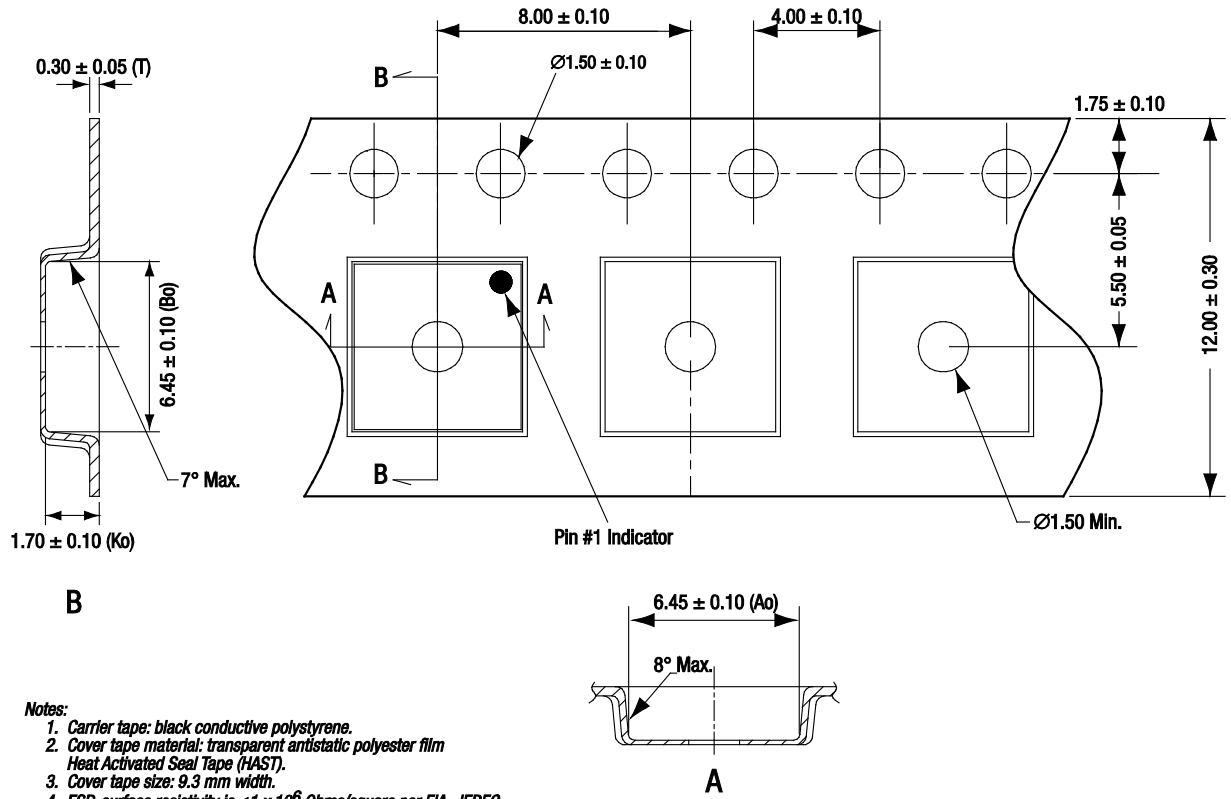


Figure 21. SKY65127-11 20-Pin MCM Package Dimensions



- Notes:**
1. Carrier tape: black conductive polystyrene.
  2. Cover tape material: transparent antistatic polyester film Heat Activated Seal Tape (HAST).
  3. Cover tape size: 9.3 mm width.
  4. ESD-surface resistivity is  $\leq 1 \times 10^6$  Ohms/square per EIA, JEDEC TNR Specification.
  5. All dimensions are in millimeters.

S3146

Figure 22. SKY65127-11 20-Pin MCM Tape and Reel Dimensions

**Ordering Information**

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY65127-11 700-800 MHz High Linearity Power Amplifier	SKY65127-11	TW17-D510-001

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