

ADSxx50 双路，750kSPS，16，14 和 12 位，同步采样， 模数转换器

1 特性

- 16、14 和 12 位引脚兼容系列
- 两个通道同时采样
- 伪差分模拟输入
- 快速数据吞吐量：750kSPS
- 出色的直流性能：
 - 线性：
 - ADS8350：16 位丢码率 (NMC) 差分非线性 (DNL)， ± 2.5 最低有效位 (LSB)，最大积分非线性 (INL)
 - ADS7850：14 位 NMC DNL， ± 1.5 LSB，最大 INL
 - ADS7250：12 位 NMC DNL， ± 1 LSB，最大 INL
- 出色的交流性能：
 - ADS8350：85dB 信噪比 (SNR)，-96dB 总谐波失真 (THD)
 - ADS7850：81dB SNR，-90dB THD
 - ADS7250：73dB SNR，-88dB THD
- 简单串行接口
- 在 -40°C 至 $+125^{\circ}\text{C}$ 的扩展工业用温度范围内完全额定运行
- 小型封装：超薄四方扁平无引线 (WQFN)-16 (3mm x 3mm)

2 应用范围

- 电机控制：使用 SinCos 编码器进行位置测量
- 光网络互连：掺铒光纤放大器 (EDFA) 增益控制环路
- 保护中继器
- 电源质量测量
- 三相电源控制
- 可编程逻辑控制器
- 工业自动化

3 说明

ADS8350、ADS7850 和 ADS7250 器件属于引脚兼容型双路高速同步采样模数转换器 (ADC) 产品系列，它们均支持伪差分模拟输入。所有器件支持一个由宽电源电压范围供电运行的简单串行接口，从而实现与多种主机控制器的轻松通信。

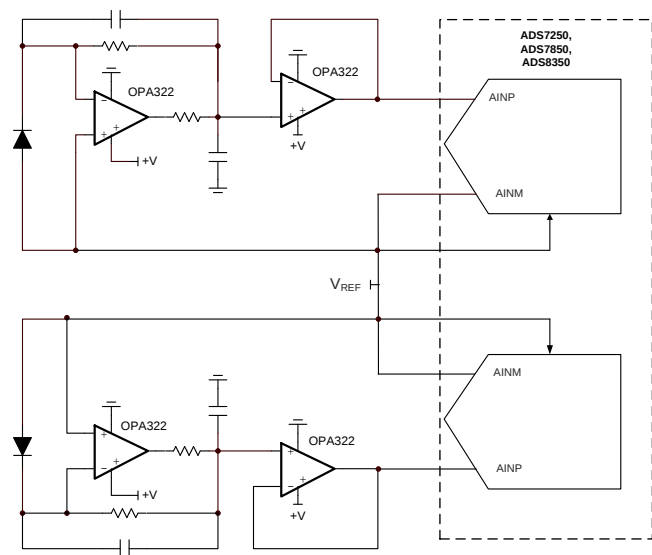
所有器件的额定扩展工业范围均为 -40°C 至 125°C ，并且采用引脚兼容 WQFN-16 (3mm x 3mm) 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
ADS7250	WQFN (16)	3.00mm x 3.00mm
ADS7850		
ADS8350		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能方框图



目录

1	特性	1	7.1	Overview	20
2	应用范围	1	7.2	Functional Block Diagram	20
3	说明	1	7.3	Feature Description	21
4	修订历史记录	2	7.4	Device Functional Modes	24
5	Pin Configuration and Functions	3	8	Application and Implementation	26
6	Specifications	4	8.1	Application Information	26
6.1	Absolute Maximum Ratings	4	8.2	Typical Applications	26
6.2	ESD Ratings	4	9	Power Supply Recommendations	33
6.3	Recommended Operating Conditions	4	10	Layout	34
6.4	Thermal Information	4	10.1	Layout Guidelines	34
6.5	Electrical Characteristics: All Devices	5	10.2	Layout Example	34
6.6	Electrical Characteristics: ADS7250	6	11	器件和文档支持	35
6.7	Electrical Characteristics: ADS7850	7	11.1	文档支持	35
6.8	Electrical Characteristics: ADS8350	8	11.2	相关链接	35
6.9	Timing Requirements	9	11.3	接收文档更新通知	35
6.10	Switching Characteristics	9	11.4	社区资源	35
6.11	Typical Characteristics: ADS7250	10	11.5	商标	35
6.12	Typical Characteristics: ADS7850	13	11.6	静电放电警告	35
6.13	Typical Characteristics: ADS8350	16	11.7	Glossary	35
6.14	Typical Characteristics: All Devices	19	12	机械、封装和可订购信息	35
7	Detailed Description	20			

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

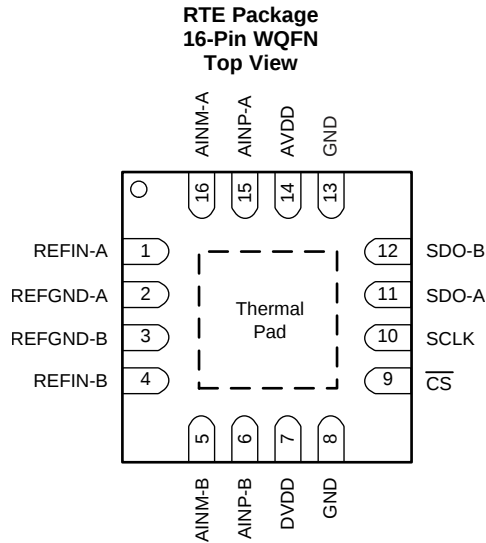
Changes from Revision C (June 2014) to Revision D	Page
• Changed <i>ESD Ratings</i> title, updated to current format, moved <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table	4
• Changed <i>Timing Characteristics</i> table: split table into <i>Timing Requirements</i> and <i>Switching Characteristics</i>	9
• Deleted t_{SU_DOCK} and t_{HT_CKDO} parameters, replaced with t_{D_CKDO} parameter	9
• Changed <i>Timing Diagram</i> figure	9

Changes from Revision B (April 2014) to Revision C	Page
• 已将器件信息表更改为最新标准	1
• 已更正功能方框图中的伪差分输入和参考连接	1
• Changed Handling Ratings table to current standards	4

Changes from Revision A (January 2014) to Revision B	Page
• 更改了格式，以符合最新数据表标准；添加了布局部分，移动了现有部分	1
• Deleted Ordering Information section	3

Changes from Original (May 2013) to Revision A	Page
• 已发布至生产	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINM-A	16	Analog input	Negative analog input, ADC_A
AINM-B	5	Analog input	Negative analog input, ADC_B
AINP-A	15	Analog input	Positive analog input, ADC_A
AINP-B	6	Analog input	Positive analog input, ADC_B
AVDD	14	Supply	ADC supply voltage
$\overline{\text{CS}}$	9	Digital input	Chip-select signal; active low
DVDD	7	Supply	Digital I/O supply
GND	8, 13	Supply	Device ground
REFGND-A	2	Supply	Reference ground potential, ADC_A
REFGND-B	3	Supply	Reference ground potential, ADC_B
REFIN-A	1	Analog input	Reference voltage input, ADC_A
REFIN-B	4	Analog input	Reference voltage input, ADC_B
SCLK	10	Digital input	Serial communication clock
SDO-A	11	Digital output	Data output for serial communication, ADC_A
SDO-B	12	Digital output	Data output for serial communication, ADC_B
Thermal pad		Supply	Exposed thermal pad. TI recommends connecting the thermal pad to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage	AVDD to GND	−0.3	7	V
	DVDD to GND	−0.3	7	
Analog input voltage	AINP_x to REFGND_x	REFGND_x − 0.3	AVDD + 0.3	V
	AINM_x to REFGND_x	REFGND_x − 0.3	AVDD + 0.3	
	REFIN_x to REFGND_x	REFGND_x − 0.3	AVDD + 0.3	
Digital input voltage	$\overline{CS}$, SCLK to GND	GND − 0.3	DVDD + 0.3	V
Ground voltage difference	REFGND_x − GND		0.3	V
Input current	Any pin except supply pins		±10	mA
Maximum virtual junction temperature, T _j			150	°C
Storage temperature, T _{stg}		−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog power supply		5		V
DVDD	Digital power supply		3.3		V

6.4 Thermal Information

THERMAL METRIC		ADS7250, ADS7850, ADS8350	UNIT
		RTE (WQFN)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	33.3	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	29.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	7.4	°C/W
R _{θJCbot}	Junction-to-case (bottom) thermal resistance	0.9	°C/W

6.5 Electrical Characteristics: All Devices

minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C , $\text{AVDD} = 5\text{ V}$, $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$, and $t_{\text{DATA}} = 750\text{ kSPS}$ (unless otherwise noted); typical values are at $T_A = 25^{\circ}\text{C}$, $\text{AVDD} = 5\text{ V}$, and $\text{DVDD} = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input range, (AINP_x – AINM_x)	$\text{AVDD} \geq 2 \times V_{\text{REF}}^{(1)}$, $\text{AINM}_x = V_{\text{REF}}$	$-V_{\text{REF}}$		V_{REF}	V
V_{INP}	Absolute input voltage, (AINP_x to REFGND)	$\text{AVDD} \geq 2 \times V_{\text{REF}}^{(1)}$, $\text{AINM}_x = V_{\text{REF}}$	0		$2 \times V_{\text{REF}}$	V
V_{INM}	Absolute input voltage, (AINM_x to REFGND)		$V_{\text{REF}} - 0.1$	V_{REF}	$V_{\text{REF}} + 0.1$	V
C_{IN}	Input capacitance	In sample mode		40		pF
		In hold mode		4		
I_{IN}	Input leakage current			1.5		nA
SAMPLING DYNAMICS						
f_{DATA}	Data rate				750	kSPS
t_A	Aperture delay			8		ns
	t_A match	ADC_A to ADC_B		40		ps
	Aperture jitter			10		ps
f_{CLK}	Clock frequency				24	MHz
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage		2.25	2.5	$\text{AVDD} / 2^{(1)}$	V
I_{REF}	Reference input current			300		μA
	Reference leakage current				1	μA
C_{REF}	External ceramic reference capacitance			10		μF
DIGITAL INPUTS⁽²⁾						
V_{IH}	Input voltage, high		0.7 DVDD		$\text{DVDD} + 0.3$	V
V_{IL}	Input voltage, low		-0.3		0.3 DVDD	V
DIGITAL OUTPUTS⁽²⁾						
V_{OH}	Output voltage, high	$I_{\text{OH}} = 500\text{-}\mu\text{A}$ source	0.8 DVDD		DVDD	V
V_{OL}	Output voltage, low	$I_{\text{OH}} = 500\text{-}\mu\text{A}$ sink	0		0.2 DVDD	V
POWER SUPPLY						
AVDD	Analog supply voltage, AVDD to GND		4.5 ⁽¹⁾	5.0	5.5	V
DVDD	Digital supply voltage, DVDD to GND		1.65		5.5	V
$I_{\text{A-DYNA}}$	Analog supply current, during conversion	$\text{AVDD} = 5\text{ V}$, throughput = max		8	9	mA
$I_{\text{A-STAT}}$	Analog supply current, no conversion	$\text{AVDD} = 5\text{ V}$, static		5	7	mA
I_{DVDD}	Digital supply current	$\text{DVDD} = 3.3\text{ V}$		0.25		mA
$P_{\text{D-DYNA}}$	Power dissipation	$\text{AVDD} = 5\text{ V}$, throughput = max		40	45	mW
$P_{\text{D-STAT}}$		$\text{AVDD} = 5\text{ V}$, static		25	35	

- (1) The AVDD supply voltage defines the permissible voltage swing on the analog input pins. To use the maximum dynamic range of the analog input pins, V_{REFIN_x} and AVDD must be in the respective permissible range with $\text{AVDD} \geq 2 \times V_{\text{REFIN}_x}$.
- (2) Specified by design; not production tested.

6.6 Electrical Characteristics: ADS7250

minimum and maximum specifications are at $T_A = -40^\circ\text{C}$ to 125°C , $AVDD = 5\text{ V}$, $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$, and $t_{\text{DATA}} = 750\text{ kSPS}$ (unless otherwise noted); typical values are at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution			12			Bits
DC ACCURACY						
INL	Integral nonlinearity		–1	± 0.5	1	LSB
DNL	Differential nonlinearity		–0.99	± 0.4	1	LSB
V_{OS}	Input offset error		–2	± 0.75	2	mV
	V_{OS} match	ADC_A to ADC_B	–2	± 0.75	2	mV
dV_{OS}/dT	Input offset thermal drift			1		$\mu\text{V}/^\circ\text{C}$
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	$\pm 0.05\%$	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	$\pm 0.05\%$	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	71.5	72.9		dB
		–0.5 dBFS at 100-kHz input		72.9		
		–0.5 dBFS at 250-kHz input		72.5		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	72	73		dB
		–0.5 dBFS at 100-kHz input		73		
		–0.5 dBFS at 250-kHz input		73		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–90		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–82		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		90		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		82		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$, $f_{\text{NOISE}} = 25\text{ kHz}$		–85		dB
$\text{BW}_{(\text{FP})}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.7 Electrical Characteristics: ADS7850

minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 5\text{ V}$, $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$, and $t_{\text{DATA}} = 750\text{ kSPS}$ (unless otherwise noted); typical values are at $T_A = 25^{\circ}\text{C}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution			14			Bits
DC ACCURACY						
INL	Integral nonlinearity		–1.5	±0.8	1.5	LSB
DNL	Differential nonlinearity		–0.99	±0.7	1	LSB
V_{OS}	Input offset error		–1	±0.25	1	mV
	V_{OS} match	ADC_A to ADC_B	–1	±0.25	1	mV
dV_{OS}/dT	Input offset thermal drift			1		$\mu\text{V}/^{\circ}\text{C}$
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/ $^{\circ}\text{C}$
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	79	81		dB
		–0.5 dBFS at 100-kHz input		81		
		–0.5 dBFS at 250-kHz input		79.9		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	79.5	81.5		dB
		–0.5 dBFS at 100-kHz input		81.5		
		–0.5 dBFS at 250-kHz input		81		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–90		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–86		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		90		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		86		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$, $f_{\text{NOISE}} = 25\text{ kHz}$		–90		dB
$\text{BW}_{(\text{FP})}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.8 Electrical Characteristics: ADS8350

minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to 125°C , $AVDD = 5\text{ V}$, $V_{\text{REFIN}_A} = V_{\text{REFIN}_B} = V_{\text{REF}}$, and $t_{\text{DATA}} = 750\text{ kSPS}$ (unless otherwise noted); typical values are at $T_A = 25^{\circ}\text{C}$, $AVDD = 5\text{ V}$, and $DVDD = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
Resolution			16			Bits
DC ACCURACY						
INL	Integral nonlinearity		–2.5	±1	2.5	LSB
DNL	Differential nonlinearity		–0.99	±0.7	2	LSB
V_{OS}	Input offset error		–1	±0.25	1	mV
	V_{OS} match	ADC_A to ADC_B	–1	±0.25	1	mV
dV_{OS}/dT	Input offset thermal drift			1		μV/°C
G_{ERR}	Gain error	Referenced to voltage at REFIN_x	–0.1%	±0.05%	0.1%	
	G_{ERR} match	ADC_A to ADC_B	–0.1%	±0.05%	0.1%	
G_{ERR}/dT	Gain error thermal drift	Referenced to voltage at REFIN_x		1		ppm/°C
CMRR	Common-mode rejection ratio	Both ADCs, dc to 20 kHz		74		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	–0.5 dBFS at 20-kHz input	83.5	84.7		dB
		–0.5 dBFS at 100-kHz input		83.7		
		–0.5 dBFS at 250-kHz input		83		
SNR	Signal-to-noise ratio	–0.5 dBFS at 20-kHz input	84	85		dB
		–0.5 dBFS at 100-kHz input		84.8		
		–0.5 dBFS at 250-kHz input		84		
THD	Total harmonic distortion	–0.5 dBFS at 20-kHz input		–96		dB
		–0.5 dBFS at 100-kHz input		–90		
		–0.5 dBFS at 250-kHz input		–90		
SFDR	Spurious-free dynamic range	–0.5 dBFS at 20-kHz input		96		dB
		–0.5 dBFS at 100-kHz input		90		
		–0.5 dBFS at 250-kHz input		90		
	Isolation between ADC_A and ADC_B	$f_{\text{IN}} = 15\text{ kHz}$, $f_{\text{NOISE}} = 25\text{ kHz}$		–90		dB
$BW_{(\text{FP})}$	Full-power bandwidth	At –3 dB		25		MHz
		At –0.1 dB		5		

6.9 Timing Requirements

			MIN	NOM	MAX	UNIT
$f_{\text{THROUGHPUT}}$	Sample taken to data read	$f_{\text{CLK}} = \text{max}$			750	kSPS
		$f_{\text{CLK}} = \text{max}$	1.33			μs
f_{CLK}	CLOCK frequency	$f_{\text{THROUGHPUT}} = \text{max}$			24	MHz
t_{CLK}	CLOCK period	$f_{\text{THROUGHPUT}} = \text{max}$	41.66			ns
$t_{\text{PH_CK}}$	CLOCK high time		0.4		0.6	t_{CLK}
$t_{\text{PL_CK}}$	CLOCK low time		0.4		0.6	t_{CLK}
t_{ACQ}	Acquisition time	ADS8350, $f_{\text{CLK}} = \text{max}$	120			ns
		ADS7850, $f_{\text{CLK}} = \text{max}$	100			
		ADS7250, $f_{\text{CLK}} = \text{max}$	70			
$t_{\text{PH_CS}}$	$\overline{\text{CS}}$ high time		20			ns
$t_{\text{PH_CS_SHRT}}$	$\overline{\text{CS}}$ high time after frame abort	ADS8350	120			ns
		ADS7850	100			
		ADS7250	70			
$t_{\text{D_CKCS}}$	Delay time from last SCLK falling to $\overline{\text{CS}}$ rising		15			ns
$t_{\text{SU_CSCK}}$	Setup time from $\overline{\text{CS}}$ falling to SCLK falling		15			ns

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time			590	ns
$t_{\text{DV_CSDO}}$	Delay time from $\overline{\text{CS}}$ falling to data enable			12	ns
$t_{\text{DZ_CSDO}}$	Delay time from $\overline{\text{CS}}$ rising to DOUT going to 3-state			10	ns
$t_{\text{D_CKDO}}$	Delay time from SCLK falling to (next) data valid on SDO	3		20	ns

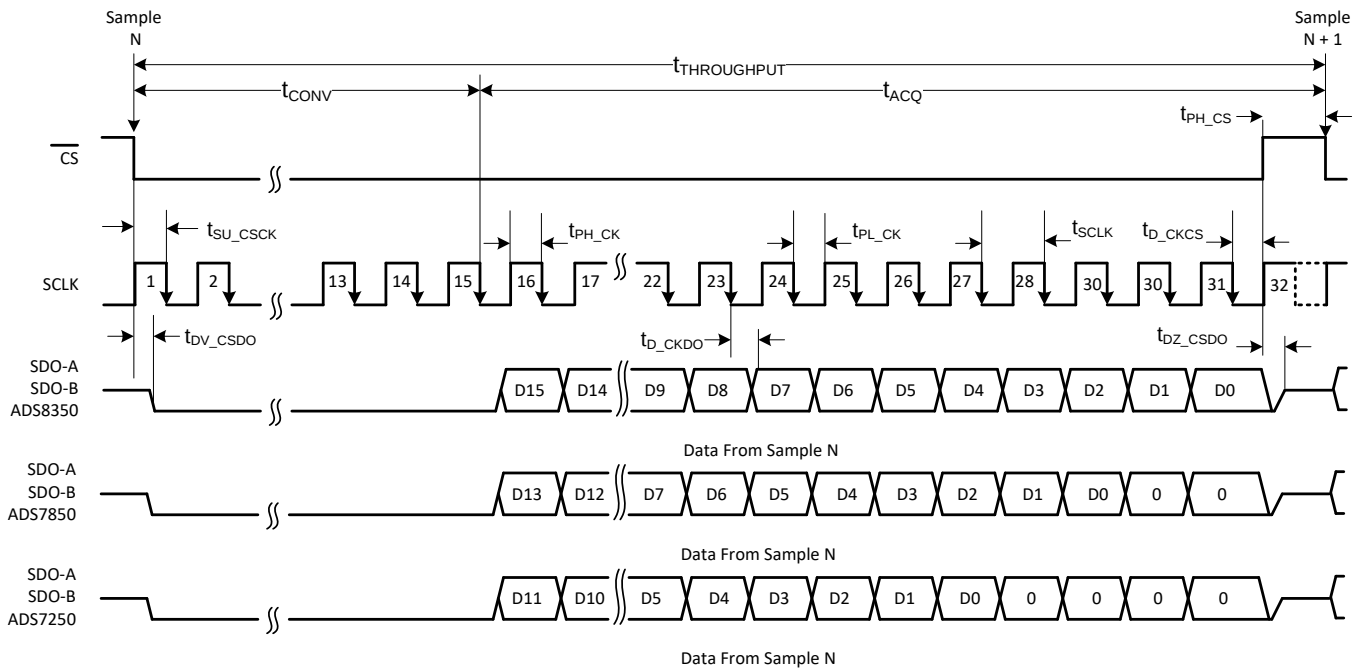


Figure 1. Timing Diagram

6.11 Typical Characteristics: ADS7250

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

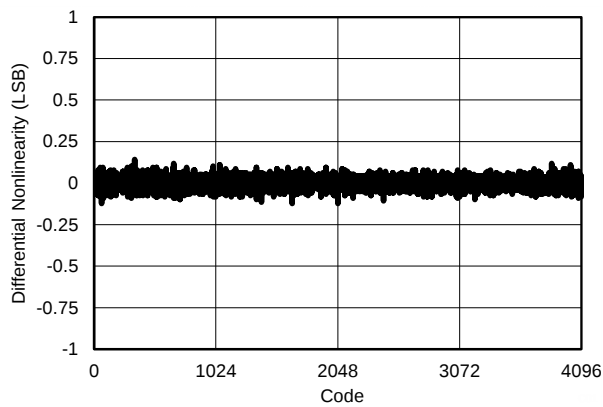


Figure 2. Typical DNL

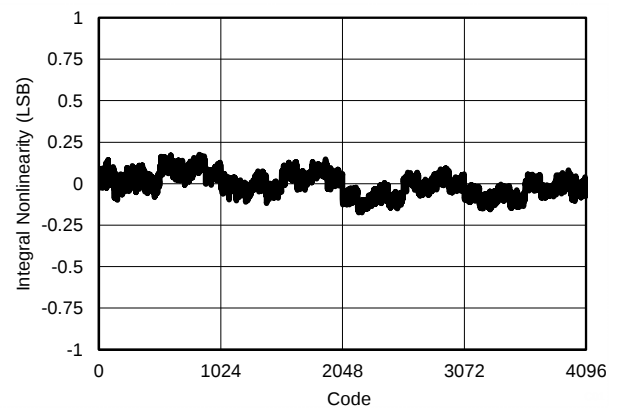


Figure 3. Typical INL

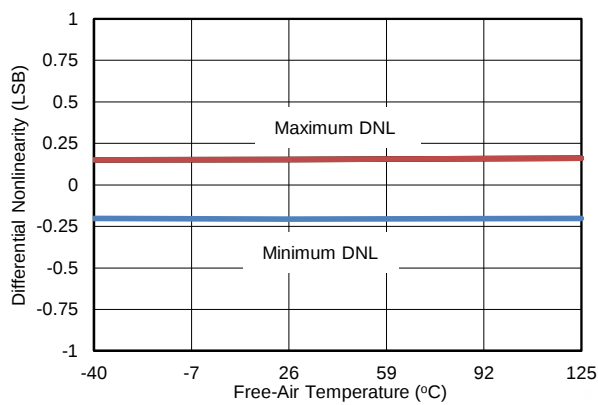


Figure 4. DNL vs Device Temperature

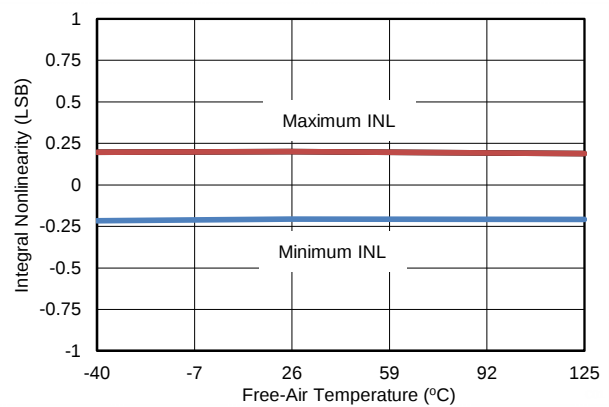


Figure 5. INL vs Device Temperature

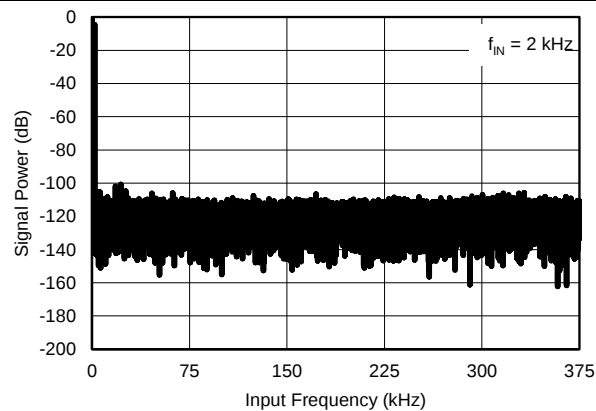


Figure 6. Typical FFT at 2-kHz Input

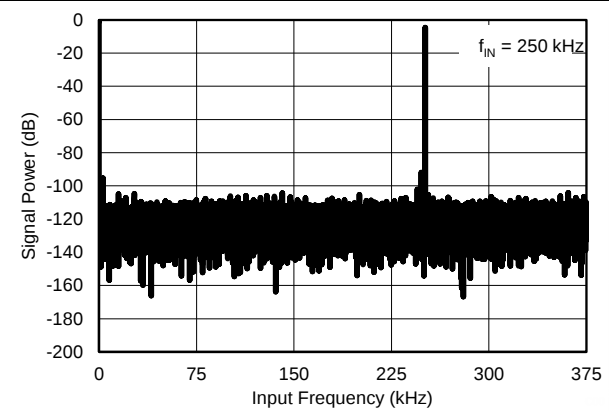


Figure 7. Typical FFT at 250-kHz Input

Typical Characteristics: ADS7250 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

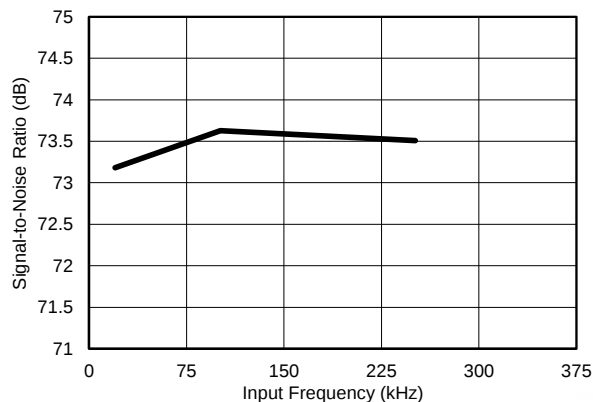


Figure 8. SNR vs Input Frequency

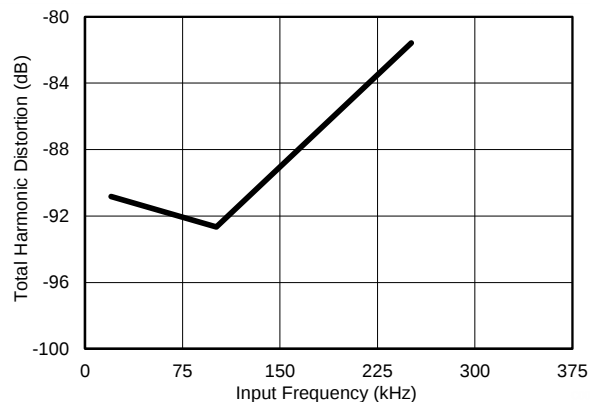


Figure 9. THD vs Input Frequency

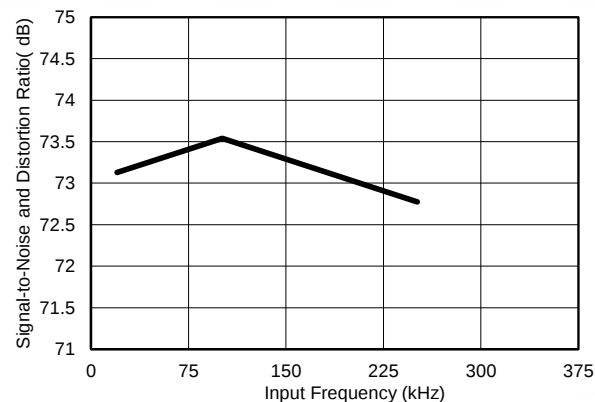


Figure 10. SINAD vs Input Frequency

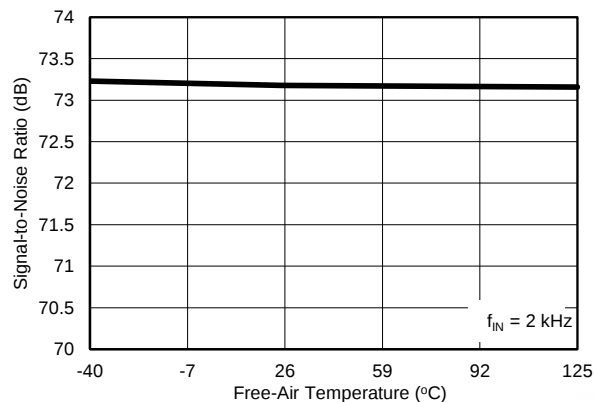


Figure 11. SNR vs Device Temperature

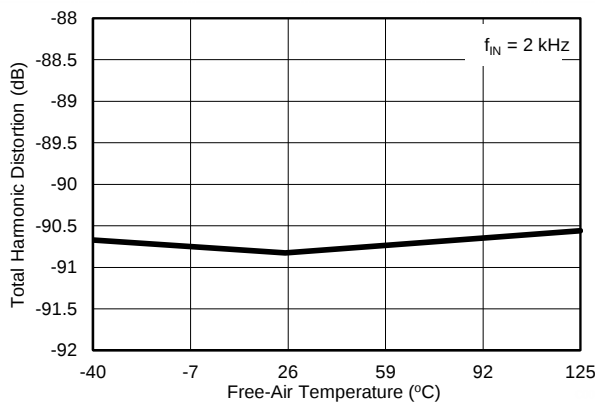


Figure 12. THD vs Device Temperature

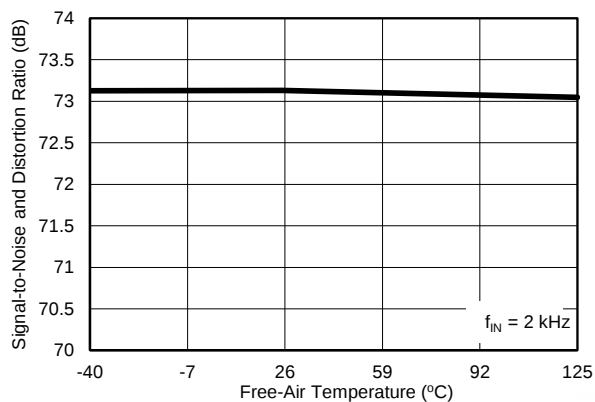


Figure 13. SINAD vs Device Temperature

Typical Characteristics: ADS7250 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

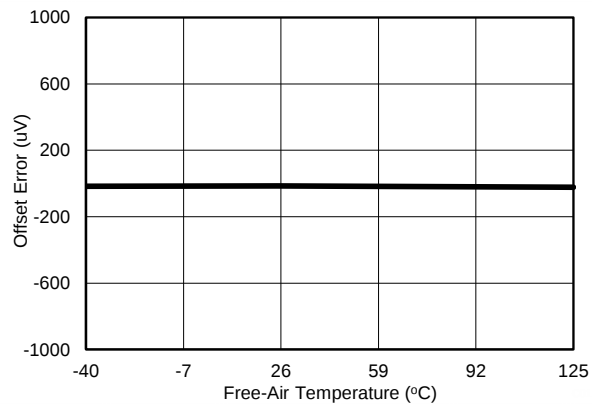


Figure 14. Offset Error vs Device Temperature

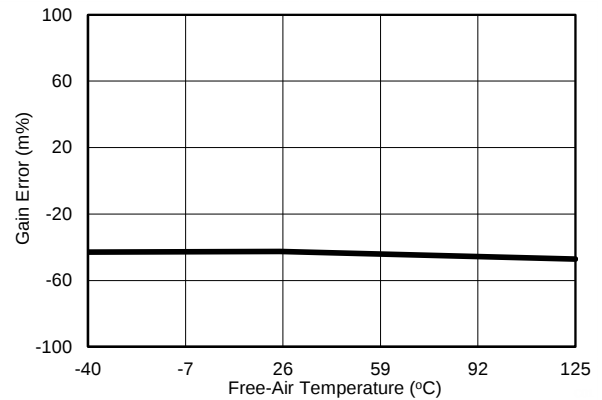


Figure 15. Gain Error vs Device Temperature

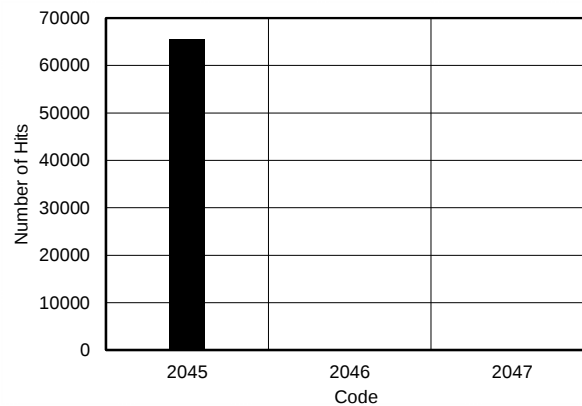


Figure 16. DC Histogram

6.12 Typical Characteristics: ADS7850

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

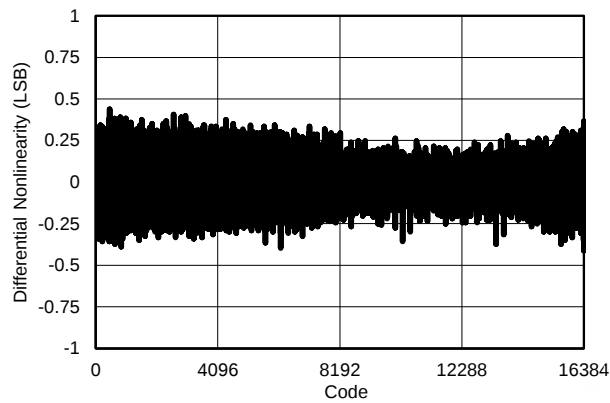


Figure 17. Typical DNL

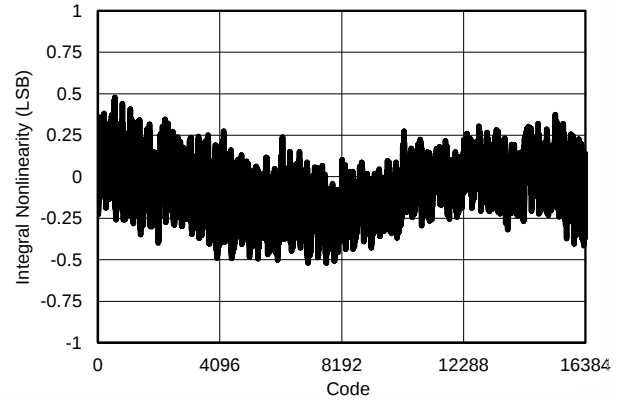


Figure 18. Typical INL

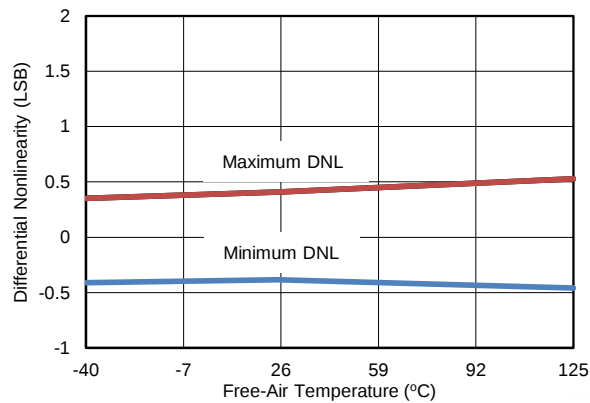


Figure 19. DNL vs Device Temperature

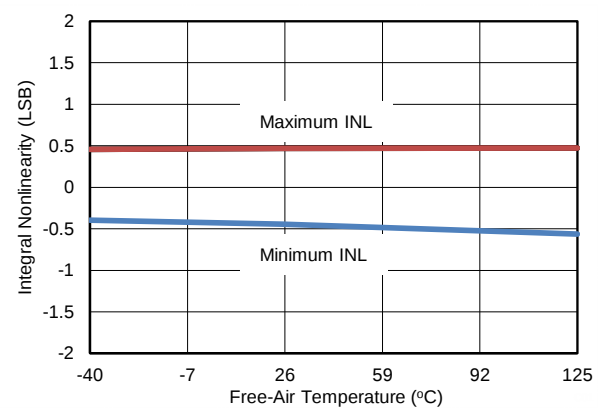


Figure 20. INL vs Device Temperature

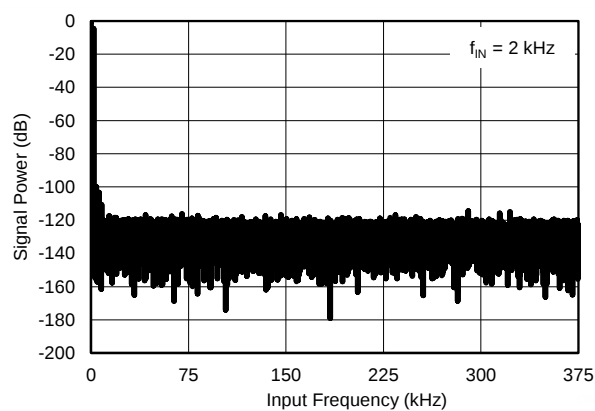


Figure 21. Typical FFT at 2-kHz Input

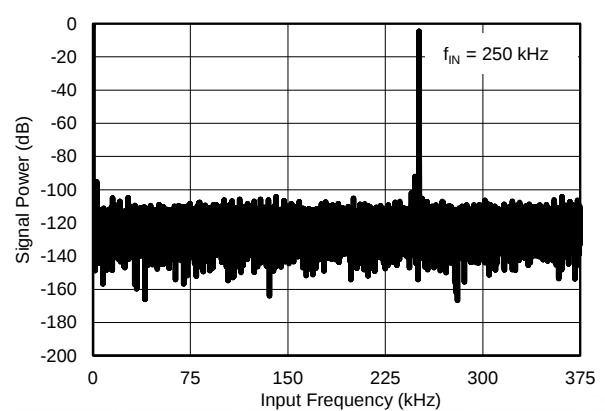


Figure 22. Typical FFT at 250-kHz Input

Typical Characteristics: ADS7850 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

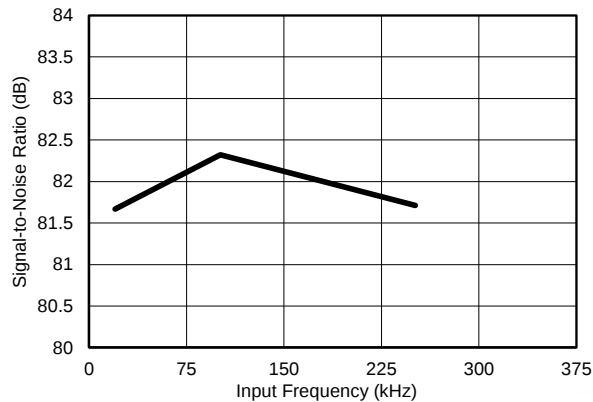


Figure 23. SNR vs Input Frequency

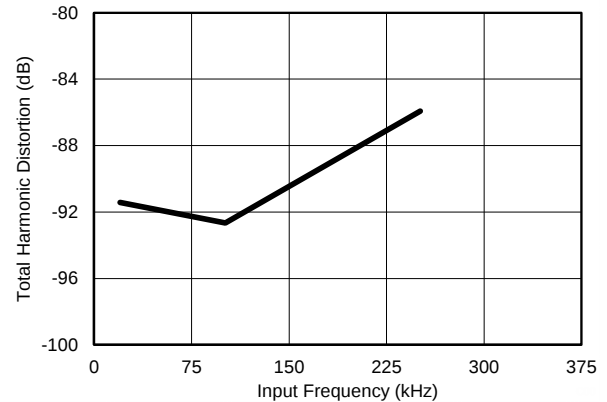


Figure 24. THD vs Input Frequency

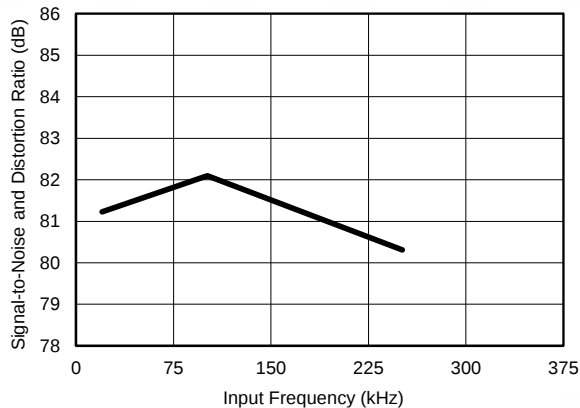


Figure 25. SINAD vs Input Frequency

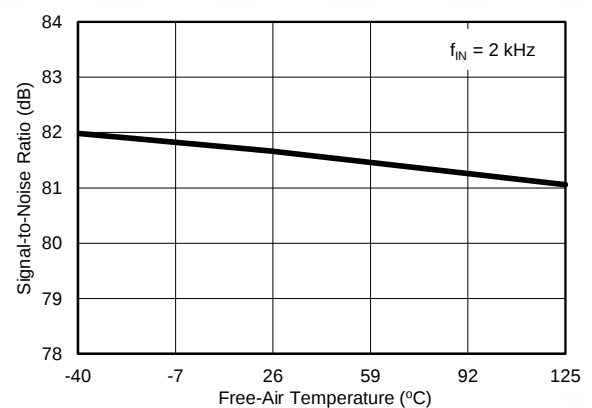


Figure 26. SNR vs Device Temperature

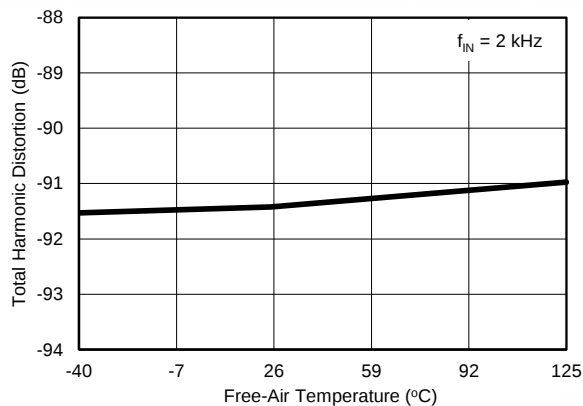


Figure 27. THD vs Device Temperature

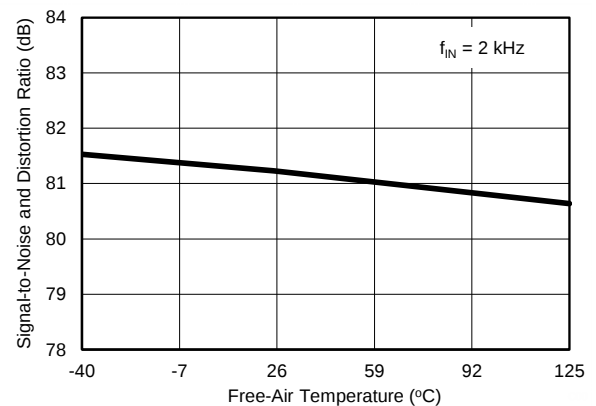


Figure 28. SINAD vs Device Temperature

Typical Characteristics: ADS7850 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

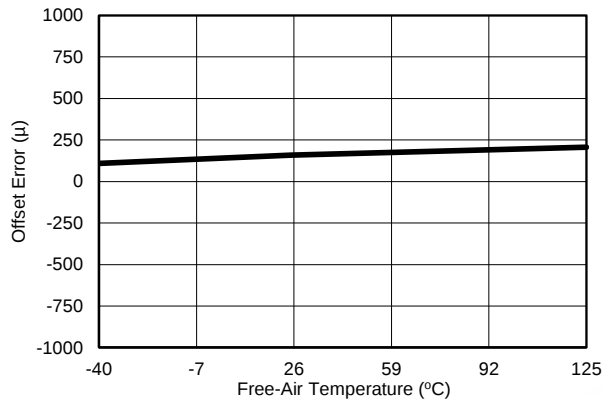


Figure 29. Offset Error vs Device Temperature

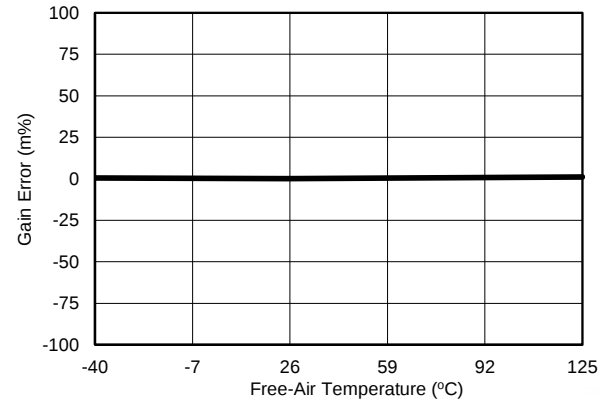


Figure 30. Gain Error vs Device Temperature

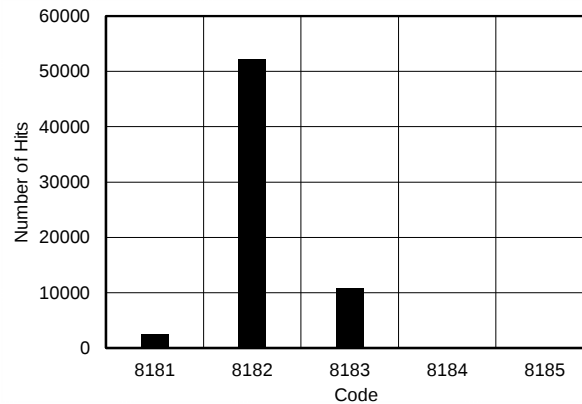


Figure 31. DC Histogram

6.13 Typical Characteristics: ADS8350

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

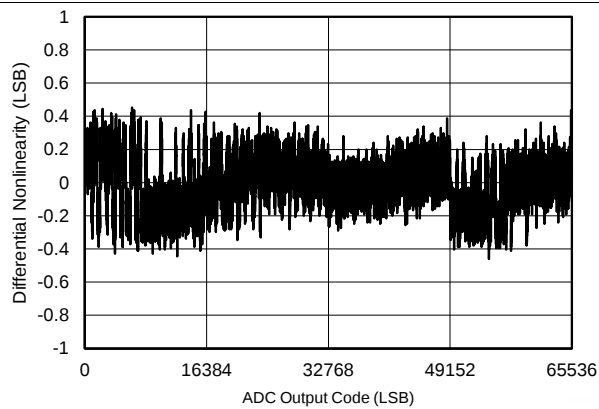


Figure 32. Typical DNL

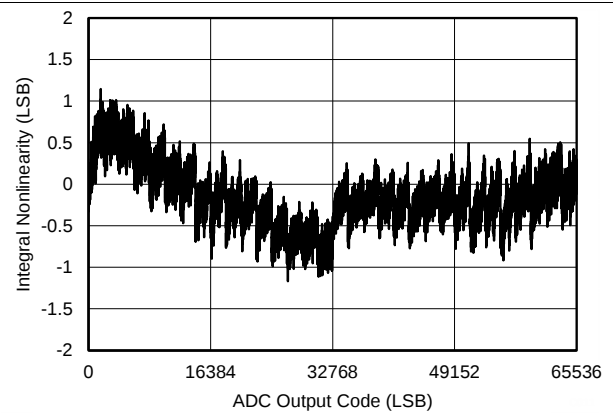


Figure 33. Typical INL

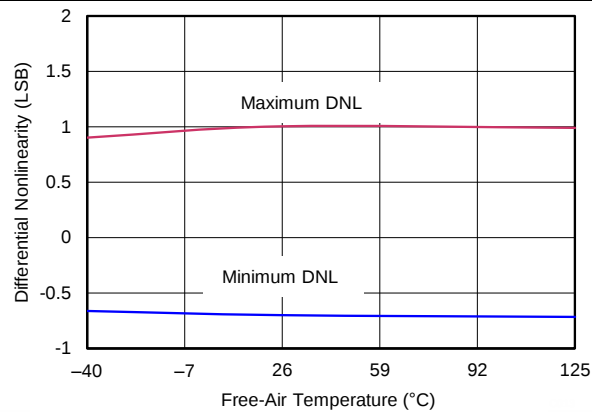


Figure 34. DNL vs Device Temperature

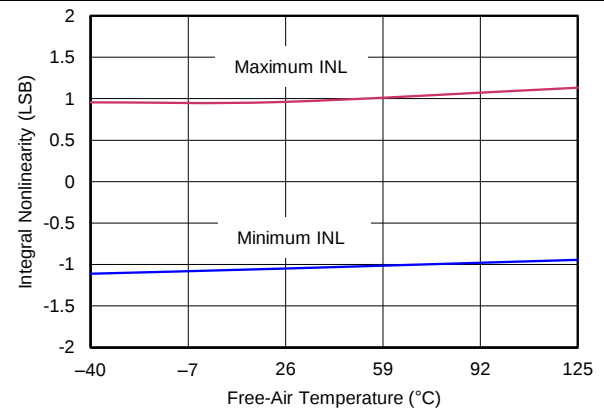


Figure 35. INL vs Device Temperature

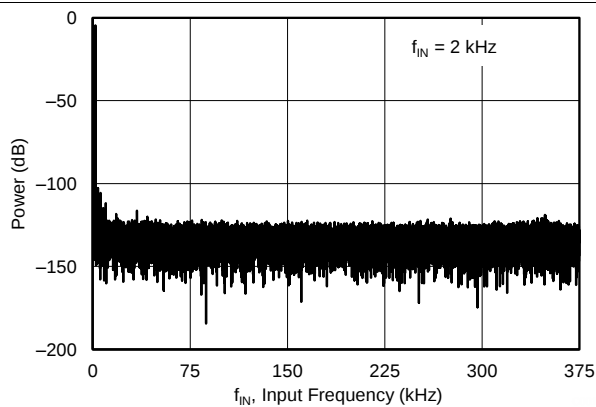


Figure 36. Typical FFT at 2-kHz Input

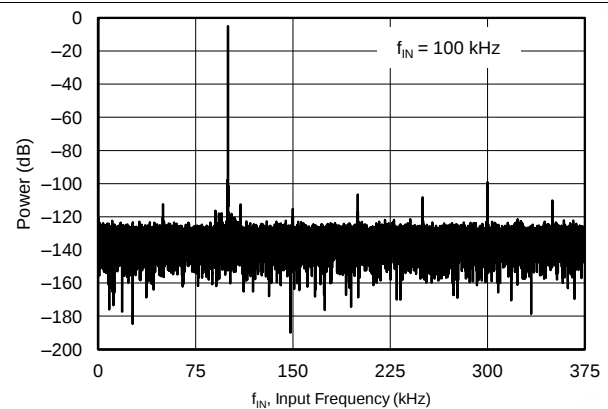


Figure 37. Typical FFT at 100-kHz Input

Typical Characteristics: ADS8350 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

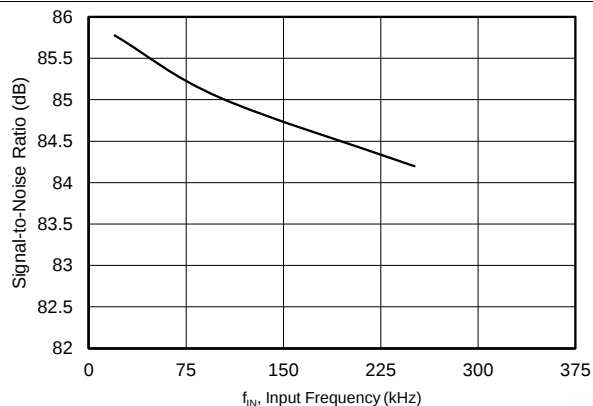


Figure 38. SNR vs Input Frequency

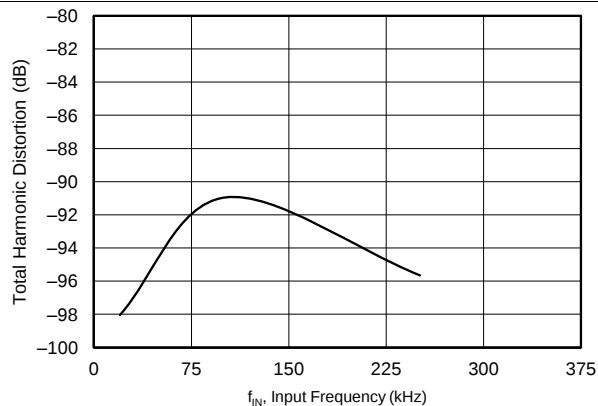


Figure 39. THD vs Input Frequency

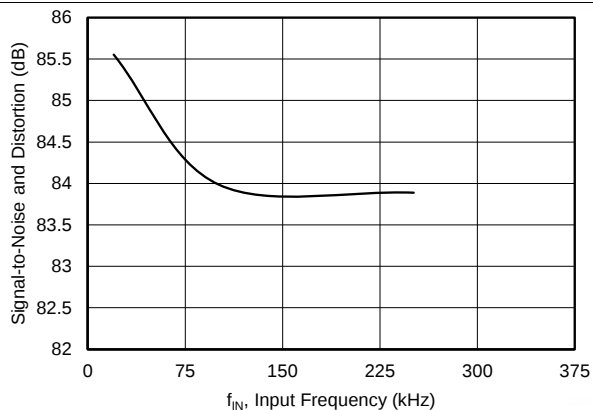


Figure 40. SINAD vs Input Frequency

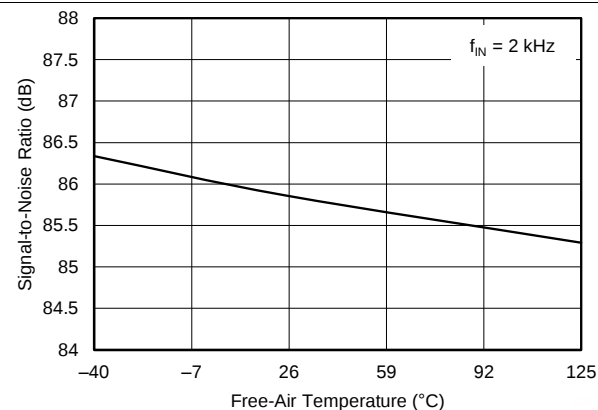


Figure 41. SNR vs Device Temperature

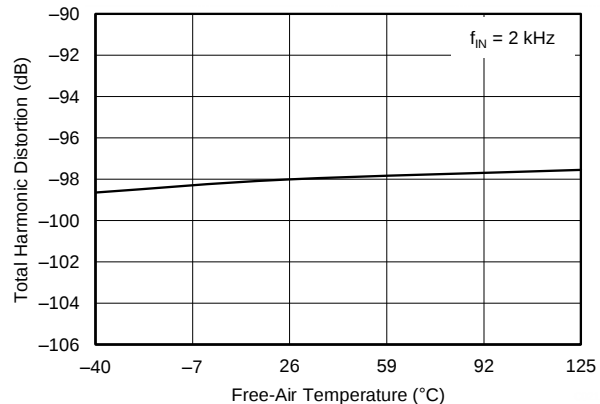


Figure 42. THD vs Device Temperature

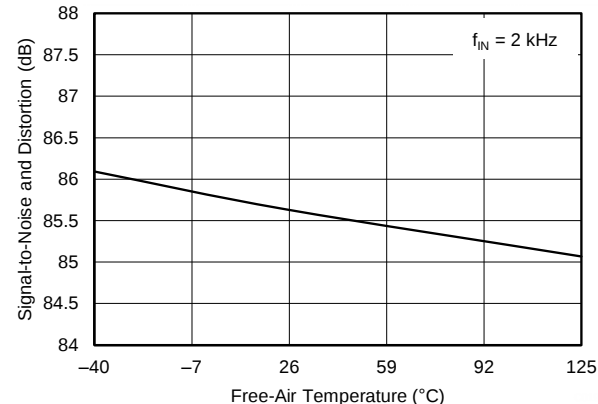


Figure 43. SINAD vs Device Temperature

Typical Characteristics: ADS8350 (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

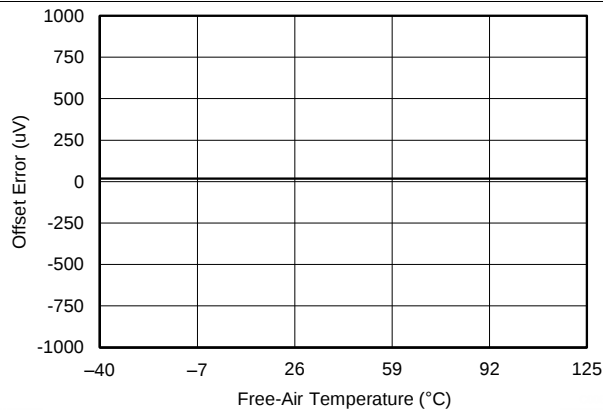


Figure 44. Offset Error vs Device Temperature

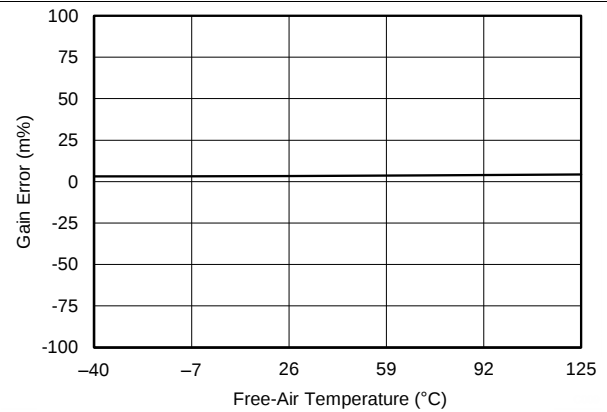


Figure 45. Gain Error vs Device Temperature

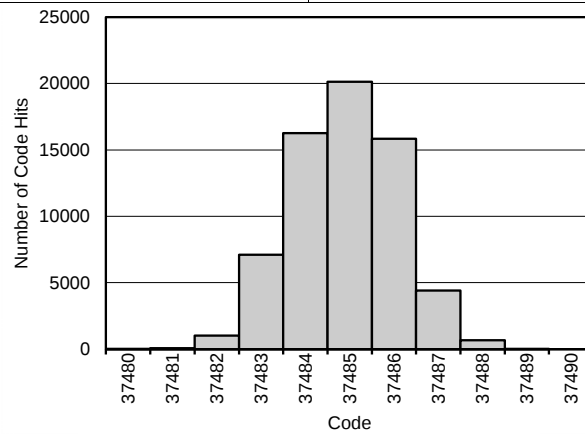


Figure 46. DC Histogram

6.14 Typical Characteristics: All Devices

at $T_A = 25^\circ\text{C}$, $AVDD = 5\text{ V}$, $DVDD = 3.3\text{ V}$, $V_{REF} = 2.5\text{ V}$, and $f_{DATA} = 750\text{ kSPS}$ (unless otherwise noted)

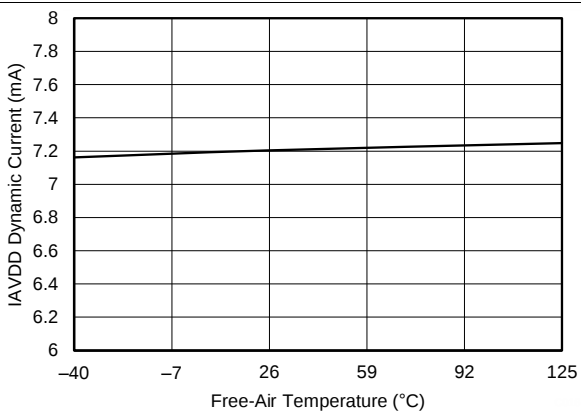


Figure 47. Dynamic Current vs Device Temperature

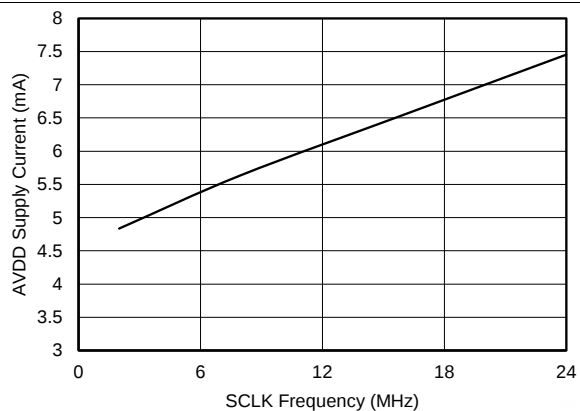


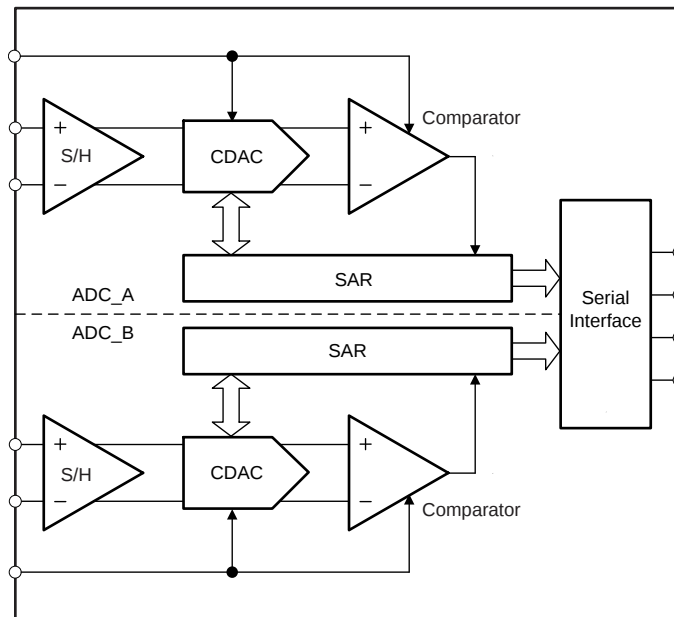
Figure 48. Supply Current vs SCLK Frequency

7 Detailed Description

7.1 Overview

The ADS8350, ADS7850, and ADS7250 belong to a family of dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The devices support pseudo-differential input signals with the input common-mode equal to the reference voltage and the full-scale input range equal to twice the reference voltage. The devices provide a simple serial interface to the host controller and operate over a wide range of digital power supplies.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference

Each device has two simultaneous-sampling ADCs (ADC_A and ADC_B). ADC_A operates with reference voltage $V_{\text{REFIN_A}}$ and ADC_B operates with reference voltage $V_{\text{REFIN_B}}$. These reference voltages must be provided on the REFIN_A and REFIN_B pins, respectively. REFIN_A and REFIN_B may be set to different values as per the application requirement.

As shown in Figure 49, decouple the REFIN_A and REFIN_B pins with the REFGND_A and REFGND_B pins, respectively, with individual 10- μF decoupling capacitors.

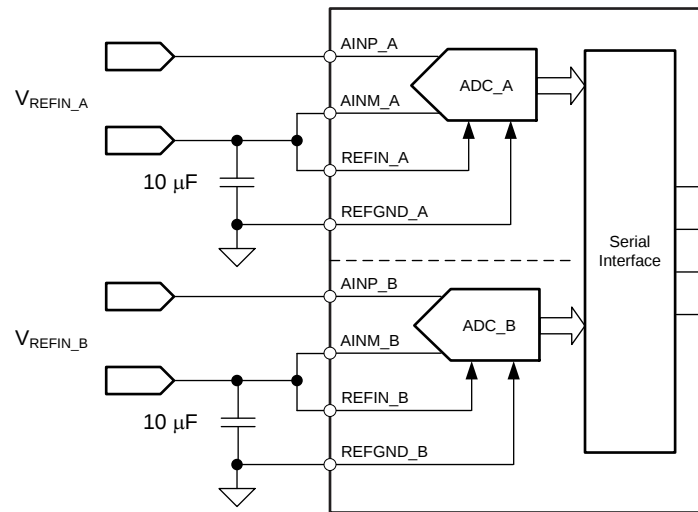


Figure 49. Reference Block Diagram

Feature Description (continued)

7.3.2 Analog Input

The devices support pseudo-differential analog input signals. These inputs are sampled and converted simultaneously by the two ADCs (ADC_A and ADC_B). ADC_A samples and converts ($V_{AINP_A} - V_{AINM_A}$), and ADC_B samples and converts ($V_{AINP_B} - V_{AINM_B}$).

Figure 50a and Figure 50b show equivalent circuits for the ADC_A and ADC_B analog input pins, respectively. R_S (typically 50 Ω) represents the on-state sampling switch resistance, and C_{SAMPLE} represents the device sampling capacitor (typically 40 pF).

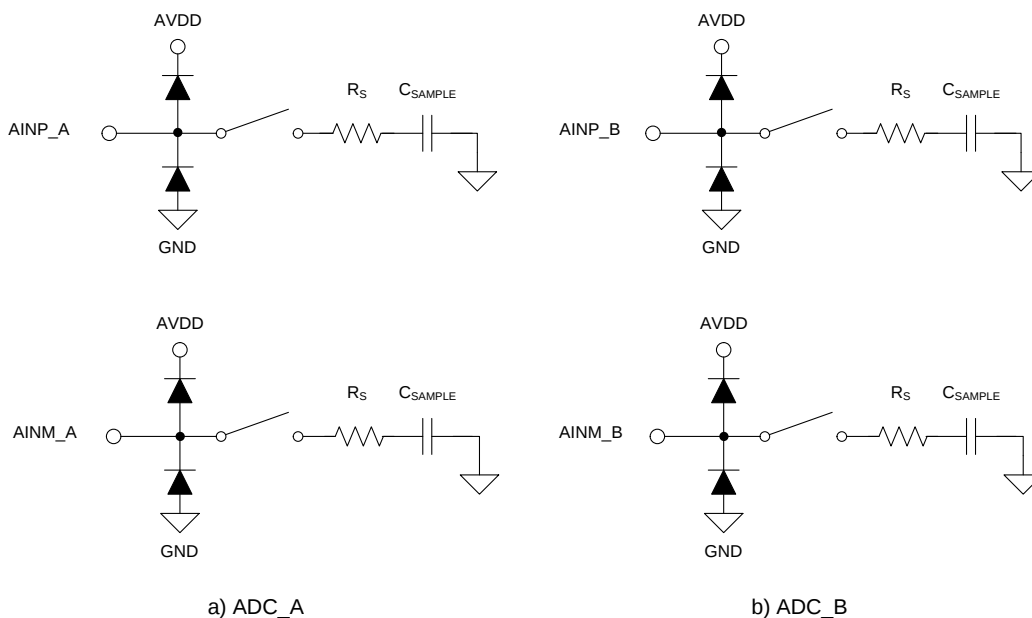


Figure 50. Equivalent Circuit for Analog Input Pins

7.3.2.1 Analog Input Full-Scale Range

The analog input full-scale range (FSR) for ADC_A and ADC_B is twice the reference voltage provided to the particular ADC. By providing different reference voltages (V_{REFIN_A} and V_{REFIN_B}), ADC_A and ADC_B can have different full-scale input ranges. Therefore, the FSR for ADC_A and ADC_B can be determined by Equation 1 and Equation 2, respectively:

$$FSR_ADC_A = 2 \times V_{REFIN_A} \quad (1)$$

$$V_{AINP_A} = 0 \text{ to } 2 \times V_{REFIN_A}$$

$$V_{AINM_A} = V_{REFIN_A}$$

The REFIN_A and AINM_A pins must be shorted and connected to the external reference voltage, V_{REFIN_A} .

$$FSR_ADC_B = 2 \times V_{REFIN_B} \quad (2)$$

$$V_{AINP_B} = 0 \text{ to } 2 \times V_{REFIN_B}$$

$$V_{AINM_B} = V_{REFIN_B}$$

The REFIN_B and AINM_B pins must be shorted and connected to the external reference voltage, V_{REFIN_B} .

To use the full dynamic input range on the analog input pins, AVDD must be as shown in Equation 3, Equation 4, and Equation 5:

$$AVDD \geq 2 \times V_{REFIN_A} \quad (3)$$

$$AVDD \geq 2 \times V_{REFIN_B} \quad (4)$$

$$4.5 \text{ V} \leq AVDD \leq 5.5 \text{ V} \quad (5)$$

Feature Description (continued)

7.3.3 ADC Transfer Function

The device output is in binary twos complement format. Device resolution is calculated by [Equation 6](#):

$$1 \text{ LSB} = (\text{FSR_ADC_x}) / (2^N)$$

where:

- $\text{FSR_ADC_x} = 2 \times V_{\text{REFIN_x}}$ and
- N is the resolution of the ADC : N = 16 for the ADS8350, N = 14 for the ADS7850, and N = 12 for the ADS7250

(6)

[Table 1](#) shows the different input voltages and the corresponding device output codes.

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINM_x)	INPUT VOLTAGE (AINP_x)	PSEUDO-DIFFERENTIAL INPUT TO ADC (AINP_x - AINM_x)		OUTPUT CODE (HEX)			
				CODE	ADS7250	ADS7850	ADS8350
$V_{\text{REFIN_x}}$	0	$-V_{\text{REFIN_x}}$	NFSR	NFSC	800	2000	8000
	1 LSB	$-V_{\text{REFIN_x}} + 1 \text{ LSB}$	$\text{NFSR} + 1 \text{ LSB}$	$\text{NFSC} + 1$	801	2001	8001
	$V_{\text{REFIN_x}} - 1 \text{ LSB}$	-1 LSB	-1 LSB	MC	FFF	3FFF	FFFF
	$V_{\text{REFIN_x}}$	0	0	PLC	000	0000	0000
	$2 \times V_{\text{REFIN_x}} - 1 \text{ LSB}$	$V_{\text{REFIN_x}} - 1 \text{ LSB}$	$\text{PFSR} - 1 \text{ LSB}$	PFSC	7FF	1FFF	7FFF

[Figure 51](#) shows the ideal transfer characteristics for the device.

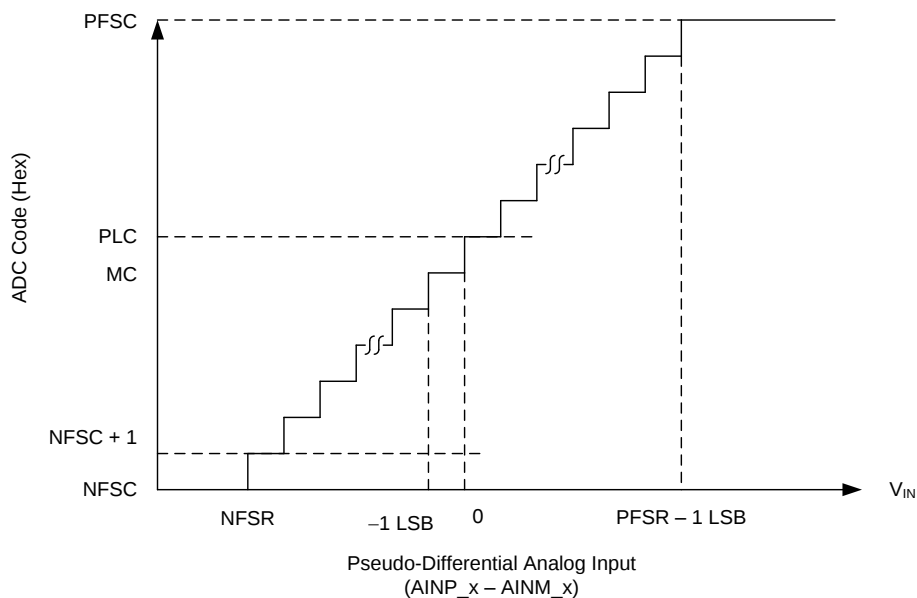


Figure 51. Ideal Transfer Characteristics

7.4 Device Functional Modes

7.4.1 Serial Interface

The devices support a simple, SPI-compatible serial interface to the external digital host. The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO_A and SDO_B pins output the ADC_A and ADC_B conversion results, respectively. Figure 52 shows a detailed timing diagram for these devices.

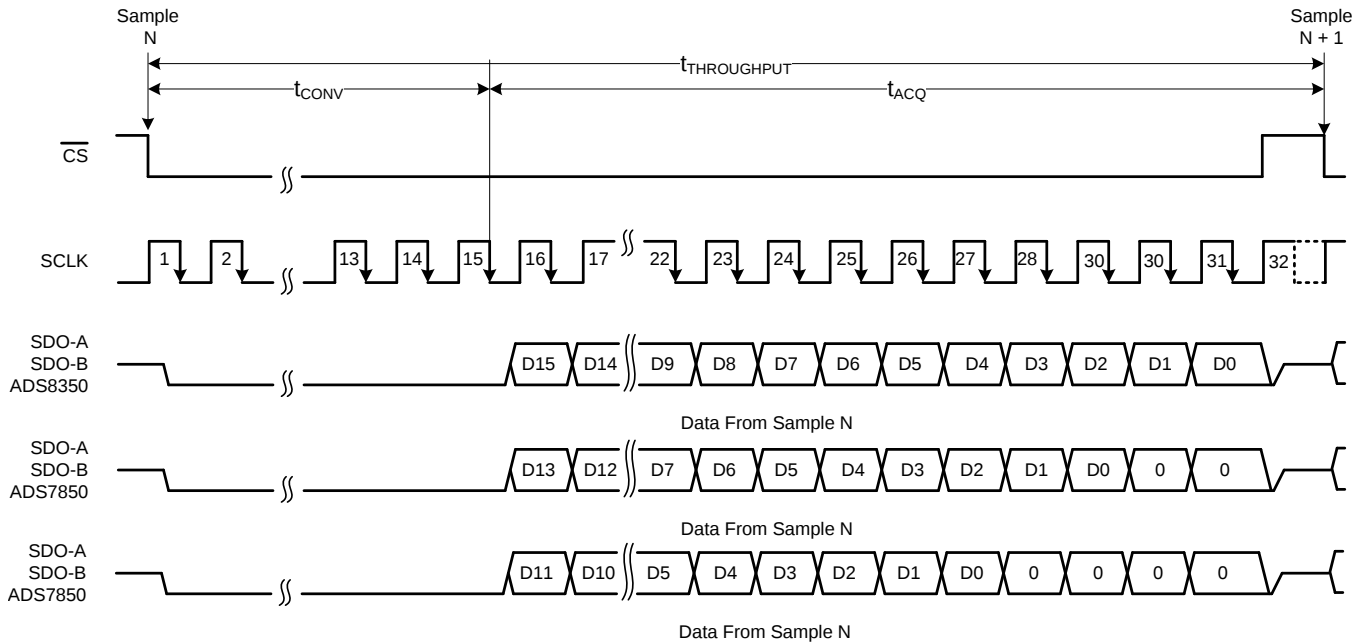


Figure 52. Serial Interface Timing Diagram

A $\overline{CS}$ falling edge brings the serial data bus out of 3-state and also outputs a '0' on the SDO_A and SDO_B pins. The device converts the sampled analog input during the next 14 clocks. SDO_A and SDO_B read '0' during this period. The sample-and-hold circuit goes back into sample mode on the 15th SCLK falling edge and the MSBs of ADC_A and ADC_B are output on SDO_A and SDO_B, respectively. The subsequent clock edges are used to shift out the conversion result using the serial interface, as shown in Table 2. Output data are in binary two's complement format. A $\overline{CS}$ rising edge ends the frame and puts the serial bus into 3-state.

Table 2. Data Launch Edge

DEVICE	PIN	LAUNCH EDGE													
		$\overline{CS} \downarrow$	SCLK												$\overline{CS} \uparrow$
			$\downarrow 1$	...	$\downarrow 14$	$\downarrow 15$	...	$\downarrow 26$	$\downarrow 27$	$\downarrow 28$	$\downarrow 29$	$\downarrow 30$	$\downarrow 31$	...	
ADS8350	SDO-A	0	0	...	0	D15_A	...	D4_A	D3_A	D2_A	D1_A	D0_A	0	...	Hi-Z
	SDO-B	0	0	...	0	D15_B	...	D4_B	D3_B	D2_B	D1_B	D0_B	0	...	Hi-Z
ADS7850	SDO-A	0	0	...	0	D13_A	...	D2_A	D1_A	D0_A	0	0	0	...	Hi-Z
	SDO-B	0	0	...	0	D13_B	...	D2_B	D1_B	D0_B	0	0	0	...	Hi-Z
ADS7250	SDO-A	0	0	...	0	D11_A	...	D0_A	0	0	0	0	0	...	Hi-Z
	SDO-B	0	0	...	0	D11_B	...	D0_B	0	0	0	0	0	...	Hi-Z

7.4.2 Short-Cycling, Frame Abort, and Reconversion Feature

Referring to Table 2, the ADS8350 requires a minimum of 31 SCLK falling edges between the beginning and end of the frame to complete the 16-bit data transfer, the ADS7850 requires a minimum of 29 SCLK falling edges between the beginning and end of the frame to complete the 14-bit data transfer, and the ADS7250 requires a minimum of 27 SCLK falling edges between the beginning and end of the frame to complete the 12-bit data transfer. However, $\overline{\text{CS}}$ can be brought high at any time during the frame to abort the frame or to *short-cycle* the converter.

As shown in Figure 53, if $\overline{\text{CS}}$ is brought high before the 15th SCLK falling edge, the device aborts the conversion and starts sampling the new analog input signal.

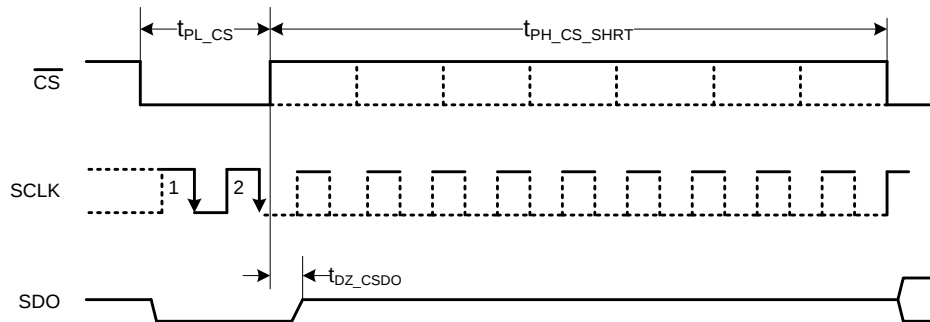


Figure 53. Frame Aborted before 15th SCLK Falling Edge

If $\overline{\text{CS}}$ is brought high after the 15th SCLK falling edge (as shown in Figure 54), the output data bits latched into the digital host before this $\overline{\text{CS}}$ rising edge are still valid data corresponding to sample N.

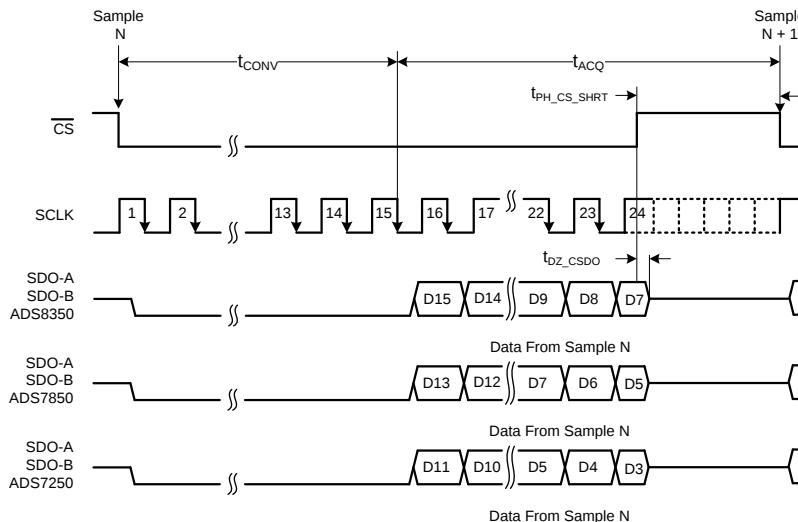


Figure 54. Frame Aborted after 15th SCLK Falling Edge

After aborting the current frame, $\overline{\text{CS}}$ must be kept high for $t_{\text{PH_CS_SHRT}}$ to ensure that the minimum acquisition time (t_{ACQ}) is provided for the next conversion.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing these circuits and provides some application circuits designed using these devices.

8.2 Typical Applications

8.2.1 DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput

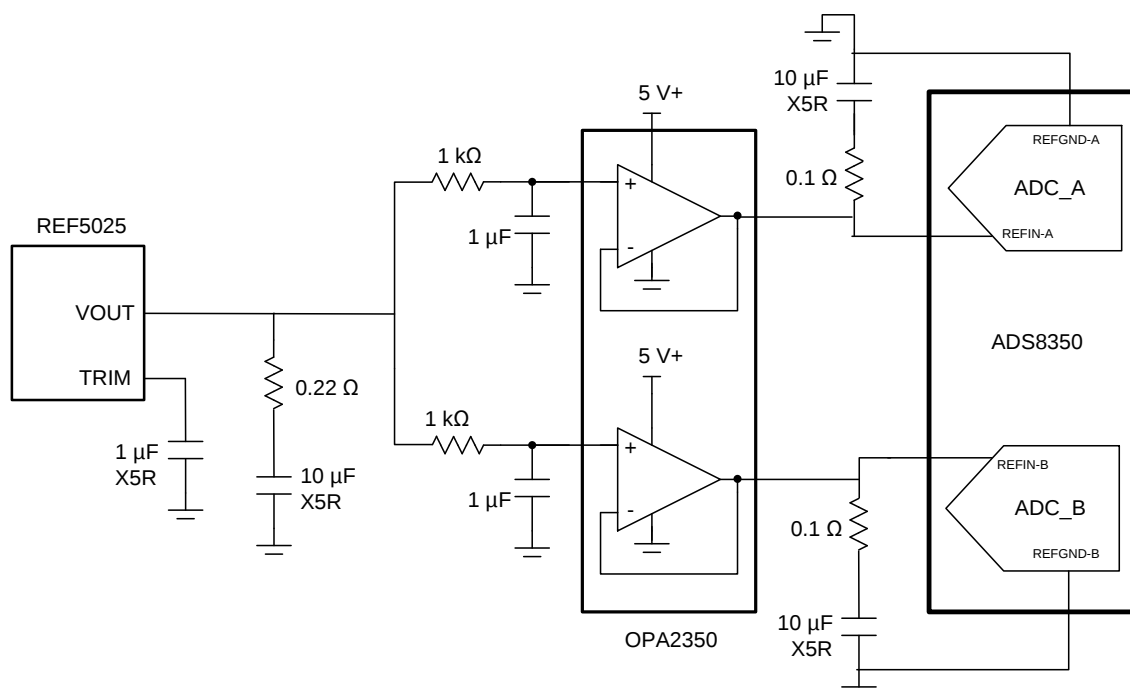


Figure 55. Reference Drive Circuit with $V_{REF} = 2.5\text{ V}$

Typical Applications (continued)

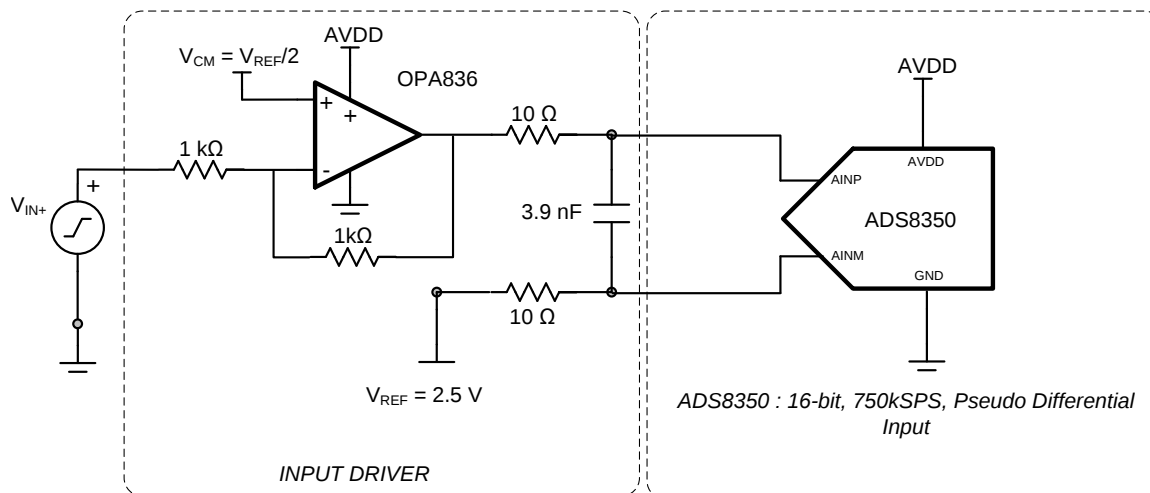


Figure 56. DAQ Circuit: Maximum SINAD for a 10-kHz Input Signal at 750-kSPS Throughput

8.2.1.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve $> 84\text{-dB}$ SNR and $< -90\text{-dB}$ THD at a 100-kHz input frequency.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 ADC Reference Driver

The external reference source to the device must provide low-drift and very accurate voltage for the ADC reference input and support the dynamic charge requirements without affecting the noise and linearity performance of the device. The output broadband noise of most references can be in the order of a few $100\text{ }\mu\text{V}_{\text{RMS}}$. Therefore, in order to prevent any degradation in the noise performance of the ADC, the output of the voltage reference must be appropriately filtered by using a low-pass filter with a cutoff frequency of a few hundred Hertz.

After band-limiting the noise from the reference source, the next important step is to design a reference buffer that can drive the dynamic load posed by the reference input of the ADC. At the start of each conversion, the reference buffer must regulate the voltage of the reference pin within 1 LSB of the intended value. This condition necessitates the use of a large filter capacitor at the reference pin of the ADC. The amplifier selected to drive this large capacitor should have low output impedance, low offset, and temperature drift specifications.

To reduce the dynamic current requirements and crosstalk between the channels, a separate reference buffer is recommended for driving the reference input of each ADC channel.

The application circuit in Figure 55 shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply.

The 2.5-V reference voltage is generated by the high-precision, low-noise REF5025 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be $10\text{ }\mu\text{F}$. The low output impedance, low noise, and fast settling time makes the OPA2350 a good choice for driving this high capacitive load.

8.2.1.2.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a fly-wheel RC filter. The amplifier is used for signal conditioning of the input voltage and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

Typical Applications (continued)

8.2.1.2.2.1 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the amplifier bandwidth should be selected as described in [Equation 7](#):

$$\text{Unity – Gain Bandwidth} \geq 4 \times \left(\frac{1}{2\pi \times (R_{FLT} + R_{FLT}) \times C_{FLT}} \right) \quad (7)$$

- **Noise.** Noise contribution of the front-end amplifiers should be as low as possible to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit should be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency RC filter, as explained in [Equation 8](#).

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f_AMP_PP}}{6.6} \right)^2 + e_{n_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{\left(\frac{SNR(dB)}{20} \right)}$$

where:

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in μV_{RMS} ,
- e_{n_RMS} is the amplifier broadband noise density in $nV/\sqrt{Hz}$,
- f_{-3dB} is the 3-dB bandwidth of the RC filter, and
- N_G is the noise gain of the front-end circuit, which is equal to '1' in a buffer configuration. (8)
- **Distortion.** Both the ADC and the input driver introduce nonlinearity in a data acquisition block. As a rule of thumb, to ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver should be at least 10 dB lower than the distortion of the ADC, as shown in [Equation 9](#).

$$THD_{AMP} \leq THD_{ADC} - 10 \text{ (dB)} \quad (9)$$

- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, the settling behavior of the input driver should always be verified by TINA™-SPICE simulations before selecting the amplifier.

Typical Applications (continued)

8.2.1.2.2 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an analog, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, for which the 3-dB bandwidth is optimized based on specific application requirements. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. For ac signals, the filter bandwidth should be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system.

Besides filtering noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT} , is connected across the ADC inputs (as shown in Figure 57).

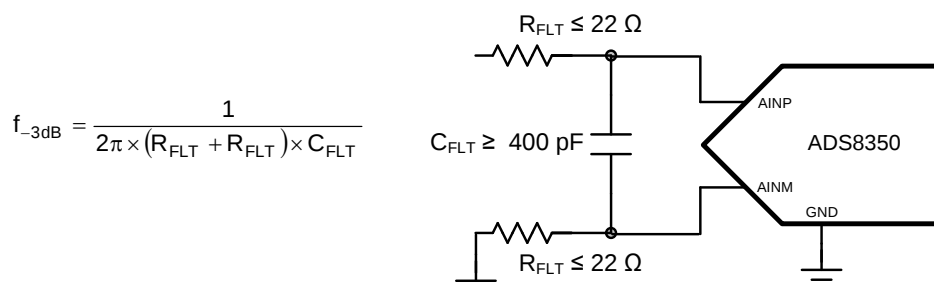


Figure 57. Antialiasing Filter

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. Thus, the value of C_{FLT} should be greater than 400 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For these devices, TI recommends limiting the value of R_{FLT} to a maximum of 22 Ω in order to avoid any significant degradation in linearity performance. The tolerance of the selected resistors can be chosen as 1% because the use of a differential capacitor at the input balances the effects resulting from any resistor mismatch.

The input amplifier bandwidth should be much higher than the cutoff frequency of the antialiasing filter. TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers might require more bandwidth than others to drive similar filters. If an amplifier has less than a 40° phase margin with 22- Ω resistors, using a different amplifier with higher bandwidth or reducing the filter cutoff frequency with a larger differential capacitor is advisable.

The application circuit shown in Figure 56 is optimized to achieve lowest distortion and lowest noise for a 10-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

Typical Applications (continued)

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. The low-power [OPA836](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion, high-bandwidth specifications. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

8.2.1.3 Application Curve

[Figure 58](#) shows FFT plot and test results obtained with circuit configuration shown in [Figure 56](#).

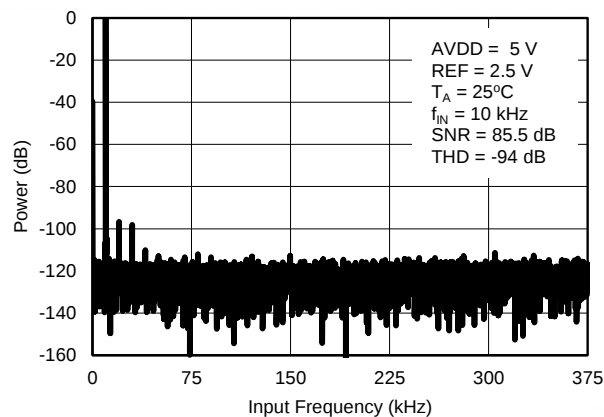


Figure 58. FFT Plot and Test Results with ADS8350

Typical Applications (continued)

8.2.2 DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

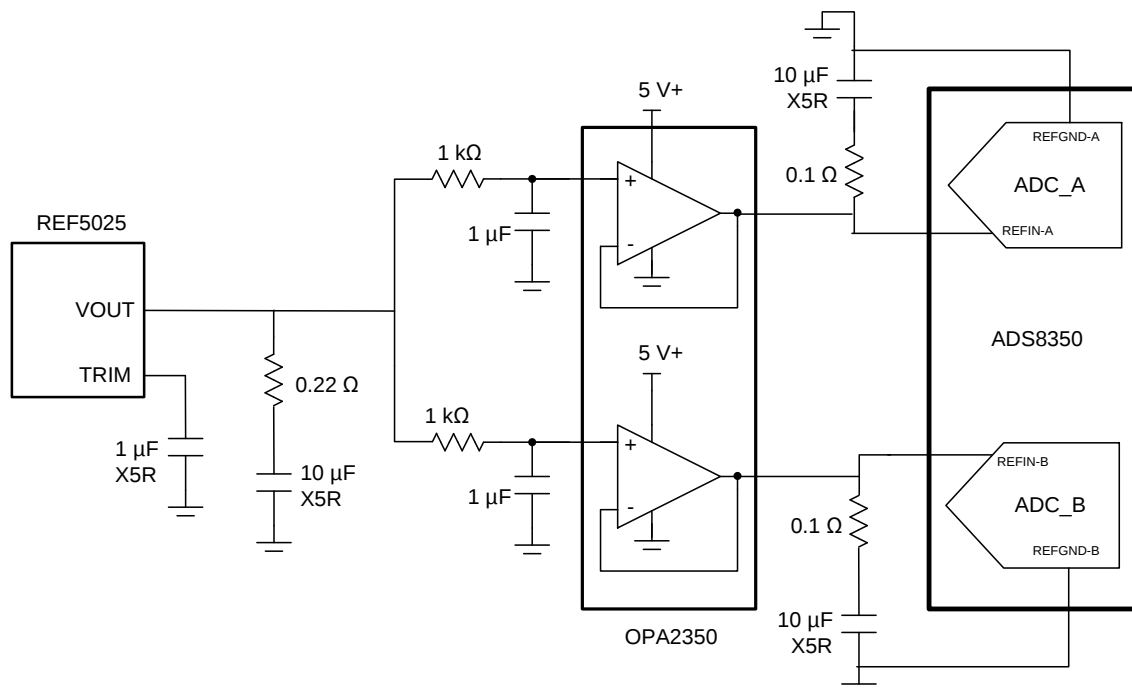


Figure 59. Reference Drive Circuit with $V_{REF} = 2.5\text{ V}$

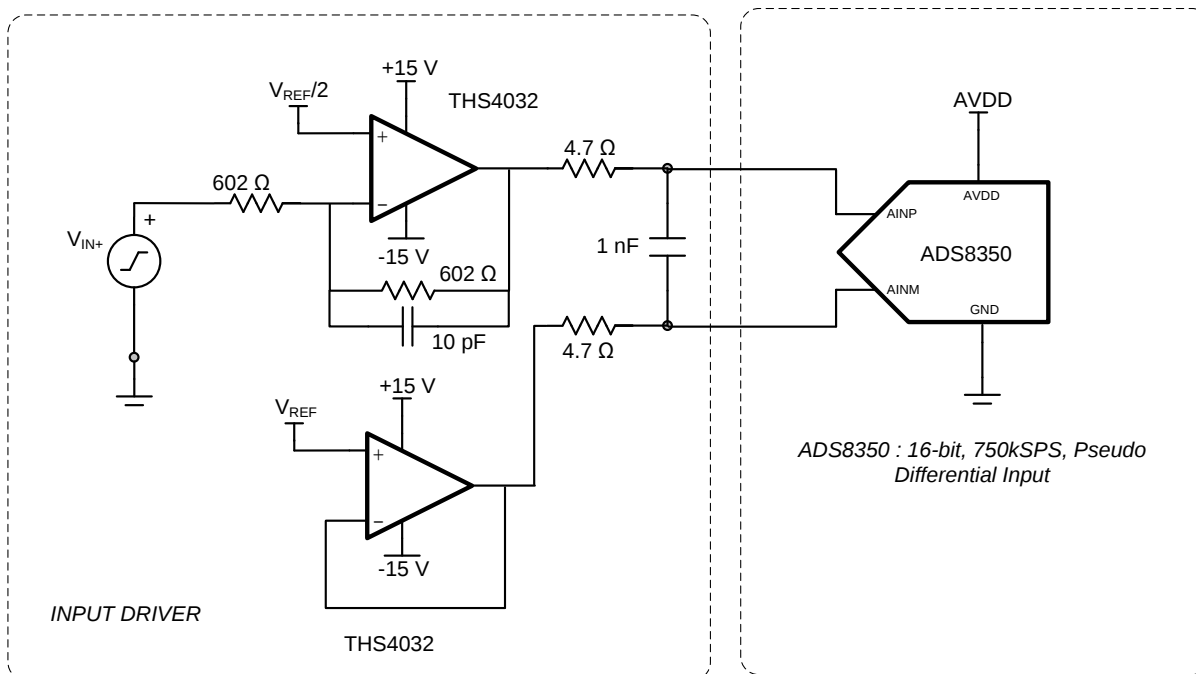


Figure 60. DAQ Circuit: Maximum SINAD for a 100-kHz Input Signal at 750-kSPS Throughput

Typical Applications (continued)

8.2.2.1 Design Requirements

For the ADS8350, design an input driver and reference driver circuit to achieve > 84-dB SNR and < –90-dB THD at a 100-kHz input frequency.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 ADC Reference Driver

Refer to the [ADC Reference Driver](#) section for a detailed design procedure for the ADC reference driver.

The application circuit in [Figure 55](#) shows the schematic of a complete reference driver circuit that generates a voltage of 2.5-V dc using a single 5-V supply. This circuit is suitable to drive the reference of the ADS8350 at sampling rates up to 750 kSPS.

The 2.5-V reference voltage is generated by the high-precision, low-noise [REF5025](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz. The decoupling capacitor on each reference pin is selected to be 10 µF. The low output impedance, low noise, and fast settling time makes the [OPA2350](#) a good choice for driving this high capacitive load.

8.2.2.2.2 ADC Input Driver

Refer to [ADC Input Driver](#) section for the detailed design procedure for an ADC input driver.

The application circuit shown in [Figure 60](#) is optimized to achieve lowest distortion and lowest noise for a 100-kHz input signal. The input signal is processed through a high-bandwidth, low-distortion amplifier in an inverting gain configuration and a low-pass RC filter before being fed into the ADS8350 operating at 750-kSPS throughput.

As a rule of thumb, the distortion from the input driver should be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the amplifier in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the input of the amplifier. The [THS4032](#), used as an input driver, provides exceptional ac performance because of its extremely low-distortion, low-noise, and high-bandwidth specifications. The ADC AINM pin is also driven to V_{REF} with the same amplifier to match the source impedance and to take full advantage of the pseudo-differential input structure of the ADC. In addition, the components of the antialiasing filter are such that the noise from the front-end circuit is kept low without adding distortion to the input signal.

NOTE

The same circuit can be used with the ADS7250 and ADS7850 to achieve their rated specifications.

Typical Applications (continued)

8.2.2.3 Application Curve

Figure 61 shows FFT plot and test results obtained with circuit configuration shown in Figure 60.

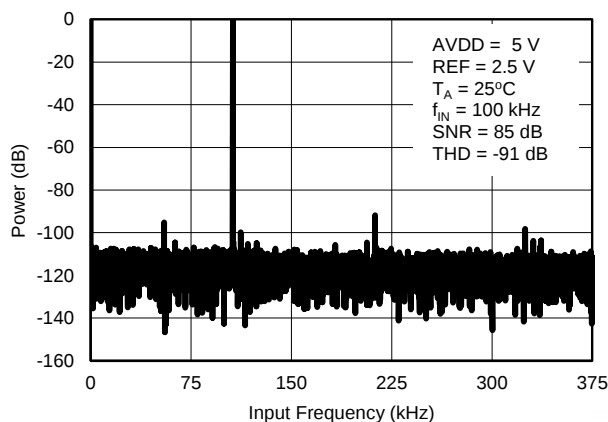


Figure 61. FFT Plot and Test Results with ADS8350

9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The ADC operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible range.

The AVDD supply voltage value defines the permissible voltage swing on the analog input pins. To avoid saturation of output codes, the external reference voltages V_{REFIN_A} and V_{REFIN_B} should be as shown in Equation 10:

$$2\text{ V} \leq V_{REFIN_X} \leq AVDD / 2 \quad (10)$$

In other words, in order to use the V_{REFIN_X} external reference voltage and use the full dynamic range on the analog input pins, AVDD must be set as shown in Equation 11, Equation 12, and Equation 13:

$$AVDD \geq 2 \times V_{REFIN_A} \quad (11)$$

$$AVDD \geq 2 \times V_{REFIN_B} \quad (12)$$

$$4.5\text{ V} \leq AVDD \leq 5.5\text{ V} \quad (13)$$

Decouple the AVDD and DVDD pins with the GND pin using individual 10-μF decoupling capacitors, as shown in Figure 62.

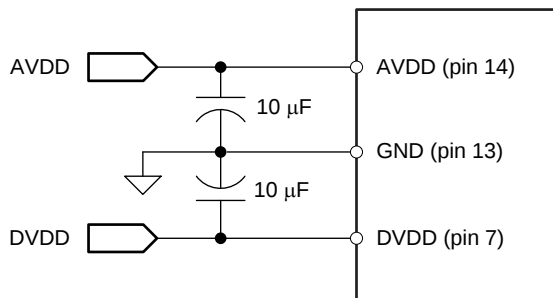


Figure 62. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

Figure 63 shows a board layout example for the ADS7250, ADS7850, and ADS8350. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. As shown in Figure 63, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the device.

The power sources to the ADS8350 must be clean and well-bypassed. Use 10- μ F ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

The REFIN-A and REFIN-B reference inputs are bypassed with 10- μ F, X7R-grade ceramic capacitors (C_{REF-x}). Although the reference inputs of the device draw little current on average, there are instantaneous dynamic current demands placed on the reference circuitry characteristic of SAR ADCs. Place the reference bypass capacitors as close as possible to the reference REFIN-x pins and connect the bypass capacitors using short, low-inductance connections. Avoid placing vias between the REFIN-x pins and the bypass capacitors. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation. Small 0.1- Ω to 0.2- Ω resistors (R_{REF-x}) are used in series with the reference bypass capacitors to improve stability.

The fly-wheel RC filters are placed immediately next to the input pins. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Figure 63 shows the C_{IN-A} and C_{IN-B} filter capacitors placed across the analog input pins of the device.

10.2 Layout Example

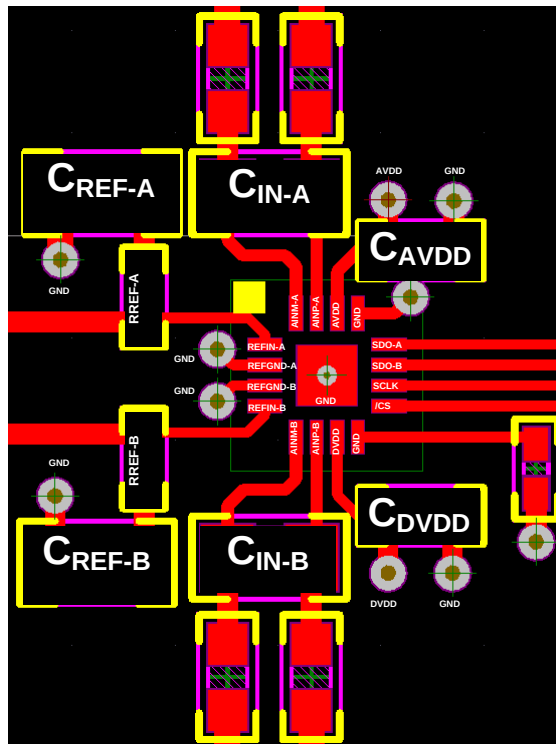


Figure 63. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

如需相关文档，请参阅：

- [REF50xx 低噪声、极低温漂、高精度电压基准](#)
- [MicroAmplifier 系列 OPAx350 高速单电源轨至轨运算放大器](#)
- [OPAx836 极低功耗、轨至轨输出、负轨输入、电压反馈运算放大器](#)
- [THS403x 100MHz 低噪声高速放大器](#)

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 3. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
ADS8350	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS7850	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
ADS7250	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](#) 上的器件产品文件夹。请单击右上角的 [提醒我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](#) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

TINA, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7250IRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250	Samples
ADS7250IRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7250	Samples
ADS7850IRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850	Samples
ADS7850IRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7850	Samples
ADS8350IRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350	Samples
ADS8350IRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8350	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

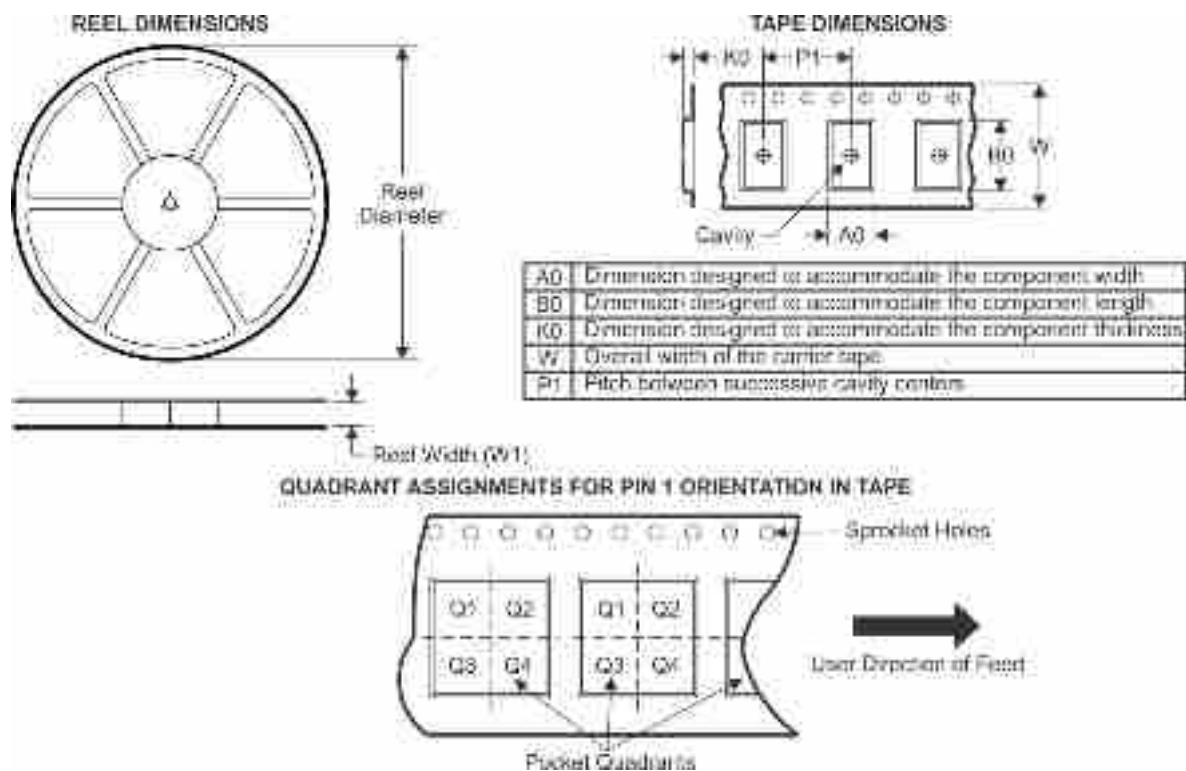
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

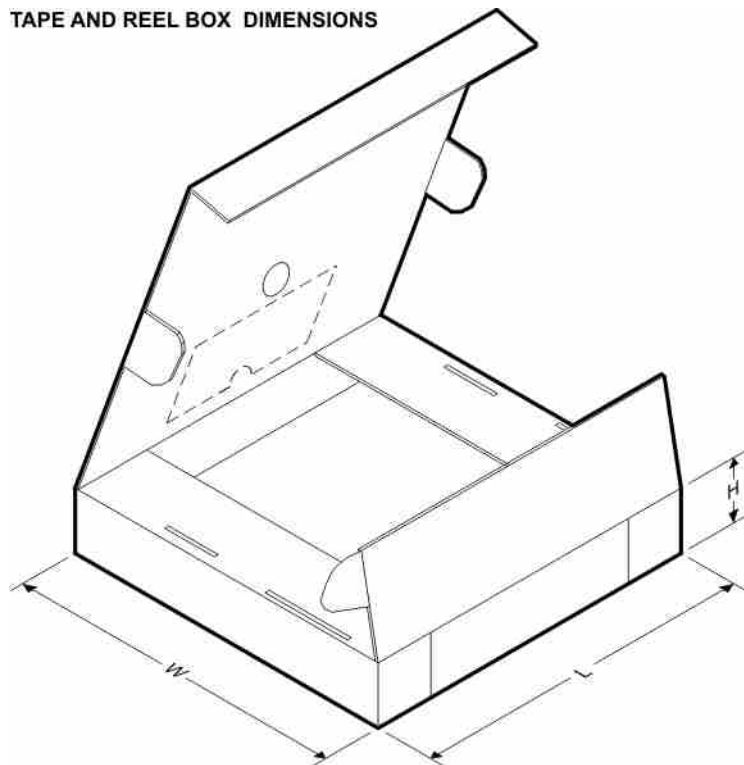
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7250IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7250IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7850IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8350IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

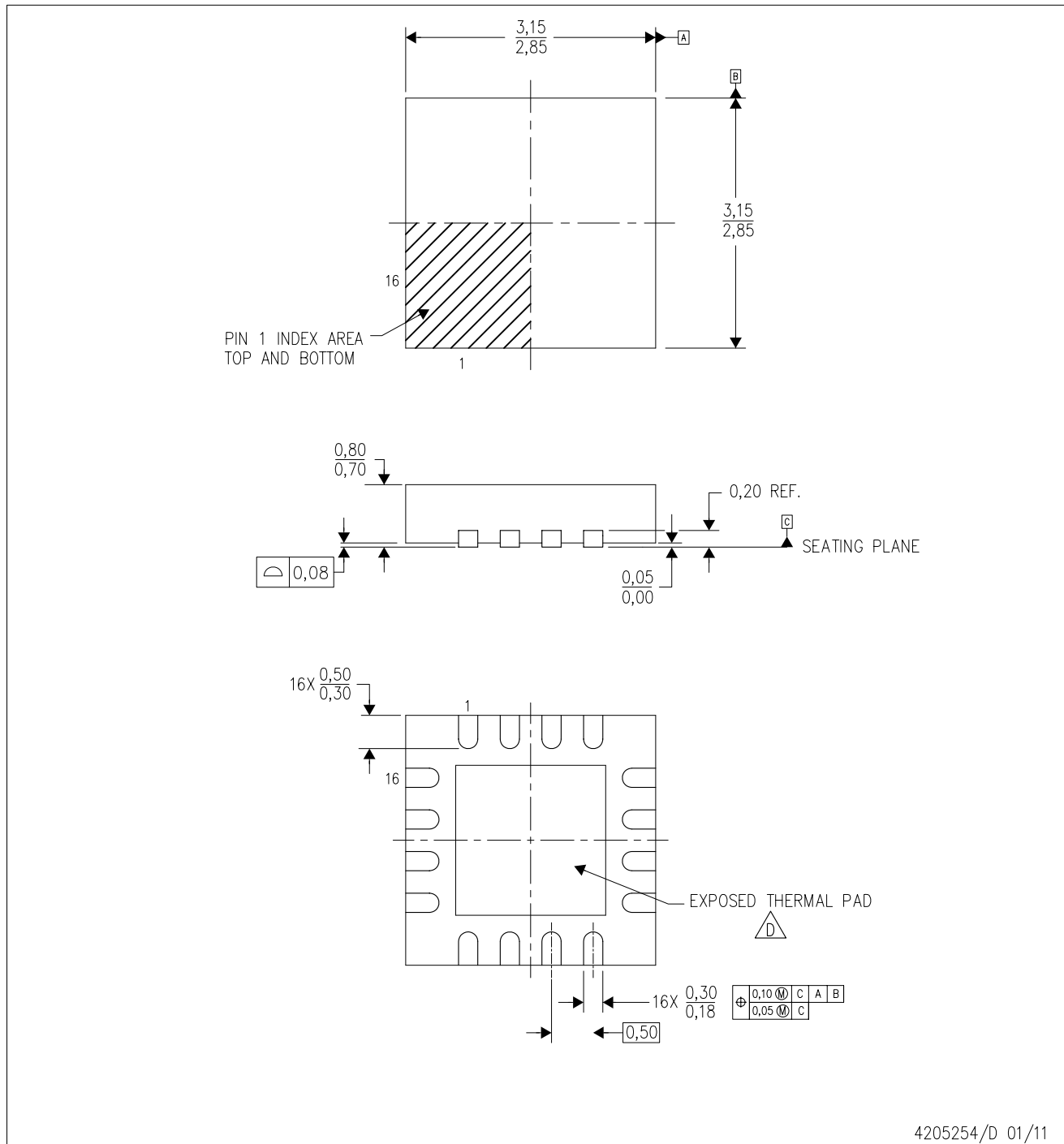


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7250IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7250IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS7850IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS7850IRTET	WQFN	RTE	16	250	210.0	185.0	35.0
ADS8350IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
ADS8350IRTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

RTE (S-PWQFN-N16)

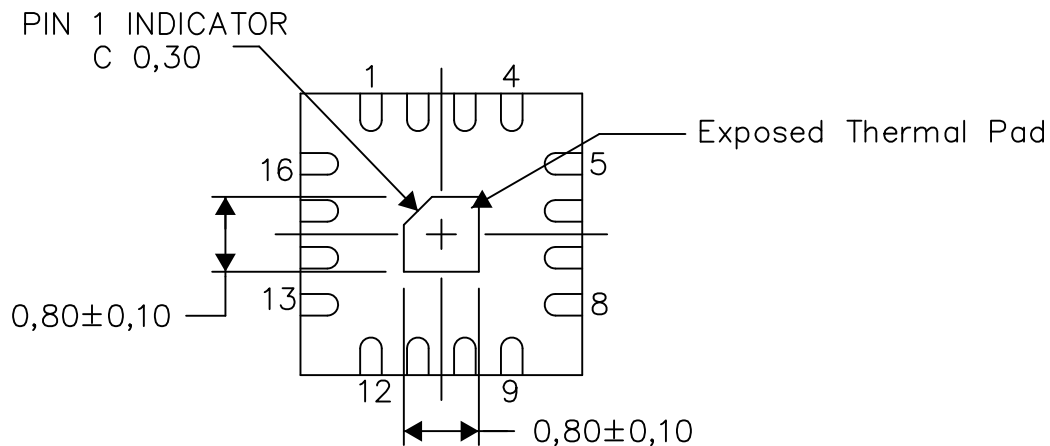
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

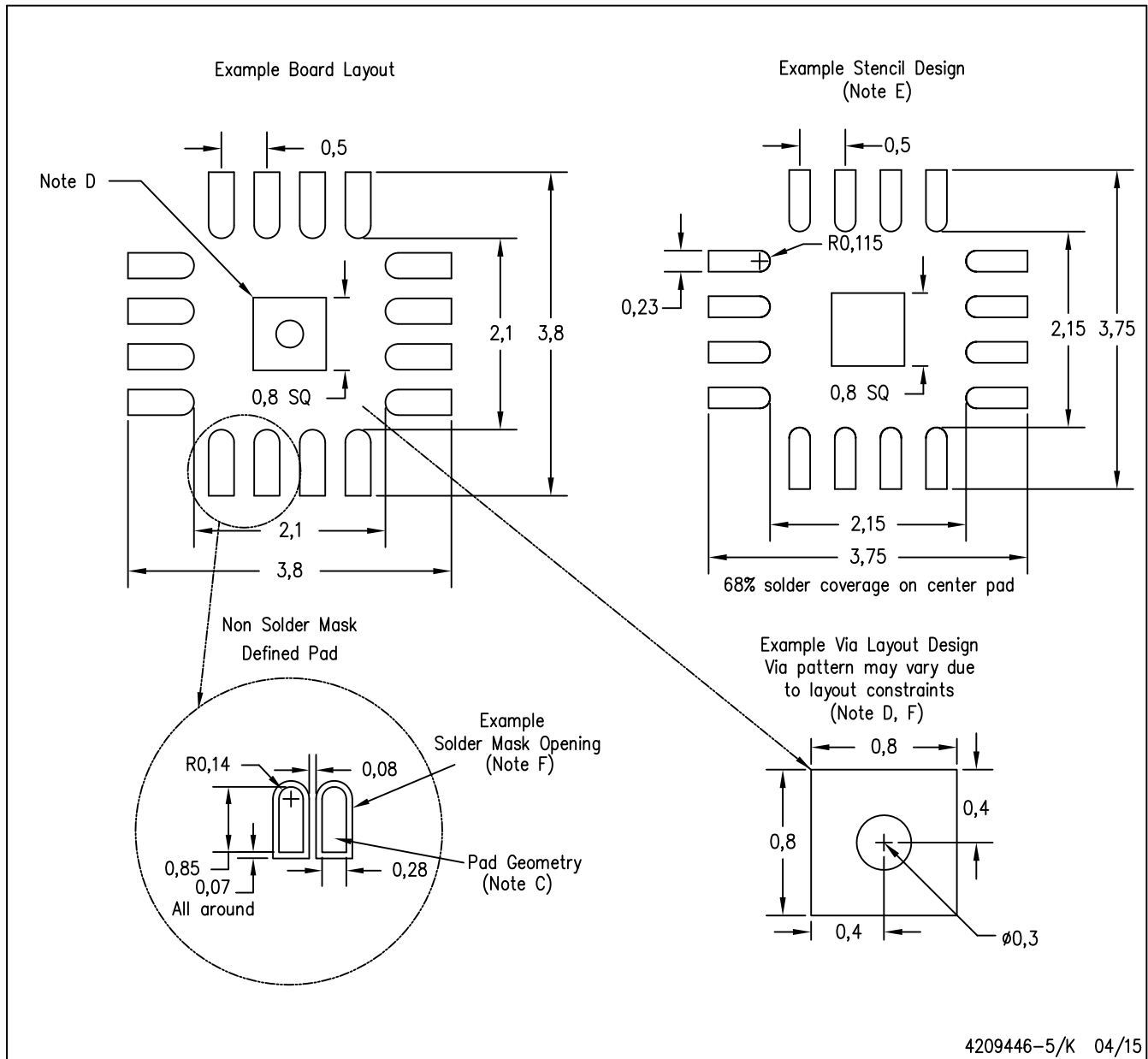
Exposed Thermal Pad Dimensions

4206446-5/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用所用 TI 产品的功能而设计。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与应用 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负任何责任，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准而设计。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理层人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2018 德州仪器半导体技术（上海）有限公司