

# 16-Bit, 500kHz, MicroPower Sampling ANALOG-TO-DIGITAL CONVERTER

Check for Samples: [ADS8322](#)

## FEATURES

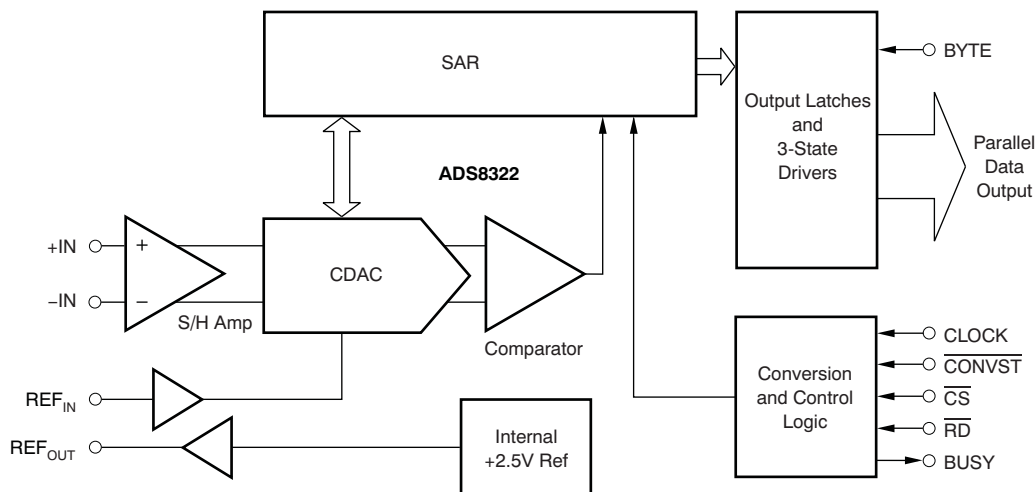
- **HIGH-SPEED PARALLEL INTERFACE**
- **500kHz SAMPLING RATE**
- **LOW POWER: 85mW at 500kHz**
- **INTERNAL 2.5V REFERENCE**
- **UNIPOLAR INPUT RANGE**
- **TQFP-32 PACKAGE**

## APPLICATIONS

- **CT SCANNERS**
- **HIGH-SPEED DATA ACQUISITION**
- **TEST AND INSTRUMENTATION**
- **MEDICAL EQUIPMENT**

## DESCRIPTION

The ADS8322 is a 16-bit, 500kHz analog-to-digital (A/D) converter with an internal 2.5V reference. The device includes a 16-bit capacitor-based successive approximation register (SAR) A/D converter with inherent sample-and-hold. The ADS8322 offers a full 16-bit interface, or an 8-bit option where data are read using two read cycles and eight pins. The ADS8322 is available in a TQFP-32 package and is ensured over the industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

| PRODUCT   | MAXIMUM INTEGRAL LINEARITY ERROR (LSB) | NO MISSING CODES ERROR (LSB) | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | TRANSPORT MEDIA, QUANTITY |
|-----------|----------------------------------------|------------------------------|--------------|--------------------|-----------------------------|-----------------|---------------------------|
| ADS8322Y  | ±8                                     | 14                           | TQFP-32      | PBS                | –40°C to +85°C              |                 | Tape and reel, 250        |
|           |                                        |                              |              |                    |                             |                 | Tape and reel, 2000       |
| ADS8322YB | ±6                                     | 15                           | TQFP-32      | PBS                | –40°C to +85°C              |                 | Tape and reel, 250        |
|           |                                        |                              |              |                    |                             |                 | Tape and reel, 2000       |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

|                                   | ADS8322                               | UNIT |
|-----------------------------------|---------------------------------------|------|
| +IN to GND                        | $V_A + 0.1$                           | V    |
| –IN to GND                        | +0.5                                  | V    |
| $V_A$ to GND                      | –0.3 to +7                            | V    |
| Digital input voltage to GND      | –0.3 to ( $V_A + 0.3$ )               | V    |
| $V_{OUT}$ to GND                  | –0.3 to ( $V_A + 0.3$ )               | V    |
| Operating temperature range       | –40 to +105                           | °C   |
| Storage temperature range         | –65 to +150                           | °C   |
| Junction temperature ( $T_J$ max) | +150                                  | °C   |
| Power dissipation                 | $(T_J \text{ max} - T_A)/\theta_{JA}$ |      |
| $\theta_{JA}$ thermal impedance   | 240                                   | °C/W |

- (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS: +V<sub>A</sub> = +5V**

At –40°C to +85°C, +V<sub>A</sub> = +5V, V<sub>REF</sub> = +2.5V, f<sub>SAMPLE</sub> = 500kHz, and f<sub>CLK</sub> = 20 • f<sub>SAMPLE</sub>, unless otherwise specified.

| PARAMETER                                | TEST CONDITIONS                              | ADS8322Y |       |                      | ADS8322YB <sup>(1)</sup> |       |                      | UNIT                |
|------------------------------------------|----------------------------------------------|----------|-------|----------------------|--------------------------|-------|----------------------|---------------------|
|                                          |                                              | MIN      | TYP   | MAX                  | MIN                      | TYP   | MAX                  |                     |
| RESOLUTION                               |                                              |          |       |                      |                          |       |                      |                     |
| Resolution                               |                                              |          | 16    |                      |                          | 16    |                      | Bits                |
| ANALOG INPUTS                            |                                              |          |       |                      |                          |       |                      |                     |
| Full-scale input span <sup>(2)</sup>     | +IN – (–IN)                                  | 0        |       | +2V <sub>REF</sub>   | 0                        |       | +2V <sub>REF</sub>   | V                   |
| Absolute input range                     | +IN                                          | –0.1     |       | V <sub>A</sub> + 0.1 | –0.1                     |       | V <sub>A</sub> + 0.1 | V                   |
|                                          | –IN                                          | –0.1     |       | +0.5                 | –0.1                     |       | +0.5                 | V                   |
| Capacitance                              |                                              |          | 25    |                      |                          | 25    |                      | pF                  |
| Leakage current                          |                                              |          | ±1    |                      |                          | ±1    |                      | nA                  |
| SYSTEM PERFORMANCE                       |                                              |          |       |                      |                          |       |                      |                     |
| No missing codes                         |                                              | 14       |       |                      | 15                       |       |                      | Bits                |
| Integral linearity error                 |                                              |          | ±4    | ±8                   |                          | ±3    | ±6                   | LSBs <sup>(3)</sup> |
| Offset error                             |                                              |          | ±1.0  | ±2                   |                          | ±0.5  | ±1.0                 | mV                  |
| Gain error <sup>(4)</sup>                |                                              |          | ±0.25 | ±0.50                |                          | ±0.22 | ±0.25                | %FSR                |
| Common-mode rejection ratio              | At dc                                        |          | 70    |                      |                          | 70    |                      | dB                  |
| Noise                                    |                                              |          | 60    |                      |                          | 60    |                      | μV <sub>RMS</sub>   |
| Power-supply rejection ratio             | At FFFFh output code                         |          | ±3    |                      |                          | ±3    |                      | LSBs                |
| SAMPLING DYNAMICS                        |                                              |          |       |                      |                          |       |                      |                     |
| Conversion time                          |                                              |          |       | 1.6                  |                          |       | 1.6                  | μs                  |
| Acquisition time                         |                                              | 350      |       |                      | 350                      |       |                      | ns                  |
| Throughput rate                          |                                              |          |       | 500                  |                          |       | 500                  | kHz                 |
| Aperture delay                           |                                              |          | 50    |                      |                          | 50    |                      | ns                  |
| Aperture jitter                          |                                              |          | 20    |                      |                          | 20    |                      | ps                  |
| Small-signal bandwidth                   |                                              |          | 30    |                      |                          | 30    |                      | MHz                 |
| Step response                            |                                              |          | 100   |                      |                          | 100   |                      | ns                  |
| DYNAMIC CHARACTERISTICS                  |                                              |          |       |                      |                          |       |                      |                     |
| Total harmonic distortion <sup>(5)</sup> | V <sub>IN</sub> = 5V <sub>PP</sub> at 100kHz |          | –90   |                      |                          | –93   |                      | dB                  |
| SINAD                                    | V <sub>IN</sub> = 5V <sub>PP</sub> at 100kHz |          | 81    |                      |                          | 83    |                      | dB                  |
| Spurious free dynamic range              | V <sub>IN</sub> = 5V <sub>PP</sub> at 100kHz |          | 94    |                      |                          | 96    |                      | dB                  |
| REFERENCE OUTPUT                         |                                              |          |       |                      |                          |       |                      |                     |
| Voltage                                  | I <sub>OUT</sub> = 0                         | 2.475    | 2.50  | 2.525                | 2.48                     | 2.50  | 2.52                 | V                   |
| Source current                           | Static load                                  |          |       | 10                   |                          |       | 10                   | μA                  |
| Drift                                    | I <sub>OUT</sub> = 0                         |          | 20    |                      |                          | 20    |                      | ppm/°C              |
| Line regulation                          | 4.75V ≤ V <sub>CC</sub> ≤ 5.25V              |          | 0.6   |                      |                          | 0.6   |                      | mV                  |
| REFERENCE INPUT                          |                                              |          |       |                      |                          |       |                      |                     |
| Range                                    |                                              | 1.5      |       | 2.55                 | 1.5                      |       | 2.55                 | V                   |
| Resistance <sup>(6)</sup>                | To internal reference voltage                |          | 10    |                      |                          | 10    |                      | kΩ                  |

(1) Shaded cells indicate different specifications from ADS8322Y.

(2) Ideal input span; does not include gain or offset error.

(3) LSB means least significant bit, with V<sub>REF</sub> equal to +2.5V; 1LSB = 76μV.

(4) Measured relative to an ideal, full-scale input [+IN – (–IN)] of 4.9999V. Thus, gain error includes the error of the internal voltage reference.

(5) Calculated on the first nine harmonics of the input frequency.

(6) Can vary ±30%.

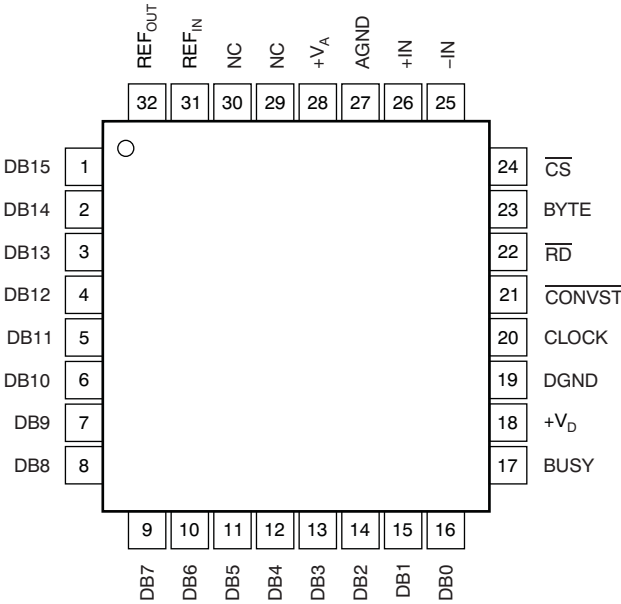
**ELECTRICAL CHARACTERISTICS: +V<sub>A</sub> = +5V (continued)**

At –40°C to +85°C, +V<sub>A</sub> = +5V, V<sub>REF</sub> = +2.5V, f<sub>SAMPLE</sub> = 500kHz, and f<sub>CLK</sub> = 20 • f<sub>SAMPLE</sub>, unless otherwise specified.

| PARAMETER                   | TEST CONDITIONS               | ADS8322Y        |      |                 | ADS8322YB <sup>(1)</sup> |      |                 | UNIT |
|-----------------------------|-------------------------------|-----------------|------|-----------------|--------------------------|------|-----------------|------|
|                             |                               | MIN             | TYP  | MAX             | MIN                      | TYP  | MAX             |      |
| DIGITAL INPUT/OUTPUT        |                               |                 |      |                 |                          |      |                 |      |
| Logic family                |                               |                 | CMOS |                 |                          | CMOS |                 |      |
| Logic levels:               |                               |                 |      |                 |                          |      |                 |      |
| V <sub>IH</sub>             | I <sub>IH</sub> ≤ +5μA        | 3.0             |      | +V <sub>A</sub> | 3.0                      |      | +V <sub>A</sub> | V    |
| V <sub>IL</sub>             | I <sub>IL</sub> ≤ +5μA        | −0.3            |      | 0.8             | −0.3                     |      | 0.8             | V    |
| V <sub>OH</sub>             | I <sub>OH</sub> = 2 TTL Loads | 4.0             |      |                 | 4.0                      |      |                 | V    |
| V <sub>OL</sub>             | I <sub>OH</sub> = 2 TTL Loads |                 |      | 0.4             |                          |      | 0.4             | V    |
| Data format                 |                               | Straight binary |      |                 | Straight binary          |      |                 |      |
| POWER-SUPPLY REQUIREMENTS   |                               |                 |      |                 |                          |      |                 |      |
| Power-supply voltage        |                               |                 |      |                 |                          |      |                 |      |
| +V <sub>A</sub>             |                               | 4.75            | 5    | 5.25            | 4.75                     | 5    | 5.25            | V    |
| +V <sub>D</sub>             |                               | 4.75            | 5    | 5.25            | 4.75                     | 5    | 5.25            | V    |
| Supply current              | f <sub>SAMPLE</sub> = 500kHz  |                 | 17   | 25              |                          | 17   | 25              | mA   |
| Power dissipation           | f <sub>SAMPLE</sub> = 500kHz  |                 | 85   | 125             |                          | 85   | 125             | mW   |
| TEMPERATURE RANGE           |                               |                 |      |                 |                          |      |                 |      |
| Specified temperature range |                               | −40             |      | +85             | −40                      |      | +85             | °C   |

**DEVICE INFORMATION**

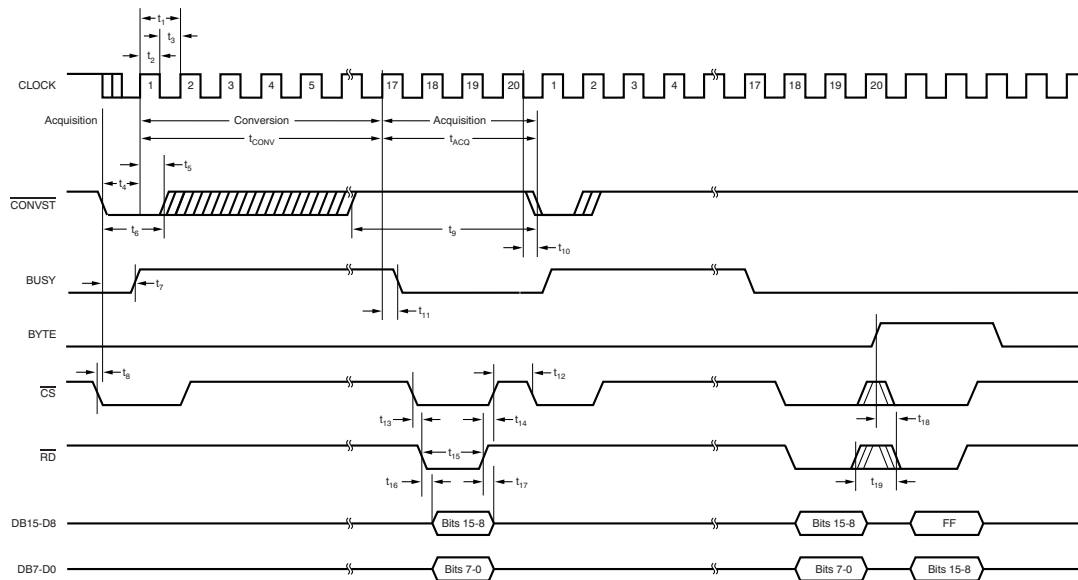
**PBS PACKAGE  
TQFP-32  
(TOP VIEW)**



## PIN ASSIGNMENTS

| TERMINAL |                            | DESCRIPTION                                                                                                                      |
|----------|----------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| NO       | NAME                       |                                                                                                                                  |
| 1        | DB15                       | Data Bit 15 (MSB)                                                                                                                |
| 2        | DB14                       | Data Bit 14                                                                                                                      |
| 3        | DB13                       | Data Bit 13                                                                                                                      |
| 4        | DB12                       | Data Bit 12                                                                                                                      |
| 5        | DB11                       | Data Bit 11                                                                                                                      |
| 6        | DB10                       | Data Bit 10                                                                                                                      |
| 7        | DB9                        | Data Bit 9                                                                                                                       |
| 8        | DB8                        | Data Bit 8                                                                                                                       |
| 9        | DB7                        | Data Bit 7                                                                                                                       |
| 10       | DB6                        | Data Bit 6                                                                                                                       |
| 11       | DB5                        | Data Bit 5                                                                                                                       |
| 12       | DB4                        | Data Bit 4                                                                                                                       |
| 13       | DB3                        | Data Bit 3                                                                                                                       |
| 14       | DB2                        | Data Bit 2                                                                                                                       |
| 15       | DB1                        | Data Bit 1                                                                                                                       |
| 16       | DB0                        | Data Bit 0 (LSB)                                                                                                                 |
| 17       | BUSY                       | High when a conversion is in progress.                                                                                           |
| 18       | V <sub>D</sub> +           | Digital Power Supply, +5VDC.                                                                                                     |
| 19       | DGND                       | Digital Ground                                                                                                                   |
| 20       | CLOCK                      | An external CMOS-compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source. |
| 21       | $\overline{\text{CONVST}}$ | Convert Start                                                                                                                    |
| 22       | $\overline{\text{RD}}$     | Synchronization pulse for the parallel output.                                                                                   |
| 23       | BYTE                       | Selects eight most significant bits (low) or eight least significant bits (high). Data valid on pins 9-16.                       |
| 24       | $\overline{\text{CS}}$     | Chip Select                                                                                                                      |
| 25       | –IN                        | Inverting Input Channel                                                                                                          |
| 26       | +IN                        | Noninverting Input Channel                                                                                                       |
| 27       | AGND                       | Analog Ground                                                                                                                    |
| 28       | +V <sub>A</sub>            | Analog Power Supply, +5VDC.                                                                                                      |
| 29       | NC                         | No connection                                                                                                                    |
| 30       | NC                         | No connection                                                                                                                    |
| 31       | REF <sub>IN</sub>          | Reference Input. When using the internal 2.5V reference, tie this pin directly to REF <sub>OUT</sub> .                           |
| 32       | REF <sub>OUT</sub>         | Reference Output. A 0.1μF capacitor should be connected to this pin when the internal reference is used.                         |

## TIMING INFORMATION



## TIMING CHARACTERISTICS<sup>(1)(2)</sup>

All specifications typical at  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+V_D = +5\text{V}$ .

| PARAMETER         |                                                              | TEST CONDITIONS | ADS8322 |     |     | UNIT          |
|-------------------|--------------------------------------------------------------|-----------------|---------|-----|-----|---------------|
|                   |                                                              |                 | MIN     | TYP | MAX |               |
| $t_{\text{CONV}}$ | Conversion Time                                              |                 |         |     | 1.6 | $\mu\text{s}$ |
| $t_{\text{AQC}}$  | Acquisition Time                                             |                 | 350     |     |     | ns            |
| $t_1$             | CLOCK Period                                                 |                 | 100     |     |     | ns            |
| $t_2$             | CLOCK High Time                                              |                 | 40      |     |     | ns            |
| $t_3$             | CLOCK Low Time                                               |                 | 40      |     |     | ns            |
| $t_4$             | $\overline{\text{CONVST}}$ Low to Clock High                 |                 | 10      |     |     | ns            |
| $t_5$             | CLOCK High to $\overline{\text{CONVST}}$ High                |                 | 5       |     |     | ns            |
| $t_6$             | $\overline{\text{CONVST}}$ Low Time                          |                 | 20      |     |     | ns            |
| $t_7$             | $\overline{\text{CONVST}}$ Low to BUSY High                  |                 |         |     | 25  | ns            |
| $t_8$             | $\overline{\text{CS}}$ Low to $\overline{\text{CONVST}}$ Low |                 | 0       |     |     | ns            |
| $t_9$             | $\overline{\text{CONVST}}$ High                              |                 | 20      |     |     | ns            |
| $t_{10}$          | CLOCK Low to $\overline{\text{CONVST}}$ Low                  |                 | 0       |     |     | ns            |
| $t_{11}$          | CLOCK High to BUSY Low                                       |                 |         |     | 25  | ns            |
| $t_{12}$          | $\overline{\text{CS}}$ High                                  |                 | 0       |     |     | ns            |
| $t_{13}$          | $\overline{\text{CS}}$ Low to $\overline{\text{RD}}$ Low     |                 | 0       |     |     | ns            |
| $t_{14}$          | $\overline{\text{RD}}$ High to $\overline{\text{CS}}$ High   |                 | 0       |     |     | ns            |
| $t_{15}$          | $\overline{\text{RD}}$ Low Time                              |                 | 50      |     |     | ns            |
| $t_{16}$          | $\overline{\text{RD}}$ Low to Data Valid                     |                 | 40      |     |     | ns            |
| $t_{17}$          | Data Hold from $\overline{\text{RD}}$ High                   |                 | 5       |     |     | ns            |
| $t_{18}$          | BYTE Change to $\overline{\text{RD}}$ Low <sup>(3)</sup>     |                 | 0       |     |     | ns            |
| $t_{19}$          | $\overline{\text{RD}}$ High Time                             |                 | 20      |     |     | ns            |

(1) All input signals are specified with  $t_R = t_F = 5\text{ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

(2) See timing diagram, above.

(3) BYTE is asynchronous; when BYTE is 0, bits 15 through 0 appear at DB15-DB0. When BUSY is 1, bits 15 through 8 appear on DB7-DB0.  $\overline{\text{RD}}$  may remain low between changes in BYTE.

## TYPICAL CHARACTERISTICS

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+V_A = +5\text{V}$ ,  $V_{\text{REF}} = +2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ , and  $f_{\text{CLK}} = 20 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.

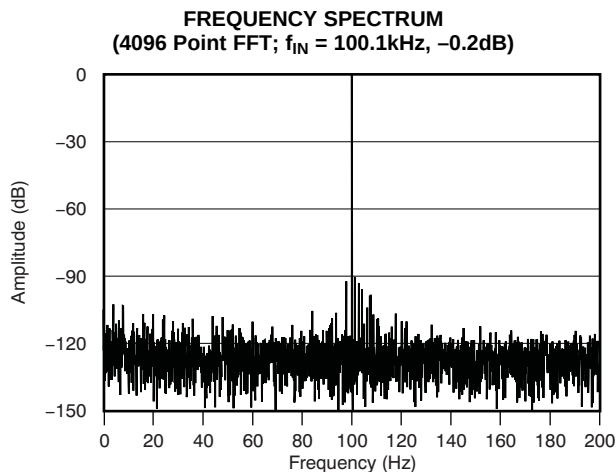


Figure 1.

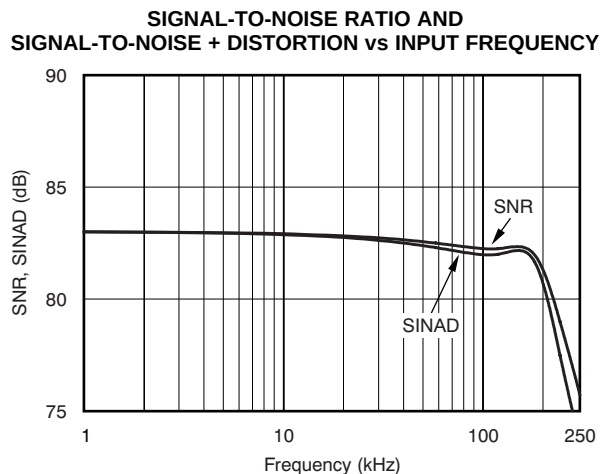


Figure 2.

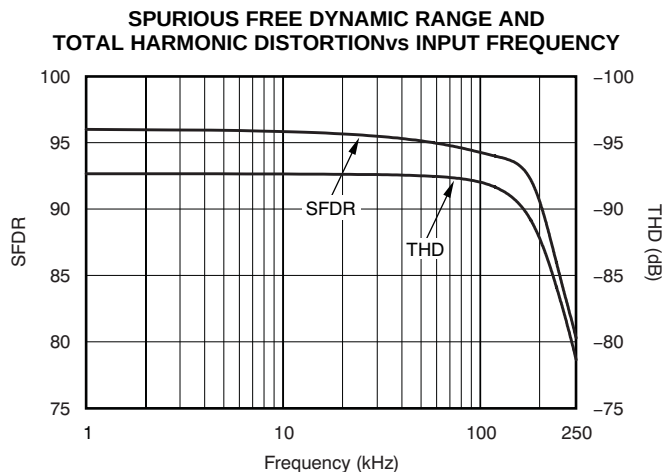


Figure 3.

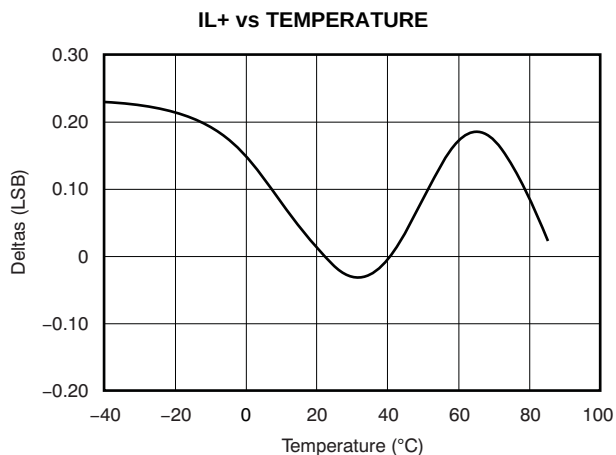


Figure 4.

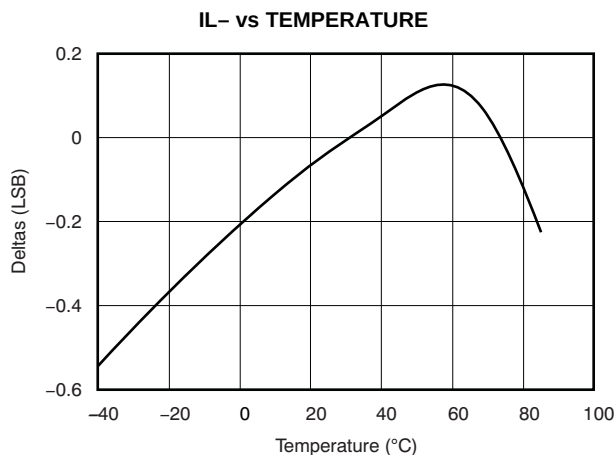


Figure 5.

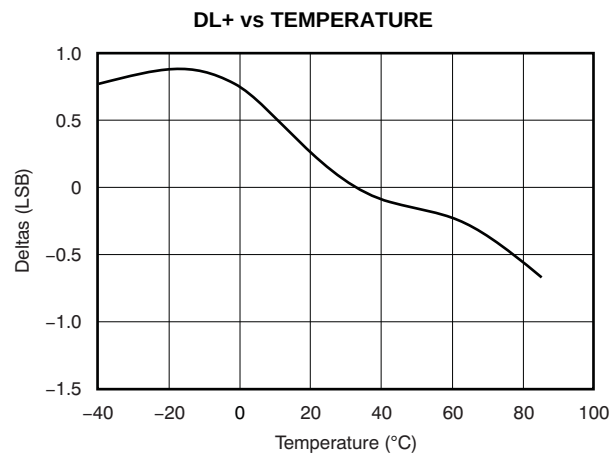
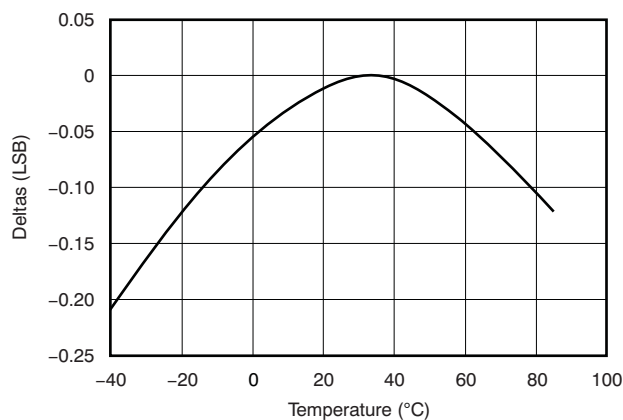


Figure 6.

## TYPICAL CHARACTERISTICS (continued)

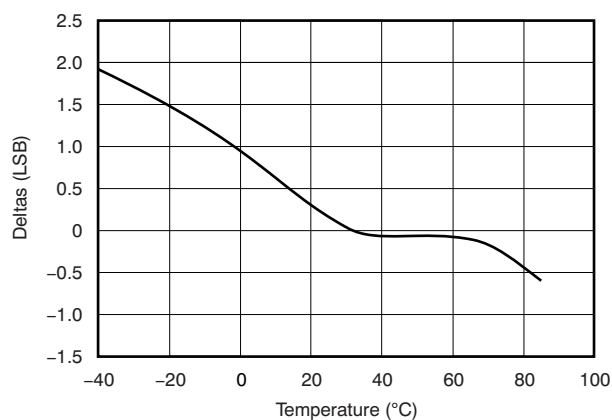
At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+V_A = +5\text{V}$ ,  $V_{\text{REF}} = +2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kHz}$ , and  $f_{\text{CLK}} = 20 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.

**DL- vs TEMPERATURE**



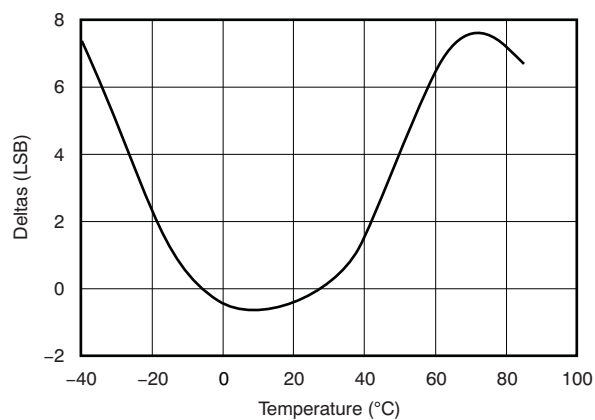
**Figure 7.**

**OFFSET ERROR vs TEMPERATURE**



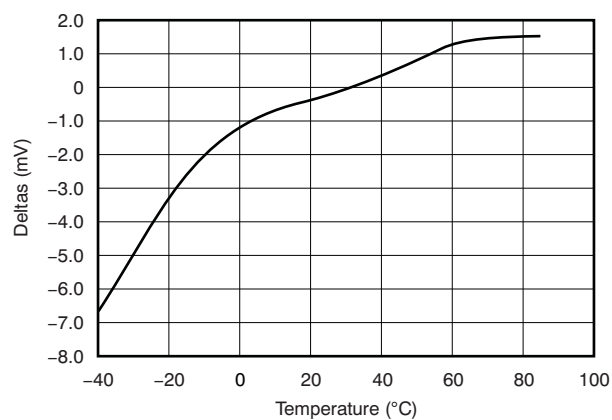
**Figure 8.**

**GAIN ERROR vs TEMPERATURE**



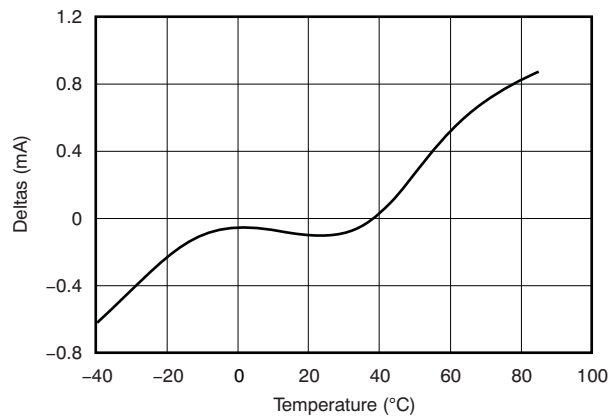
**Figure 9.**

**$V_{\text{REF}}$  vs TEMPERATURE**



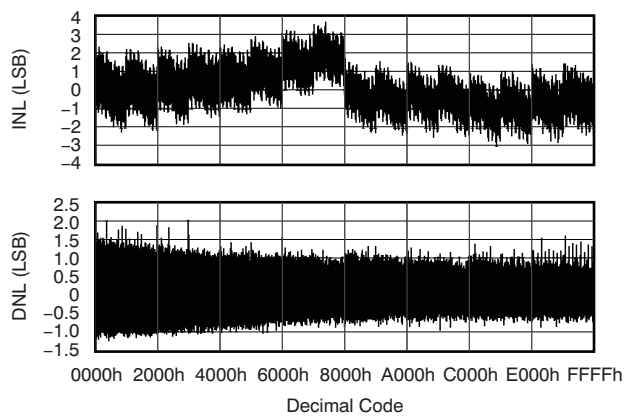
**Figure 10.**

**$I_Q$  vs TEMPERATURE**



**Figure 11.**

**LINEARITY ERROR AND  
DIFFERENTIAL LINEARITY ERROR vs CODE**



**Figure 12.**

## THEORY OF OPERATION

The ADS8322 is a high-speed successive approximation register (SAR) A/D converter with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution, which inherently includes a sample-and-hold function. The basic operating circuit for the ADS8322 is shown in Figure 13.

The ADS8322 requires an external clock to run the conversion process. The clock can be run continuously or it can be gated to conserve power between conversions. This clock can vary between 25kHz (1.25kHz throughput) and 10MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW

times are at least 40ns and the clock period is at least 100ns. The minimum clock frequency is governed by the parasitic leakage of the capacitive digital-to-analog (CDAC) capacitors internal to the ADS8322.

The analog input is provided to two input pins, +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

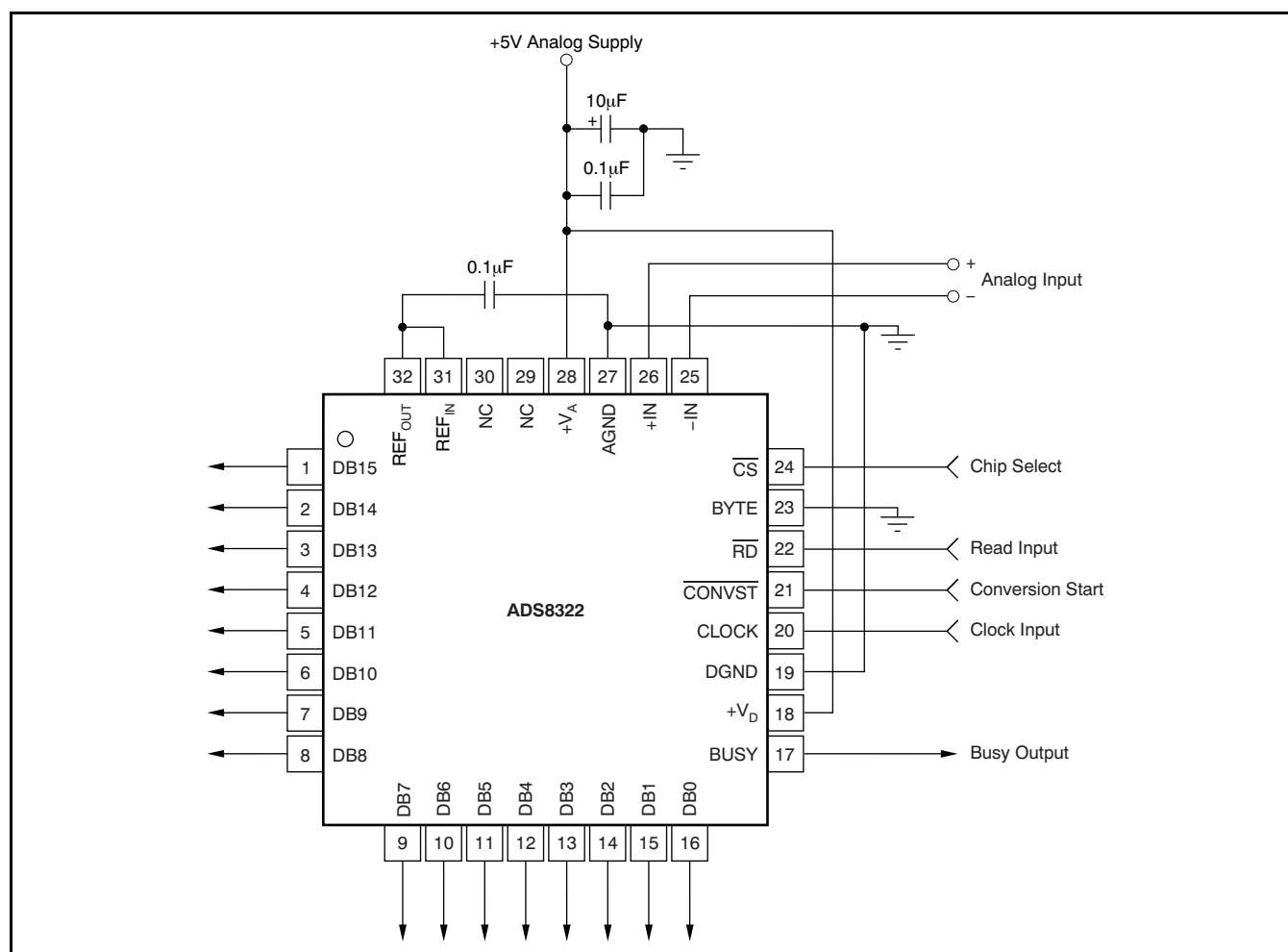


Figure 13. Typical Circuit Configuration

## REFERENCE

Under normal operation, the REF<sub>OUT</sub> pin should be directly connected to the REF<sub>IN</sub> pin to provide an internal +2.5V reference to the ADS8322. The ADS8322 can operate, however, with an external reference in the range of 1.5V to 2.6V for a corresponding full-scale range of 3.0V to 5.2V.

The internal reference of the ADS8322 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to the REF<sub>OUT</sub> pin (the internal reference can typically source and sink 10μA of current). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the CDAC capacitors during conversion.

## ANALOG INPUT

When the converter enters the Hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.1V and 0.5V, allowing the input to reject small signals which are common to both the +IN and –IN inputs. The +IN input has a range of –0.1V to +V<sub>A</sub> + 0.1V.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8322 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25pF) to a 16-bit settling level within the acquisition time (400ns) of the device. When the converter goes into Hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –IN input should not drop below GND – 100mV or exceed GND + 0.5V. The +IN input should always remain within the range of GND – 100mV to V<sub>A</sub> + 100mV. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low-bandwidth input signals with low-pass filters should be used.

## DIGITAL INTERFACE

### TIMING AND CONTROL

See the [timing diagram](#) and the [Timing Characteristics](#) section for detailed information on timing signals and the respective requirements for each.

The ADS8322 uses an external clock (CLOCK) which controls the conversion rate of the CDAC. With a 10MHz external clock, the A/D converter sampling rate is 500kHz, which corresponds to a 2μs maximum throughput time.

Conversions are initiated by bringing the CONVST pin low for a minimum of 20ns (after the 20ns minimum requirement has been met, the CONVST pin can be brought high), while CS is low. The ADS8322 switches from Sample-to-Hold mode on the falling edge of the CONVST command. Following the first rising edge of the external clock after a CONVST low, the ADS8322 begins conversion (this first rising edge of the external clock represents the start of clock cycle one; the ADS8322 requires 16 rising clock edges to complete a conversion). The BUSY output goes high immediately following CONVST going low. BUSY stays high through the conversion process and returns low when the conversion has ended.

Both RD and CS can be high during and before a conversion (although CS must be low when CONVST goes low to initiate a conversion). Both the RD and CS pins are brought low in order to enable the parallel output bus with the conversion.

## READING DATA

The ADS8322 outputs full parallel data in Straight Binary format, as shown in [Table 1](#). The parallel output is active when CS and RD are both LOW. The output data should not be read 125ns before the falling edge of CONVST and 10ns after the falling edge. Any other combination of CS and RD will 3-state the parallel output. Refer to [Table 1](#) for ideal output codes.

**Table 1. Ideal Input Voltages and Output Codes**

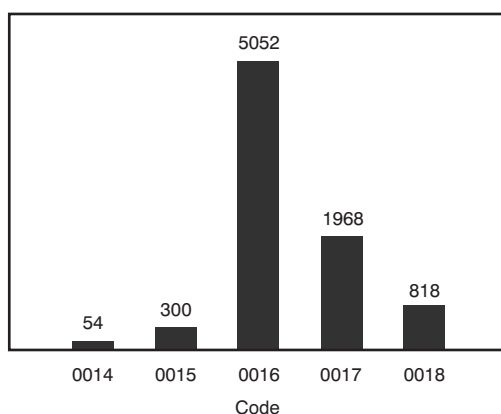
| DESCRIPTION                 | ANALOG VALUE               | DIGITAL OUTPUT STRAIGHT BINARY |          |
|-----------------------------|----------------------------|--------------------------------|----------|
| Full-Scale Range            | $2 \cdot V_{REF}$          | BINARY CODE                    | HEX CODE |
| Least Significant Bit (LSB) | $2 \cdot V_{REF}/65535$    |                                |          |
| +Full Scale                 | $2V_{REF} - 1 \text{ LSB}$ | 1111 1111<br>1111 1111         | FFFF     |
| Midscale                    | $V_{REF}$                  | 1000 0000<br>0000 0000         | 8000     |
| Midscale – LSB              | $V_{REF} - 1 \text{ LSB}$  | 0111 1111<br>1111 1111         | 7FFF     |
| Zero                        | 0                          | 0000 0000<br>0000 0000         | 0000     |

## BYTE

The output data appear as a full 16-bit word on DB15- DB0 (MSB-LSB), if BYTE is low. The result may also be read on an 8-bit bus by using only DB7-DB0. In this case two reads are necessary. The first read proceeds as before, leaving BYTE low and reading the eight least significant bits on DB7-DB0, then bringing BYTE high. When BYTE is high, the upper eight bits (D15-D8) appear on DB7-DB0.

## NOISE

Figure 14 shows the transition noise of the ADS8322. A low-level dc input was applied to the analog input pins and the converter was put through 8,192 conversions. The digital output of the A/D converter varies in output code due to the internal noise of the ADS8322. This characteristic is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped, with the peak of the bell curve representing the nominal code for the input value. The  $\pm 1\sigma$ ,  $\pm 2\sigma$ , and  $\pm 3\sigma$  distributions respectively represent the 68.3%, 95.5%, and 99.7% of all codes. The transition noise can be calculated by dividing the number of codes measured by six; this yields the  $\pm 3\sigma$  distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1,000 conversions. The ADS8322, with five output codes for the  $\pm 3\sigma$  distribution, yields a  $< \pm 0.8\text{LSB}$  transition noise at 5V operation. Remember that to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be  $< 50\mu\text{V}$ .



**Figure 14. Histogram of 8,192 Conversions of a Low-Level DC Input**

## AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of  $1/\sqrt{n}$ , where  $n$  is the number of averages. For example, averaging four conversion results reduces the transition noise by 1/2 to  $\pm 0.25\text{LSBs}$ . Averaging should only be used for input signals with frequencies near dc.

For ac signals, a digital filter can be used to low-pass filter and decimate the output codes. This configuration works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio improves by 3dB.

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8322 circuitry. This consideration is particularly true if the CLOCK input is approaching the maximum throughput rate.

As the ADS8322 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just before latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are  $n$  windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, or nearby digital logic or high-power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event changes in time with respect to the CLOCK input.

On average, the ADS8322 draws very little current from an external reference, as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation.

The AGND and DGND pins should be connected to a clean ground point. In all cases, this point should be the *analog* ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

As with the GND connections,  $V_{DD}$  should be connected to a +5V power supply plane, or trace, that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8322 should be clean and well-bypassed. A 0.1μF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1μF to 10μF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor, or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (July, 2001) to Revision A                                                          | Page |
|-----------------------------------------------------------------------------------------------------------|------|
| • Updated document format to current standards .....                                                      | 1    |
| • Deleted <i>lead temperature</i> specifications from Absolute Maximum Ratings table .....                | 2    |
| • Changed acquisition time specification from .4μs (max) to 350ns (min) .....                             | 3    |
| • Changed acquisition time specification from .4μs (max) to 350ns (min) .....                             | 6    |
| • Added <a href="#">Figure 12</a> , <i>Linearity Error and Differential Linearity Error vs Code</i> ..... | 8    |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ADS8322Y/250     | ACTIVE        | TQFP         | PBS                | 32   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | B22Y                    | <a href="#">Samples</a> |
| ADS8322Y/2K      | ACTIVE        | TQFP         | PBS                | 32   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | B22Y                    | <a href="#">Samples</a> |
| ADS8322YB/250    | ACTIVE        | TQFP         | PBS                | 32   | 250            | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-3-260C-168 HR  | -40 to 85    | B22Y<br>B               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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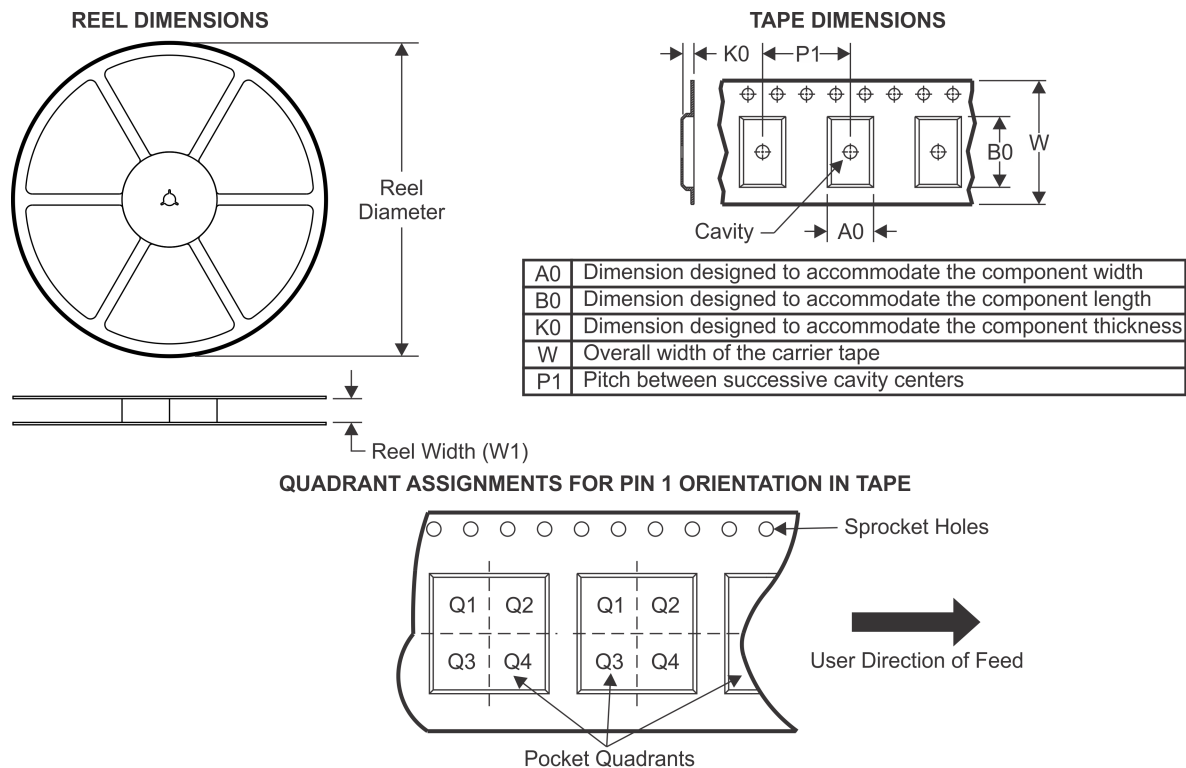
www.ti.com

## PACKAGE OPTION ADDENDUM

24-Aug-2018

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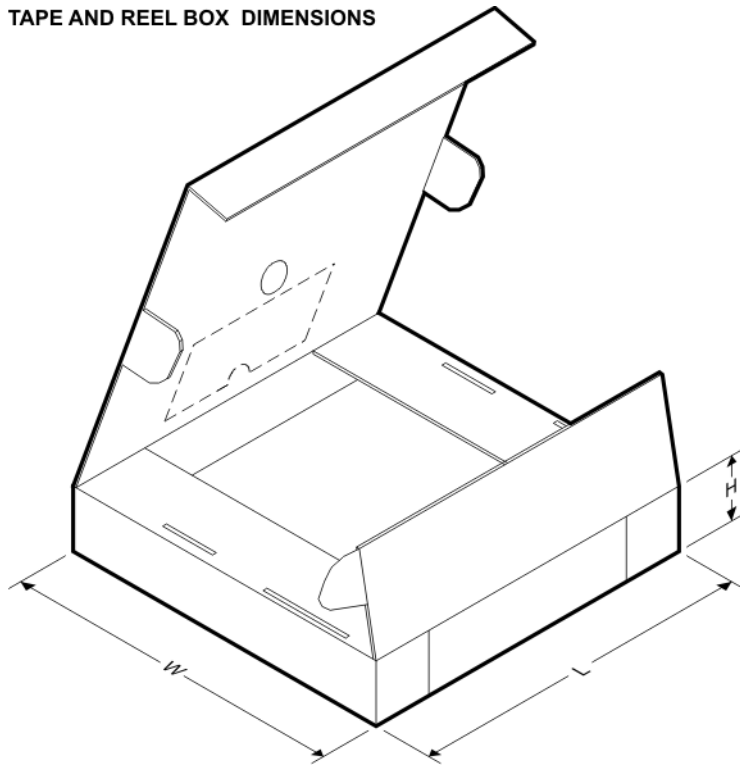
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS8322Y/250  | TQFP         | PBS             | 32   | 250  | 180.0              | 16.4               | 7.2     | 7.2     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS8322Y/2K   | TQFP         | PBS             | 32   | 2000 | 330.0              | 16.4               | 7.2     | 7.2     | 1.5     | 12.0    | 16.0   | Q2            |
| ADS8322YB/250 | TQFP         | PBS             | 32   | 250  | 180.0              | 16.4               | 7.2     | 7.2     | 1.5     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS

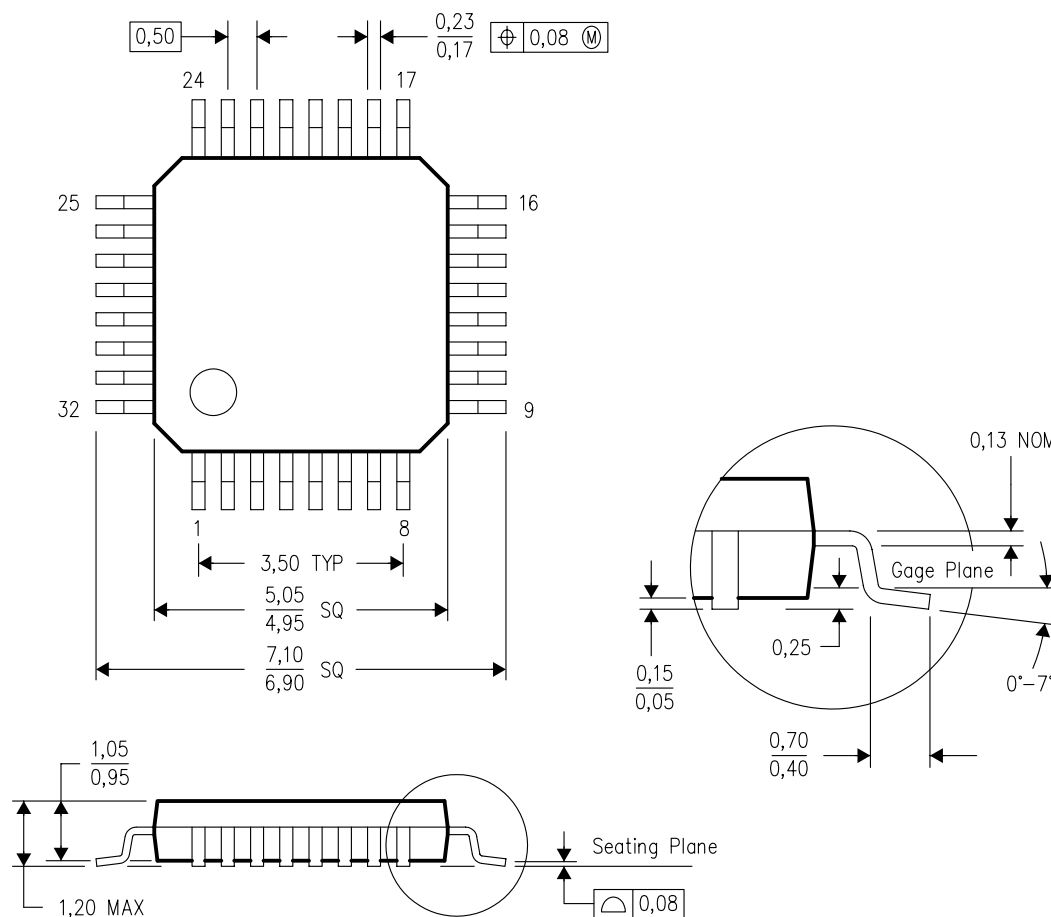


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS8322Y/250  | TQFP         | PBS             | 32   | 250  | 213.0       | 191.0      | 55.0        |
| ADS8322Y/2K   | TQFP         | PBS             | 32   | 2000 | 350.0       | 350.0      | 43.0        |
| ADS8322YB/250 | TQFP         | PBS             | 32   | 250  | 213.0       | 191.0      | 55.0        |

PBS (S-PQFP-G32)

## PLASTIC QUAD FLATPACK



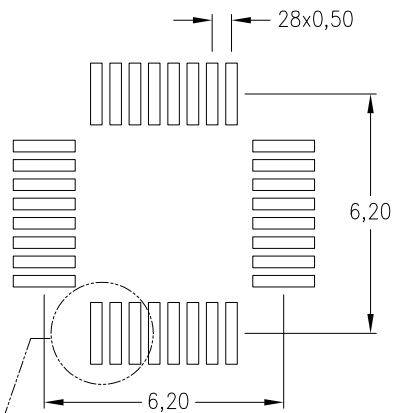
4087735/B 07/05

- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.

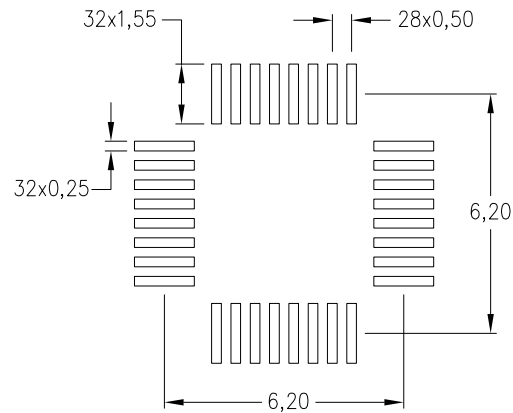
PBS (S-PQFP-G32)

PLASTIC QUAD FLATPACK

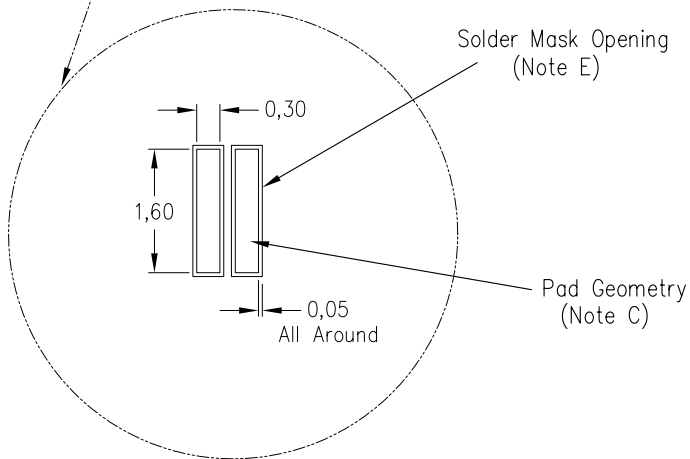
Example Board Layout  
(Note C)



0,127mm Thick Stencil Design Example  
(Note D)



Non Solder Mask  
Defined Pad



4212229/A 10/11

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - E. Customers should contact their board fabrication site for recommended solder mask tolerances between and around signal pads.

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