MSP432P411xT、MSP432P401xT SimpleLink™ 混合信号微控制器

1 器件概述

1.1 特性

- 内核
  - Arm®32 位 Cortex®-M4F CPU，具有浮点单元和内存保护单元
  - 频率高达 24MHz
  - 性能基准
    - 3.41 CoreMark/MHz
    - 1.196 DMIPS/MHz (Dhrystone 2.1)
- 高级低功耗模拟 特性
  - 具有 16 位精度和高达 500ksps 速率的 SAR 模数转换器 (ADC)
  - 内部电压基准，典型温漂为 25ppm/°C
  - 两个模拟比较器
  - 具有高达 320 段对比度控制的集成 LCD 驱动器
- 存储器
  - 高达 2048KB 的闪存主存储器（分为两组，支持在擦除期间同时读取或执行）
  - 32KB 的闪存信息存储器（包括用于 BSL、TLV 和闪存邮箱的区域）
  - 高达 256KB 的 SRAM（包括 8KB 的备用存储器）
  - 2KB 的实用程序 SRAM
  - 32KB 的 ROM，具有 MSP432™外设驱动程序库
- 超低功耗工作模式
  - 工作状态：100µA/MHz
  - 低频工作状态：96µA（128kHz 时）
  - LPM3（带 RTC）：14.4µA（典型值）
  - LPM3.5（带 RTC）：10.5µA（典型值）
  - LPM4：14µA（典型值）
  - LPM4.5：24nA
- SimpleLink™ 平台
  - 支持低功耗 *Bluetooth*®、 Wi-Fi®以及低于 1GHz
  - 单一开发环境
  - 在 SimpleLink SDK 上实现 100% 代码重复使用
- 工作特性
  - 宽电源电压范围：1.62V 至 3.7V
  - 环境温度范围：–40°C 至 105°C
- 灵活的时钟 特性
  - 可编程的内部 DCO（高达 24MHz）
  - 32.768kHz 低频晶振支持 (LFXT)
  - 高达 24MHz 的高频晶振支持 (HFXT)
  - 低频调整内部基准振荡器 (REFO)
  - 极低功耗低频内部振荡器 (VLO)
  - 模块振荡器 (MODOSC)
  - 系统振荡器 (SYSOSC)
- 代码安全性 特性
  - JTAG 和 SWD 锁
  - IP 保护（多达四个安全闪存区，每个都可配置起始地址和大小）
- 增强型系统选项
  - 可编程的电源电压监控功能
  - 多类复位功能，可实现对应用和调试的更好控制
  - 8 通道 DMA
  - 具有日历和报警功能的实时时钟 (RTC)
- 计时和控制
  - 多达四个 16 位计时器，每个都具有多达五个捕获、比较和 PWM 功能
  - 两个 32 位计时器，每个都具有中断生成功能
- 串行通信
  - 多达四个 eUSCI_A 模块
    - 支持自动波特率检测的 UART
    - IrDA 编码和解码
    - SPI（高达 8Mbps）
  - 多达四个 eUSCI_B 模块
    - I^2C（支持多从器件寻址）
    - SPI（高达 8Mbps）
- 灵活的 I/O 特性
  - 超低漏电 I/O（最大值为 ±30nA）
  - 所有 I/O 均具备电容式触控功能
  - 多达 48 个具有中断和唤醒功能的 I/O
  - 多达 24 个具有端口映射功能的 I/O
  - 八个具有干扰滤波功能的 I/O
- 加密和数据完整性加速器
  - 128 位、192 位或 256 位 AES 加密和解密加速器
  - 32 位硬件 CRC 引擎

- JTAG 和调试支持
  - 支持 4 引脚 JTAG 和 2 引脚 SWD 调试接口
  - 支持串行线迹
  - 支持电源调试和 应用评测

1.2 应用

- 计量
  - 流量计
  - 电表
  - 故障探测器
  - 现场发送器
- 楼宇自动化
  - 恒温器
  - 安全系统
  - 烟雾探测器
  - 门禁面板
- 工厂自动化
  - 无线电源监控器
  - 故障预警传感器
  - 现场发送器
  - 基础现场总线
- 健康与健身
  - 健康监控器
  - 健身附件
  - 血糖仪

1.3 说明

SimpleLink MSP432P411xT 和 MSP432P401xT 微控制器 (MCU) 是具有集成式 16 位精密 ADC 的优化型无线主机 MCU，可借助 FPU 和 DSP 扩展提供超低功耗性能，其中包括 100µA/MHz 的工作功耗和 14.4µA 的待机功耗。作为优化的无线主机 MCU，MSP432P411xT 和 MSP432P401xT 可让开发人员向 基于 SimpleLink 无线连接解决方案的应用中添加高精度模拟和存储器扩展。

MSP432P411xT 和 MSP432P401xT 器件是 SimpleLink MCU 平台的一部分，包含 Wi-Fi、低功耗蓝牙、低于 1GHz和主机 MCU。它们均共用一个通用、简单易用的开发环境，其中包含单核软件开发套件 (SDK) 和丰富的工具集。只需进行一次 SimpleLink 平台集成，便可将配置文件中的任意器件组合添加到设计中。SimpleLink 平台的最终目标是确保设计要求变更时，完全重复使用代码。更多详细信息，请访问 www.ti.com.cn/simplelink。

MSP432P411xT 和 MSP432P401xT MCU 具有配套的综合生态系统，其中包含工具、软件、文档、培训和支持，旨在帮助您迅速开始开发。MSP-EXP432P4111 有了 LaunchPad™开发套件或 MSP-TS432PZ100 目标插座板（附带额外的 MCU 样片）以及免费的 SimpleLink MSP432 SDK，即可开始开发。

器件信息(1)

器件型号	封装	封装尺寸(2)
MSP432P4111TPZ MSP432P411YTPZ MSP432P411VTPZ	LQFP (100)	14mm x 14mm
MSP432P4011TRGC MSP432P401YTRGC MSP432P401VTRGC	VQFN (64)	9mm x 9mm

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见*封装选项附录*（节 9）或浏览 TI 网站 www.ti.com.cn。
(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 9）。

1.4 功能方框图

图 1-1 和 图 1-2 分别显示了 MSP432P411xT 和 MSP432P401xT 器件的功能框图。

CPU 和器件中的所有外设通过共同的先进高性能总线 (AHB) 矩阵彼此交互。在某些情况下，AHB 端口和外设之间存在电桥。从存储器映射的角度来看，这些电桥对于应用而言是透明的，因此未显示在框图中。

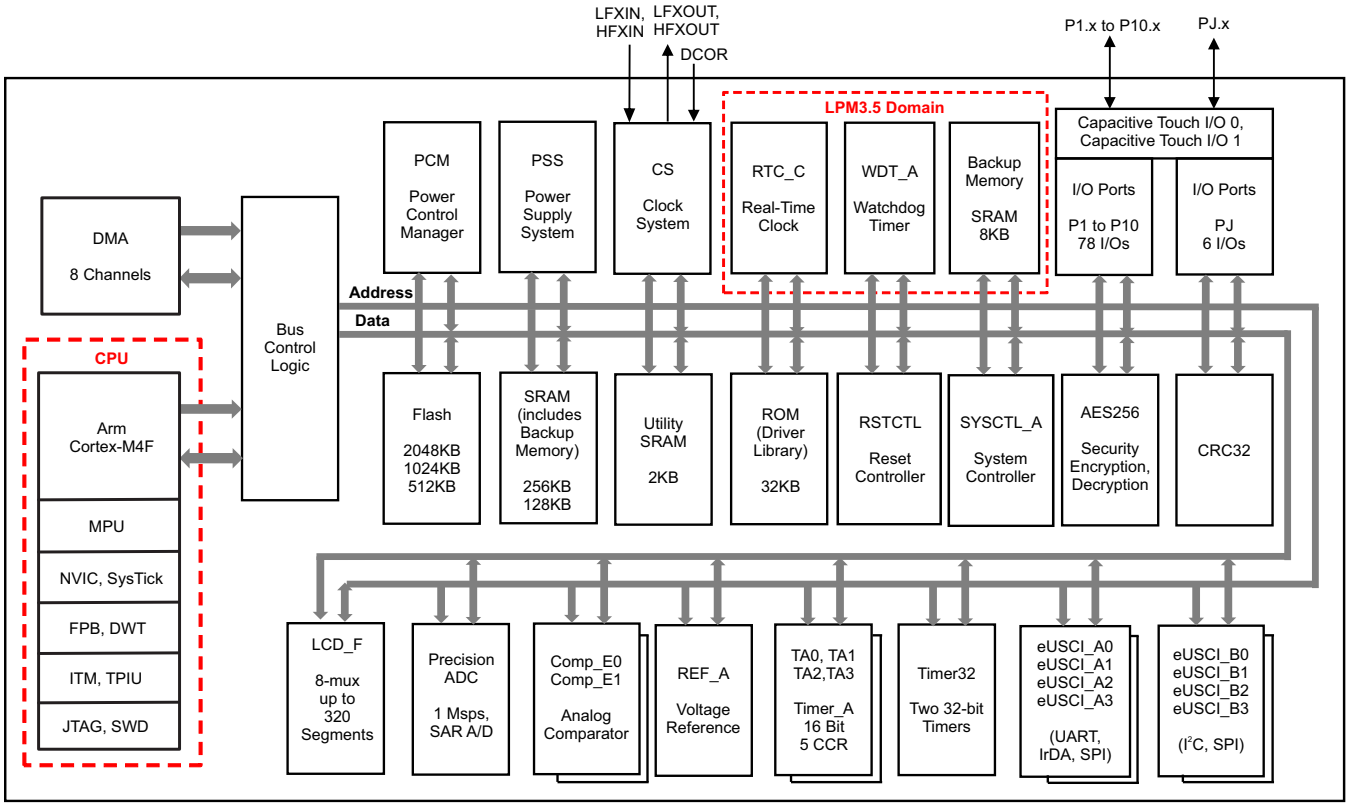


图 **1-1. MSP432P411xT** 功能框图

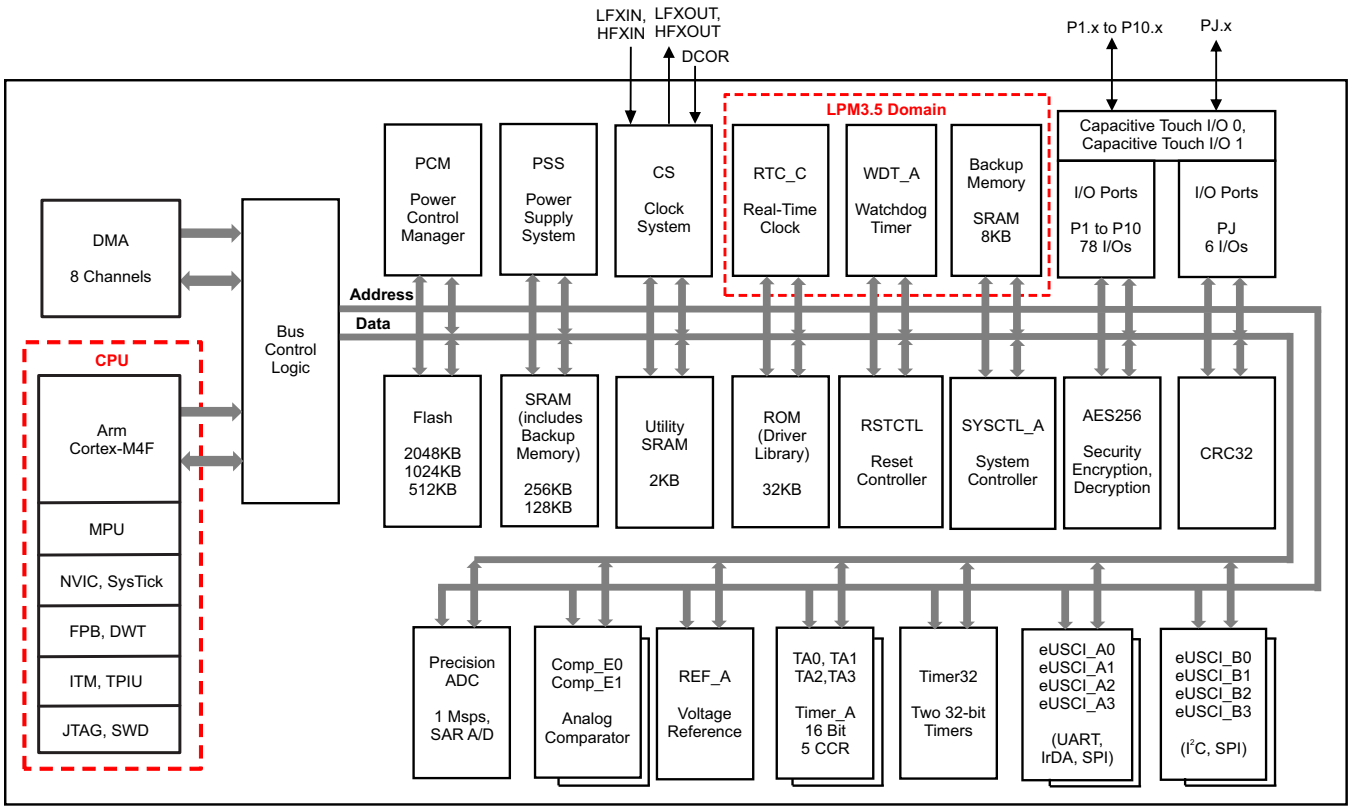


图 **1-2. MSP432P401xT** 功能框图

内容

2 修订历史记录

Changes from February 3, 2018 to June 17, 2019 **Page**

- Added that the I_{RESET} parameter applies to only the 100-pin LQFP package and not to the 64-pin VQFN package in Section 5.9, *Current Consumption During Device Reset of the 100-pin LQFP Package* 34
- Changed the MIN values for the $t_{HD,STA}$, $t_{SU,STA}$, $t_{HD,DAT}$, $t_{SU,DAT}$, and $t_{SU,STO}$ parameters in Table 5-45, *eUSCI Switching Characteristics (I^2C Mode)* 88
- 更新了 节 8.2，*器件命名规则* 中的文本 193

3 Device Comparison

Table 3-1 summarizes the features of MSP432P4x1xT devices.

Table 3-1. Device Comparison(1)

DEVICE	FLASH (KB)	SRAM (KB)	Precision ADC (Channels)	LCD (Segments)	COMP_E0 (Channels)	COMP_E1 (Channels)	Timer_A(2)	eUSCI_A: UART, IrDA, SPI	eUSCI_B: SPI, I²C	20-mA DRIVE I/Os	TOTAL I/Os	PACKAGE
MSP432P4111TPZ	2048	256	24 ext, 2 int	320	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P411YTPZ	1024	256	24 ext, 2 int	320	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P411VTPZ	512	128	24 ext, 2 int	320	8	8	5, 5, 5, 5	4	4	4	84	100 PZ
MSP432P4011TRGC	2048	256	12 ext, 2 int	N/A	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401YTRGC	1024	256	12 ext, 2 int	N/A	2	4	5, 5, 5	3	3	4	48	64 RGC
MSP432P401VTRGC	512	128	12 ext, 2 int	N/A	2	4	5, 5, 5	3	3	4	48	64 RGC

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in 节 9, or see the TI website at www.ti.com.
(2) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-Bit and 32-Bit Microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for SimpleLink Wired MCUs From precision sensors to intelligent gateway to cloud

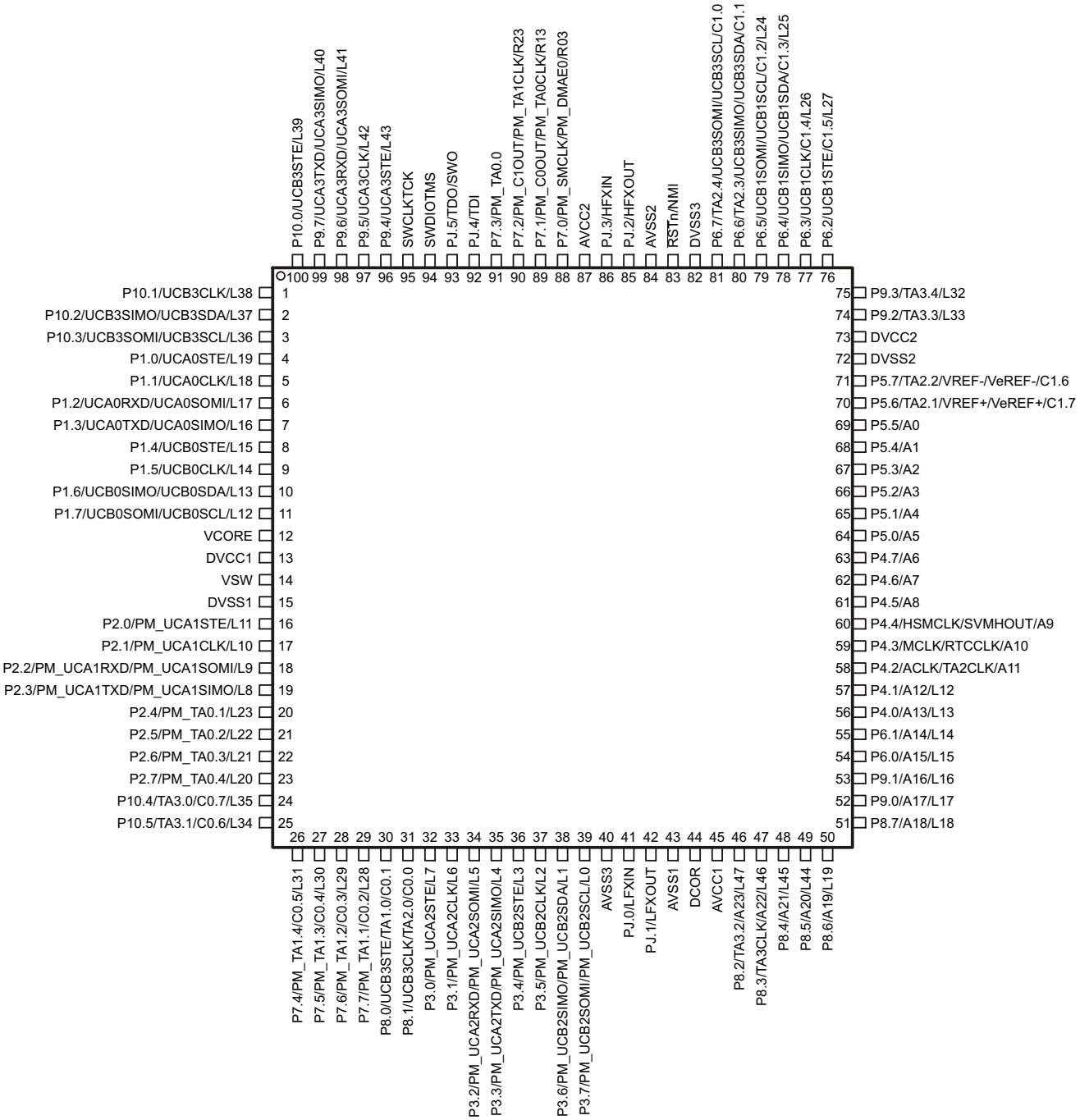
Companion Products for MSP432P4111T Review products that are frequently purchased or used with this product.

Reference Designs for MSP432P4111T Find reference designs that leverage the best in TI technology to solve your system-level challenges.

4 Terminal Configuration and Functions

4.1 Pin Diagram for MSP432P411xT Devices

Figure 4-1 shows the pinout of the 100-pin PZ package.



A. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. This pinout shows only the default mapping. See 节 6.9.2 for details.

B. A glitch filter is implemented on these digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.

C. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD

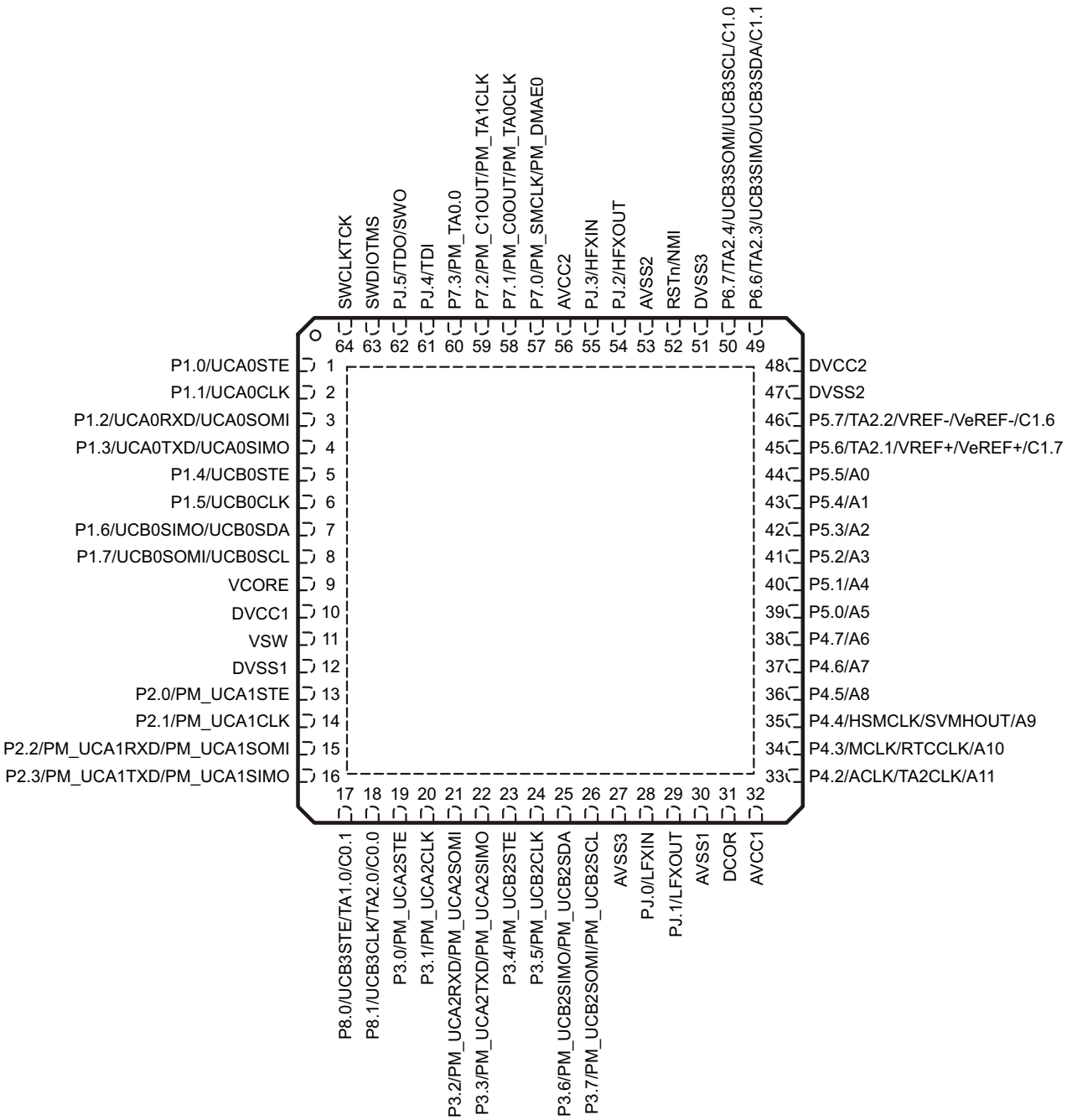
D. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI

E. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-1. 100-Pin PZ Package (Top View)

4.2 Pin Diagram for MSP432P401xT Devices

Figure 4-2 shows the pinout of the 64-pin RGC package.



A. The secondary digital functions on Ports P2, P3, and P7 are fully mappable. This pinout shows only the default mapping. See 节 6.9.2 for details.
B. A glitch filter is implemented on these digital I/Os: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, P6.7.
C. TI recommends connecting the thermal pad on the QFN package to DVSS.
D. UART BSL pins: P1.2 - BSLRXD, P1.3 - BSLTXD
E. SPI BSL pins: P1.4 - BSLSTE, P1.5 - BSLCLK, P1.6 - BSLSIMO, P1.7 - BSLSOMI
F. I^2C BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

Figure 4-2. 64-Pin RGC Package (Top View)

4.3 Pin Attributes

Table 4-1 describes the attributes of the pins for the MSP432P411xT devices.

Table 4-1. Pin Attributes for MSP432P411xT

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
1	P10.1 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3CLK	I/O	LVCMOS	DVCC	N/A
	L38	O	Analog	DVCC	N/A
2	P10.2 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3SIMO	I/O	LVCMOS	DVCC	N/A
	UCB3SDA	I/O	LVCMOS	DVCC	N/A
	L37	O	Analog	DVCC	N/A
3	P10.3 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3SOMI	I/O	LVCMOS	DVCC	N/A
	UCB3SCL	I/O	LVCMOS	DVCC	N/A
	L36	O	Analog	DVCC	N/A
4	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0STE	I/O	LVCMOS	DVCC	N/A
	L19(7)	O	Analog	DVCC	N/A
5	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0CLK	I/O	LVCMOS	DVCC	N/A
	L18(7)	O	Analog	DVCC	N/A
6	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0RXD	I	LVCMOS	DVCC	N/A
	UCA0SOMI	I/O	LVCMOS	DVCC	N/A
	L17(7)	O	Analog	DVCC	N/A
7	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0TXD	O	LVCMOS	DVCC	N/A
	UCA0SIMO	I/O	LVCMOS	DVCC	N/A
	L16(7)	O	Analog	DVCC	N/A
8	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0STE	I/O	LVCMOS	DVCC	N/A
	L15(7)	O	Analog	DVCC	N/A
9	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0CLK	I/O	LVCMOS	DVCC	N/A
	L14(7)	O	Analog	DVCC	N/A

(1) (RD) indicates the reset default signal name for that pin.
(2) To determine the pin mux encodings for each pin, see 节 6.12.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power
(4) Buffer Types: see Section 4.6 for details
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:
OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
N/A = Not applicable
(7) This LCD drive pin is also mirrored at a different location in the 100-pin PZ package. Assign the LCD drive output to only one pin at a time.

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
10	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0SIMO	I/O	LVCMOS	DVCC	N/A
	UCB0SDA	I/O	LVCMOS	DVCC	N/A
	L13(7)	O	Analog	DVCC	N/A
11	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0SOMI	I/O	LVCMOS	DVCC	N/A
	UCB0SCL	I/O	LVCMOS	DVCC	N/A
	L12(7)	O	Analog	DVCC	N/A
12	VCORE	–	Power	DVCC	N/A
13	DVCC1	–	Power	N/A	N/A
14	VSW	–	Power	N/A	N/A
15	DVSS1	–	Power	N/A	N/A
16	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1STE	I/O	LVCMOS	DVCC	N/A
	L11	O	Analog	DVCC	N/A
17	P2.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1CLK	I/O	LVCMOS	DVCC	N/A
	L10	O	Analog	DVCC	N/A
18	P2.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1RXD	I	LVCMOS	DVCC	N/A
	PM_UCA1SOMI	I/O	LVCMOS	DVCC	N/A
	L9	O	Analog	DVCC	N/A
19	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1TXD	O	LVCMOS	DVCC	N/A
	PM_UCA1SIMO	I/O	LVCMOS	DVCC	N/A
	L8	O	Analog	DVCC	N/A
20	P2.4 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.1	I/O	LVCMOS	DVCC	N/A
	L23	O	Analog	DVCC	N/A
21	P2.5 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.2	I/O	LVCMOS	DVCC	N/A
	L22	O	Analog	DVCC	N/A
22	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.3	I/O	LVCMOS	DVCC	N/A
	L21	O	Analog	DVCC	N/A
23	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.4	I/O	LVCMOS	DVCC	N/A
	L20	O	Analog	DVCC	N/A
24	P10.4 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3.0	I/O	LVCMOS	DVCC	N/A
	C0.7	I	Analog	DVCC	N/A
	L35	O	Analog	DVCC	N/A
25	P10.5 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3.1	I/O	LVCMOS	DVCC	N/A
	C0.6	I	Analog	DVCC	N/A
	L34	O	Analog	DVCC	N/A

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
26	P7.4 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA1.4	I/O	LVCMOS	DVCC	N/A
	C0.5	I	Analog	DVCC	N/A
	L31	O	Analog	DVCC	N/A
27	P7.5 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA1.3	I/O	LVCMOS	DVCC	N/A
	C0.4	I	Analog	DVCC	N/A
	L30	O	Analog	DVCC	N/A
28	P7.6 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA1.2	I/O	LVCMOS	DVCC	N/A
	C0.3	I	Analog	DVCC	N/A
	L29	O	Analog	DVCC	N/A
29	P7.7 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA1.1	I/O	LVCMOS	DVCC	N/A
	C0.2	I	Analog	DVCC	N/A
	L28	O	Analog	DVCC	N/A
30	P8.0 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3STE	I/O	LVCMOS	DVCC	N/A
	TA1.0	I/O	LVCMOS	DVCC	N/A
	C0.1	I	Analog	DVCC	N/A
31	P8.1 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3CLK	I/O	LVCMOS	DVCC	N/A
	TA2.0	I/O	LVCMOS	DVCC	N/A
	C0.0	I	Analog	DVCC	N/A
32	P3.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2STE	I/O	LVCMOS	DVCC	N/A
	L7	O	Analog	DVCC	N/A
33	P3.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2CLK	I/O	LVCMOS	DVCC	N/A
	L6	O	Analog	DVCC	N/A
34	P3.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2RXD	I	LVCMOS	DVCC	N/A
	PM_UCA2SOMI	I/O	LVCMOS	DVCC	N/A
	L5	O	Analog	DVCC	N/A
35	P3.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2TXD	O	LVCMOS	DVCC	N/A
	PM_UCA2SIMO	I/O	LVCMOS	DVCC	N/A
	L4	O	Analog	DVCC	N/A
36	P3.4 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2STE	I/O	LVCMOS	DVCC	N/A
	L3	O	Analog	DVCC	N/A
37	P3.5 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2CLK	I/O	LVCMOS	DVCC	N/A
	L2	O	Analog	DVCC	N/A

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
38	P3.6 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2SIMO	I/O	LVCMOS	DVCC	N/A
	PM_UCB2SDA	I/O	LVCMOS	DVCC	N/A
	L1	O	Analog	DVCC	N/A
39	P3.7 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2SOMI	I/O	LVCMOS	DVCC	N/A
	PM_UCB2SCL	I	LVCMOS	DVCC	N/A
	L0	O	Analog	DVCC	N/A
40	AVSS3	–	Power	N/A	N/A
41	PJ.0 (RD)	I/O	LVCMOS	DVCC	OFF
	LFXIN	I	Analog	DVCC	N/A
42	PJ.1 (RD)	I/O	LVCMOS	DVCC	OFF
	LFXOUT	O	Analog	DVCC	N/A
43	AVSS1	–	Power	N/A	N/A
44	DCOR	–	Analog	N/A	N/A
45	AVCC1	–	Power	N/A	N/A
46	P8.2 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3.2	I/O	LVCMOS	DVCC	N/A
	A23	I	Analog	DVCC	N/A
	L47	O	Analog	DVCC	N/A
47	P8.3 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3CLK	I	LVCMOS	DVCC	N/A
	A22	I	Analog	DVCC	N/A
	L46	O	Analog	DVCC	N/A
48	P8.4 (RD)	I/O	LVCMOS	DVCC	OFF
	A21	I	Analog	DVCC	N/A
	L45	O	Analog	DVCC	N/A
49	P8.5 (RD)	I/O	LVCMOS	DVCC	OFF
	A20	I	Analog	DVCC	N/A
	L44	O	Analog	DVCC	N/A
50	P8.6 (RD)	I/O	LVCMOS	DVCC	OFF
	A19	I	Analog	DVCC	N/A
	L19(7)	O	Analog	DVCC	N/A
51	P8.7 (RD)	I/O	LVCMOS	DVCC	OFF
	A18	I	Analog	DVCC	N/A
	L18(7)	O	Analog	DVCC	N/A
52	P9.0 (RD)	I/O	LVCMOS	DVCC	OFF
	A17	I	Analog	DVCC	N/A
	L17(7)	O	Analog	DVCC	N/A
53	P9.1 (RD)	I/O	LVCMOS	DVCC	OFF
	A16	I	Analog	DVCC	N/A
	L16(7)	O	Analog	DVCC	N/A
54	P6.0 (RD)	I/O	LVCMOS	DVCC	OFF
	A15	I	Analog	DVCC	N/A
	L15(7)	O	Analog	DVCC	N/A

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE[5]	RESET STATE AFTER POR[6]
55	P6.1 (RD)	I/O	LVCMOS	DVCC	OFF
	A14	I	Analog	DVCC	N/A
	L14[7]	O	Analog	DVCC	N/A
56	P4.0 (RD)	I/O	LVCMOS	DVCC	OFF
	A13	I	Analog	DVCC	N/A
	L13[7]	O	Analog	DVCC	N/A
57	P4.1 (RD)	I/O	LVCMOS	DVCC	OFF
	A12	I	Analog	DVCC	N/A
	L12[7]	O	Analog	DVCC	N/A
58	P4.2 (RD)	I/O	LVCMOS	DVCC	OFF
	ACLK	O	LVCMOS	DVCC	N/A
	TA2CLK	I	LVCMOS	DVCC	N/A
	A11	I	Analog	DVCC	N/A
59	P4.3 (RD)	I/O	LVCMOS	DVCC	OFF
	MCLK	O	LVCMOS	DVCC	N/A
	RTCCLK	O	LVCMOS	DVCC	N/A
	A10	I	Analog	DVCC	N/A
60	P4.4 (RD)	I/O	LVCMOS	DVCC	OFF
	HSMCLK	O	LVCMOS	DVCC	N/A
	SVMHOUT	O	LVCMOS	DVCC	N/A
	A9	I	Analog	DVCC	N/A
61	P4.5 (RD)	I/O	LVCMOS	DVCC	OFF
	A8	I	Analog	DVCC	N/A
62	P4.6 (RD)	I/O	LVCMOS	DVCC	OFF
	A7	I	Analog	DVCC	N/A
63	P4.7 (RD)	I/O	LVCMOS	DVCC	OFF
	A6	I	Analog	DVCC	N/A
64	P5.0 (RD)	I/O	LVCMOS	DVCC	OFF
	A5	I	Analog	DVCC	N/A
65	P5.1 (RD)	I/O	LVCMOS	DVCC	OFF
	A4	I	Analog	DVCC	N/A
66	P5.2 (RD)	I/O	LVCMOS	DVCC	OFF
	A3	I	Analog	DVCC	N/A
67	P5.3 (RD)	I/O	LVCMOS	DVCC	OFF
	A2	I	Analog	DVCC	N/A
68	P5.4 (RD)	I/O	LVCMOS	DVCC	OFF
	A1	I	Analog	DVCC	N/A
69	P5.5 (RD)	I/O	LVCMOS	DVCC	OFF
	A0	I	Analog	DVCC	N/A
70	P5.6 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.1	I/O	LVCMOS	DVCC	N/A
	VREF+	O	Analog	DVCC	N/A
	VeREF+	I	Analog	DVCC	N/A
	C1.7	I	Analog	DVCC	N/A

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
71	P5.7 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.2	I/O	LVCMOS	DVCC	N/A
	VREF-	O	Analog	DVCC	N/A
	VeREF-	I	Analog	DVCC	N/A
	C1.6	I	Analog	DVCC	N/A
72	DVSS2	–	Power	N/A	N/A
73	DVCC2	–	Power	N/A	N/A
74	P9.2 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3.3	I/O	LVCMOS	DVCC	N/A
	L33	O	Analog	DVCC	N/A
75	P9.3 (RD)	I/O	LVCMOS	DVCC	OFF
	TA3.4	I/O	LVCMOS	DVCC	N/A
	L32	O	Analog	DVCC	N/A
76	P6.2 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB1STE	I/O	LVCMOS	DVCC	N/A
	C1.5	I	Analog	DVCC	N/A
	L27	O	Analog	DVCC	N/A
77	P6.3 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB1CLK	I/O	LVCMOS	DVCC	N/A
	C1.4	I	Analog	DVCC	N/A
	L26	O	Analog	DVCC	N/A
78	P6.4 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB1SIMO	I/O	LVCMOS	DVCC	N/A
	UCB1SDA	I/O	LVCMOS	DVCC	N/A
	C1.3	I	Analog	DVCC	N/A
	L25	O	Analog	DVCC	N/A
79	P6.5 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB1SOMI	I/O	LVCMOS	DVCC	N/A
	UCB1SCL	I/O	LVCMOS	DVCC	N/A
	C1.2	I	Analog	DVCC	N/A
	L24	O	Analog	DVCC	N/A
80	P6.6 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.3	I/O	LVCMOS	DVCC	N/A
	UCB3SIMO	I/O	LVCMOS	DVCC	N/A
	UCB3SDA	I/O	LVCMOS	DVCC	N/A
	C1.1	I	Analog	DVCC	N/A
81	P6.7 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.4	I/O	LVCMOS	DVCC	N/A
	UCB3SOMI	I/O	LVCMOS	DVCC	N/A
	UCB3SCL	I/O	LVCMOS	DVCC	N/A
	C1.0	I	Analog	DVCC	N/A
82	DVSS3	–	Power	N/A	N/A
83	RSTn (RD)	I	LVCMOS	DVCC	PU
	NMI	I	LVCMOS	DVCC	N/A
84	AVSS2	–	Power	N/A	N/A

Table 4-1. Pin Attributes for MSP432P411xT (continued)

PIN NO. (PZ PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
85	PJ.2 (RD)	I/O	LVCMOS	DVCC	OFF
	HFXOUT	O	Analog	DVCC	N/A
86	PJ.3 (RD)	I/O	LVCMOS	DVCC	OFF
	HFXIN	I	Analog	DVCC	N/A
87	AVCC2	–	Power	N/A	N/A
88	P7.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_SMCLK	O	LVCMOS	DVCC	N/A
	PM_DMAE0	I	LVCMOS	DVCC	N/A
	R03	I	Analog	DVCC	N/A
89	P7.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_C0OUT	O	LVCMOS	DVCC	N/A
	PM_TA0CLK	I	LVCMOS	DVCC	N/A
	R13	I	Analog	DVCC	N/A
90	P7.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_C1OUT	O	LVCMOS	DVCC	N/A
	PM_TA1CLK	I	LVCMOS	DVCC	N/A
	R23	I	Analog	DVCC	N/A
91	P7.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.0	I/O	LVCMOS	DVCC	N/A
92	PJ.4	I/O	LVCMOS	DVCC	N/A
	TDI (RD)	I	LVCMOS	DVCC	PU
93	PJ.5	I/O	LVCMOS	DVCC	N/A
	TDO (RD)	O	LVCMOS	DVCC	N/A
	SWO	O	LVCMOS	DVCC	N/A
94	SWDIOTMS	I/O	LVCMOS	DVCC	PU
95	SWCLKTCK	I	LVCMOS	DVCC	PD
96	P9.4 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA3STE	I/O	LVCMOS	DVCC	N/A
	L43	O	Analog	DVCC	N/A
97	P9.5 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA3CLK	I/O	LVCMOS	DVCC	N/A
	L42	O	Analog	DVCC	N/A
98	P9.6 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA3RXD	I	LVCMOS	DVCC	N/A
	UCA3SOMI	I/O	LVCMOS	DVCC	N/A
	L41	O	Analog	DVCC	N/A
99	P9.7 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA3TXD	O	LVCMOS	DVCC	N/A
	UCA3SIMO	I/O	LVCMOS	DVCC	N/A
	L40	O	Analog	DVCC	N/A
100	P10.0 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3STE	I/O	LVCMOS	DVCC	N/A
	L39	O	Analog	DVCC	N/A

Table 4-2 describes the attributes of the pins for the MSP432P401xT devices.

Table 4-2. Pin Attributes for MSP432P401xT

PIN NO. (RGC PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
1	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0STE	I/O	LVCMOS	DVCC	N/A
2	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0CLK	I/O	LVCMOS	DVCC	N/A
3	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0RXD	I	LVCMOS	DVCC	N/A
	UCA0SOMI	I/O	LVCMOS	DVCC	N/A
4	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
	UCA0TXD	O	LVCMOS	DVCC	N/A
	UCA0SIMO	I/O	LVCMOS	DVCC	N/A
5	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0STE	I/O	LVCMOS	DVCC	N/A
6	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0CLK	I/O	LVCMOS	DVCC	N/A
7	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0SIMO	I/O	LVCMOS	DVCC	N/A
	UCB0SDA	I/O	LVCMOS	DVCC	N/A
8	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB0SOMI	I/O	LVCMOS	DVCC	N/A
	UCB0SCL	I/O	LVCMOS	DVCC	N/A
9	VCORE	–	Power	DVCC	N/A
10	DVCC1	–	Power	N/A	N/A
11	VSW	–	Power	N/A	N/A
12	DVSS1	–	Power	N/A	N/A
13	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1STE	I/O	LVCMOS	DVCC	N/A
14	P2.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1CLK	I/O	LVCMOS	DVCC	N/A
15	P2.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1RXD	I	LVCMOS	DVCC	N/A
	PM_UCA1SOMI	I/O	LVCMOS	DVCC	N/A
16	P2.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA1TXD	O	LVCMOS	DVCC	N/A
	PM_UCA1SIMO	I/O	LVCMOS	DVCC	N/A

(1) (RD) indicates the reset default signal name for that pin.
(2) To determine the pin mux encodings for each pin, see 节 6.12.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power
(4) Buffer Types: see Section 4.6 for details
(5) The power source shown in this table is the I/O power source, which may differ from the module power source.
(6) Reset States:
OFF = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled
PD = High-impedance input with pulldown enabled
PU = High-impedance input with pullup enabled
N/A = Not applicable

Table 4-2. Pin Attributes for MSP432P401xT (continued)

PIN NO. (RGC PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
17	P8.0 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3STE	I/O	LVCMOS	DVCC	N/A
	TA1.0	I/O	LVCMOS	DVCC	N/A
	C0.1	I	Analog	DVCC	N/A
18	P8.1 (RD)	I/O	LVCMOS	DVCC	OFF
	UCB3CLK	I/O	LVCMOS	DVCC	N/A
	TA2.0	I/O	LVCMOS	DVCC	N/A
	C0.0	I	Analog	DVCC	N/A
19	P3.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2STE	I/O	LVCMOS	DVCC	N/A
20	P3.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2CLK	I/O	LVCMOS	DVCC	N/A
21	P3.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2RXD	I	LVCMOS	DVCC	N/A
	PM_UCA2SOMI	I/O	LVCMOS	DVCC	N/A
22	P3.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCA2TXD	O	LVCMOS	DVCC	N/A
	PM_UCA2SIMO	I/O	LVCMOS	DVCC	N/A
23	P3.4 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2STE	I/O	LVCMOS	DVCC	N/A
24	P3.5 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2CLK	I/O	LVCMOS	DVCC	N/A
25	P3.6 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2SIMO	I/O	LVCMOS	DVCC	N/A
	PM_UCB2SDA	I/O	LVCMOS	DVCC	N/A
26	P3.7 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_UCB2SOMI	I/O	LVCMOS	DVCC	N/A
	PM_UCB2SCL	I	LVCMOS	DVCC	N/A
27	AVSS3	–	Power	N/A	N/A
28	PJ.0 (RD)	I/O	LVCMOS	DVCC	OFF
	LFXIN	I	Analog	DVCC	N/A
29	PJ.1 (RD)	I/O	LVCMOS	DVCC	OFF
	LFXOUT	O	Analog	DVCC	N/A
30	AVSS1	–	Power	N/A	N/A
31	DCOR	–	Analog	N/A	N/A
32	AVCC1	–	Power	N/A	N/A
33	P4.2 (RD)	I/O	LVCMOS	DVCC	OFF
	ACLK	O	LVCMOS	DVCC	N/A
	TA2CLK	I	LVCMOS	DVCC	N/A
	A11	I	Analog	DVCC	N/A
34	P4.3 (RD)	I/O	LVCMOS	DVCC	OFF
	MCLK	O	LVCMOS	DVCC	N/A
	RTCCLK	O	LVCMOS	DVCC	N/A
	A10	I	Analog	DVCC	N/A

Table 4-2. Pin Attributes for MSP432P401xT (continued)

PIN NO. (RGC PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
35	P4.4 (RD)	I/O	LVCMOS	DVCC	OFF
	HSMCLK	O	LVCMOS	DVCC	N/A
	SVMHOUT	O	LVCMOS	DVCC	N/A
	A9	I	Analog	DVCC	N/A
36	P4.5 (RD)	I/O	LVCMOS	DVCC	OFF
	A8	I	Analog	DVCC	N/A
37	P4.6 (RD)	I/O	LVCMOS	DVCC	OFF
	A7	I	Analog	DVCC	N/A
38	P4.7 (RD)	I/O	LVCMOS	DVCC	OFF
	A6	I	Analog	DVCC	N/A
39	P5.0 (RD)	I/O	LVCMOS	DVCC	OFF
	A5	I	Analog	DVCC	N/A
40	P5.1 (RD)	I/O	LVCMOS	DVCC	OFF
	A4	I	Analog	DVCC	N/A
41	P5.2 (RD)	I/O	LVCMOS	DVCC	OFF
	A3	I	Analog	DVCC	N/A
42	P5.3 (RD)	I/O	LVCMOS	DVCC	OFF
	A2	I	Analog	DVCC	N/A
43	P5.4 (RD)	I/O	LVCMOS	DVCC	OFF
	A1	I	Analog	DVCC	N/A
44	P5.5 (RD)	I/O	LVCMOS	DVCC	OFF
	A0	I	Analog	DVCC	N/A
45	P5.6 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.1	I/O	LVCMOS	DVCC	N/A
	VREF+	O	Analog	DVCC	N/A
	VeREF+	I	Analog	DVCC	N/A
	C1.7	I	Analog	DVCC	N/A
46	P5.7 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.2	I/O	LVCMOS	DVCC	N/A
	VREF-	O	Analog	DVCC	N/A
	VeREF-	I	Analog	DVCC	N/A
	C1.6	I	Analog	DVCC	N/A
47	DVSS2	–	Power	N/A	N/A
48	DVCC2	–	Power	N/A	N/A
49	P6.6 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.3	I/O	LVCMOS	DVCC	N/A
	UCB3SIMO	I/O	LVCMOS	DVCC	N/A
	UCB3SDA	I/O	LVCMOS	DVCC	N/A
	C1.1	I	Analog	DVCC	N/A
50	P6.7 (RD)	I/O	LVCMOS	DVCC	OFF
	TA2.4	I/O	LVCMOS	DVCC	N/A
	UCB3SOMI	I/O	LVCMOS	DVCC	N/A
	UCB3SCL	I/O	LVCMOS	DVCC	N/A
	C1.0	I	Analog	DVCC	N/A
51	DVSS3	–	Power	N/A	N/A

Table 4-2. Pin Attributes for MSP432P401xT (continued)

PIN NO. (RGC PACKAGE)	SIGNAL NAME(1) (2)	SIGNAL TYPE(3)	BUFFER TYPE(4)	POWER SOURCE(5)	RESET STATE AFTER POR(6)
52	RSTn (RD)	I	LVCMOS	DVCC	PU
	NMI	I	LVCMOS	DVCC	N/A
53	AVSS2	–	Power	N/A	N/A
54	PJ.2 (RD)	I/O	LVCMOS	DVCC	OFF
	HFXOUT	O	Analog	DVCC	N/A
55	PJ.3 (RD)	I/O	LVCMOS	DVCC	OFF
	HFXIN	I	Analog	DVCC	N/A
56	AVCC2	–	Power	N/A	N/A
57	P7.0 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_SMCLK	O	LVCMOS	DVCC	N/A
	PM_DMAE0	I	LVCMOS	DVCC	N/A
58	P7.1 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_C0OUT	O	LVCMOS	DVCC	N/A
	PM_TA0CLK	I	LVCMOS	DVCC	N/A
59	P7.2 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_C1OUT	O	LVCMOS	DVCC	N/A
	PM_TA1CLK	I	LVCMOS	DVCC	N/A
60	P7.3 (RD)	I/O	LVCMOS	DVCC	OFF
	PM_TA0.0	I/O	LVCMOS	DVCC	N/A
61	PJ.4	I/O	LVCMOS	DVCC	N/A
	TDI (RD)	I	LVCMOS	DVCC	PU
62	PJ.5	I/O	LVCMOS	DVCC	N/A
	TDO (RD)	O	LVCMOS	DVCC	N/A
	SWO	O	LVCMOS	DVCC	N/A
63	SWDIOTMS	I/O	LVCMOS	DVCC	PU
64	SWCLKTCK	I	LVCMOS	DVCC	PD
Pad	QFN Pad	–	–	N/A	–

4.4 Signal Descriptions

Table 4-3 describes the signals for all device variants and package options.

Table 4-3. Signal Descriptions

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
ADC	A0	69	44	I	ADC analog input A0
	A1	68	43	I	ADC analog input A1
	A2	67	42	I	ADC analog input A2
	A3	66	41	I	ADC analog input A3
	A4	65	40	I	ADC analog input A4
	A5	64	39	I	ADC analog input A5
	A6	63	38	I	ADC analog input A6
	A7	62	37	I	ADC analog input A7
	A8	61	36	I	ADC analog input A8
	A9	60	35	I	ADC analog input A9
	A10	59	34	I	ADC analog input A10
	A11	58	33	I	ADC analog input A11
	A12	57	N/A	I	ADC analog input A12
	A13	56	N/A	I	ADC analog input A13
	A14	55	N/A	I	ADC analog input A14
	A15	54	N/A	I	ADC analog input A15
	A16	53	N/A	I	ADC analog input A16
	A17	52	N/A	I	ADC analog input A17
	A18	51	N/A	I	ADC analog input A18
	A19	50	N/A	I	ADC analog input A19
	A20	49	N/A	I	ADC analog input A20
	A21	48	N/A	I	ADC analog input A21
	A22	47	N/A	I	ADC analog input A22
	A23	46	N/A	I	ADC analog input A23
Clock	ACLK	58	33	O	ACLK clock output
	DCOR	44	31	–	DCO external resistor pin
	HFXIN	86	55	I	Input for high-frequency crystal oscillator HFXT
	HFXOUT	85	54	O	Output for high-frequency crystal oscillator HFXT
	HSMCLK	60	35	O	HSMCLK clock output
	LFXIN	41	28	I	Input for low-frequency crystal oscillator LFXT
	LFXOUT	42	29	O	Output of low-frequency crystal oscillator LFXT
	MCLK	59	34	O	MCLK clock output

(1) N/A = not available
(2) I = input, O = output

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
Comparator	C0.0	31	18	I	Comparator_E0 input 0
	C0.1	30	17	I	Comparator_E0 input 1
	C0.2	29	N/A	I	Comparator_E0 input 2
	C0.3	28	N/A	I	Comparator_E0 input 3
	C0.4	27	N/A	I	Comparator_E0 input 4
	C0.5	26	N/A	I	Comparator_E0 input 5
	C0.6	25	N/A	I	Comparator_E0 input 6
	C0.7	24	N/A	I	Comparator_E0 input 7
	C1.0	81	50	I	Comparator_E1 input 0
	C1.1	80	49	I	Comparator_E1 input 1
	C1.2	79	N/A	I	Comparator_E1 input 2
	C1.3	78	N/A	I	Comparator_E1 input 3
	C1.4	77	N/A	I	Comparator_E1 input 4
	C1.5	76	N/A	I	Comparator_E1 input 5
	C1.6	71	46	I	Comparator_E1 input 6
	C1.7	70	45	I	Comparator_E1 input 7
LCD(3)	L0	39	N/A	O	LCD drive pin 0; either segment or common output
	L1	38	N/A	O	LCD drive pin 1; either segment or common output
	L2	37	N/A	O	LCD drive pin 2; either segment or common output
	L3	36	N/A	O	LCD drive pin 3; either segment or common output
	L4	35	N/A	O	LCD drive pin 4; either segment or common output
	L5	34	N/A	O	LCD drive pin 5; either segment or common output
	L6	33	N/A	O	LCD drive pin 6; either segment or common output
	L7	32	N/A	O	LCD drive pin 7; either segment or common output
	L8	19	N/A	O	LCD drive pin 8; either segment or common output
	L9	18	N/A	O	LCD drive pin 9; either segment or common output
	L10	17	N/A	O	LCD drive pin 10; either segment or common output
	L11	16	N/A	O	LCD drive pin 11; either segment or common output
	L12(4)	11, 57	N/A	O	LCD drive pin 12; either segment or common output
	L13(4)	10, 56	N/A	O	LCD drive pin 13; either segment or common output
	L14(4)	9, 55	N/A	O	LCD drive pin 14; either segment or common output
	L15(4)	8, 54	N/A	O	LCD drive pin 15; either segment or common output
	L16(4)	7, 53	N/A	O	LCD drive pin 16; either segment or common output
	L17(4)	6, 52	N/A	O	LCD drive pin 17; either segment or common output
	L18(4)	5, 51	N/A	O	LCD drive pin 18; either segment or common output
	L19(4)	4, 50	N/A	O	LCD drive pin 19; either segment or common output
	L20	23	N/A	O	LCD drive pin 20; either segment or common output
	L21	22	N/A	O	LCD drive pin 21; either segment or common output
	L22	21	N/A	O	LCD drive pin 22; either segment or common output
	L23	20	N/A	O	LCD drive pin 23; either segment or common output
	L24	79	N/A	O	LCD drive pin 24; either segment or common output

(3) Available on MSP432P411xT devices only.
(4) This LCD drive pin is also mirrored at a different location in the 100-pin PZ package. Assign the LCD drive output to only one pin at a time.

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
LCD(3) (continued)	L25	78	N/A	O	LCD drive pin 25; either segment or common output
	L26	77	N/A	O	LCD drive pin 26; either segment or common output
	L27	76	N/A	O	LCD drive pin 27; either segment or common output
	L28	29	N/A	O	LCD drive pin 28; either segment or common output
	L29	28	N/A	O	LCD drive pin 29; either segment or common output
	L30	27	N/A	O	LCD drive pin 30; either segment or common output
	L31	26	N/A	O	LCD drive pin 31; either segment or common output
	L32	75	N/A	O	LCD drive pin 32; either segment or common output
	L33	74	N/A	O	LCD drive pin 33; either segment or common output
	L34	25	N/A	O	LCD drive pin 34; either segment or common output
	L35	24	N/A	O	LCD drive pin 35; either segment or common output
	L36	3	N/A	O	LCD drive pin 36; either segment or common output
	L37	2	N/A	O	LCD drive pin 37; either segment or common output
	L38	1	N/A	O	LCD drive pin 38; either segment or common output
	L39	100	N/A	O	LCD drive pin 39; either segment or common output
	L40	99	N/A	O	LCD drive pin 40; either segment or common output
	L41	98	N/A	O	LCD drive pin 41; either segment or common output
	L42	97	N/A	O	LCD drive pin 42; either segment or common output
	L43	96	N/A	O	LCD drive pin 43; either segment or common output
	L44	49	N/A	O	LCD drive pin 44; either segment or common output
	L45	48	N/A	O	LCD drive pin 45; either segment or common output
	L46	47	N/A	O	LCD drive pin 46; either segment or common output
	L47	46	N/A	O	LCD drive pin 47; either segment or common output
	R03	88	N/A	I	Input port of fourth most positive analog LCD voltage V4 in External Bias Mode.
	R13	89	N/A	I	Input port of fourth most positive analog LCD voltage V3 in External Bias Mode.
	R23	90	N/A	I	Input port of fourth most positive analog LCD voltage V2 in External Bias Mode.
Debug	SWCLKTCK	95	64	I	Serial wire clock input (SWCLK)/JTAG clock input (TCK)
	SWDIOTMS	94	63	I/O	Serial wire data input/output (SWDIO)/JTAG test mode select (TMS)
	SWO	93	62	O	Serial wire trace output
	TDI	92	61	I	JTAG test data input
	TDO	93	62	O	JTAG test data output

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
GPIO (P1)	P1.0	4	1	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.1	5	2	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.2	6	3	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.3	7	4	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.4	8	5	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.5	9	6	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P1.6	10	7	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P1.7	11	8	I/O	General-purpose digital I/O with port interrupt and wake-up capability
GPIO (P2)	P2.0	16	13	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with a drive capability of up to 20 mA.
	P2.1	17	14	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with a drive capability of up to 20 mA.
	P2.2	18	15	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with a drive capability of up to 20 mA.
	P2.3	19	16	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function. This I/O can be configured for high-drive operation with a drive capability of up to 20 mA.
	P2.4	20	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.5	21	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.6	22	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P2.7	23	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
GPIO (P3)	P3.0	32	19	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.1	33	20	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.2	34	21	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.3	35	22	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.4	36	23	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.5	37	24	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability, and with reconfigurable port mapping secondary function
	P3.6	38	25	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
	P3.7	39	26	I/O	General-purpose digital I/O with port interrupt and wake-up capability and with reconfigurable port mapping secondary function
GPIO (P4)	P4.0	56	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.1	57	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.2	58	33	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.3	59	34	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.4	60	35	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.5	61	36	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.6	62	37	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P4.7	63	38	I/O	General-purpose digital I/O with port interrupt and wake-up capability
GPIO (P5)	P5.0	64	39	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.1	65	40	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.2	66	41	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.3	67	42	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.4	68	43	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.5	69	44	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.6	70	45	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P5.7	71	46	I/O	General-purpose digital I/O with port interrupt and wake-up capability

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
GPIO (P6)	P6.0	54	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.1	55	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.2	76	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.3	77	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.4	78	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.5	79	N/A	I/O	General-purpose digital I/O with port interrupt and wake-up capability
	P6.6	80	49	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
	P6.7	81	50	I/O	General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability
GPIO (P7)	P7.0	88	57	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.1	89	58	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.2	90	59	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.3	91	60	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.4	26	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.5	27	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.6	28	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
	P7.7	29	N/A	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function (RD)
GPIO (P8)	P8.0	30	17	I/O	General-purpose digital I/O
	P8.1	31	18	I/O	General-purpose digital I/O
	P8.2	46	N/A	I/O	General-purpose digital I/O
	P8.3	47	N/A	I/O	General-purpose digital I/O
	P8.4	48	N/A	I/O	General-purpose digital I/O
	P8.5	49	N/A	I/O	General-purpose digital I/O
	P8.6	50	N/A	I/O	General-purpose digital I/O
	P8.7	51	N/A	I/O	General-purpose digital I/O
GPIO (P9)	P9.0	52	N/A	I/O	General-purpose digital I/O
	P9.1	53	N/A	I/O	General-purpose digital I/O
	P9.2	74	N/A	I/O	General-purpose digital I/O
	P9.3	75	N/A	I/O	General-purpose digital I/O
	P9.4	96	N/A	I/O	General-purpose digital I/O
	P9.5	97	N/A	I/O	General-purpose digital I/O
	P9.6	98	N/A	I/O	General-purpose digital I/O
	P9.7	99	N/A	I/O	General-purpose digital I/O

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
GPIO (P10)	P10.0	100	N/A	I/O	General-purpose digital I/O
	P10.1	1	N/A	I/O	General-purpose digital I/O
	P10.2	2	N/A	I/O	General-purpose digital I/O
	P10.3	3	N/A	I/O	General-purpose digital I/O
	P10.4	24	N/A	I/O	General-purpose digital I/O
	P10.5	25	N/A	I/O	General-purpose digital I/O
GPIO (PJ)	PJ.0	41	28	I/O	General-purpose digital I/O
	PJ.1	42	29	I/O	General-purpose digital I/O
	PJ.2	85	54	I/O	General-purpose digital I/O
	PJ.3	86	55	I/O	General-purpose digital I/O
	PJ.4	92	61	I/O	General-purpose digital I/O
	PJ.5	93	62	I/O	General-purpose digital I/O
I^2C	UCB0SCL	11	8	I/O	I^2C clock – eUSCI_B0 I^2C mode
	UCB0SDA	10	7	I/O	I^2C data – eUSCI_B0 I^2C mode
	UCB1SCL	79	N/A	I/O	I^2C clock – eUSCI_B1 I^2C mode
	UCB1SDA	78	N/A	I/O	I^2C data – eUSCI_B1 I^2C mode
	UCB3SCL	3	N/A	I/O	I^2C clock – eUSCI_B3 I^2C mode
	UCB3SCL	81	50	I/O	I^2C clock – eUSCI_B3 I^2C mode
	UCB3SDA	2	N/A	I/O	I^2C data – eUSCI_B3 I^2C mode
	UCB3SDA	80	49	I/O	I^2C data – eUSCI_B3 I^2C mode

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
Port Mapper	PM_C0OUT	89	58	O	Default mapping: Comparator_E0 output
	PM_C1OUT	90	59	O	Default mapping: Comparator_E1 output
	PM_DMAE0	88	57	I	Default mapping: DMA external trigger input
	PM_SMCLK	88	57	O	Default mapping: SMCLK clock output
	PM_TA0.0	91	60	I/O	Default mapping: TA0 CCR0 capture: CCI0A input, compare: Out0
	PM_TA0.1	20	N/A	I/O	Default mapping: TA0 CCR1 capture: CCI1A input, compare: Out1
	PM_TA0.2	21	N/A	I/O	Default mapping: TA0 CCR2 capture: CCI2A input, compare: Out2
	PM_TA0.3	22	N/A	I/O	Default mapping: TA0 CCR3 capture: CCI3A input, compare: Out3
	PM_TA0.4	23	N/A	I/O	Default mapping: TA0 CCR4 capture: CCI4A input, compare: Out4
	PM_TA0CLK	89	58	I	Default mapping: TA0 input clock
	PM_TA1.2	28	N/A	I/O	Default mapping: TA1 CCR2 capture: CCI2A input, compare: Out2
	PM_TA1.3	27	N/A	I/O	Default mapping: TA1 CCR3 capture: CCI3A input, compare: Out3
	PM_TA1.4	26	N/A	I/O	Default mapping: TA1 CCR4 capture: CCI4A input, compare: Out4
	PM_TA1CLK	90	59	I	Default mapping: TA1 input clock
	PM_UCA1CLK	17	14	I/O	Default mapping: Clock signal input for eUSCI_A1 SPI slave mode Clock signal output for eUSCI_A1 SPI master mode
	PM_UCA1RXD	18	15	I	Default mapping: Receive data for eUSCI_A1 UART mode
	PM_UCA1SIMO	19	16	I/O	Default mapping: Slave in, master out for eUSCI_A1 SPI mode
	PM_UCA1SOMI	18	15	I/O	Default mapping: Slave out, master in for eUSCI_A1 SPI mode
	PM_UCA1STE	16	13	I/O	Default mapping: Slave transmit enable for eUSCI_A1 SPI mode
	PM_UCA1TXD	19	16	O	Default mapping: Transmit data for eUSCI_A1 UART mode
	PM_UCA2CLK	33	20	I/O	Default mapping: Clock signal input for eUSCI_A2 SPI slave mode Clock signal output for eUSCI_A2 SPI master mode
	PM_UCA2RXD	34	21	I	Default mapping: Receive data for eUSCI_A2 UART mode
	PM_UCA2SIMO	35	22	I/O	Default mapping: Slave in, master out for eUSCI_A2 SPI mode
	PM_UCA2SOMI	34	21	I/O	Default mapping: Slave out, master in for eUSCI_A2 SPI mode
	PM_UCA2STE	32	19	I/O	Default mapping: Slave transmit enable for eUSCI_A2 SPI mode
	PM_UCA2TXD	35	22	O	Default mapping: Transmit data for eUSCI_A2 UART mode

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
Port Mapper (continued)	PM_UCB2CLK	37	24	I/O	Default mapping: Clock signal input for eUSCI_B2 SPI slave mode Clock signal output for eUSCI_B2 SPI master mode
	PM_UCB2SCL	39	26	I	Default mapping: I^2C clock for eUSCI_B2 I^2C mode
	PM_UCB2SDA	38	25	I/O	Default mapping: I^2C data for eUSCI_B2 I^2C mode
	PM_UCB2SIMO	38	25	I/O	Default mapping: Slave in, master out for eUSCI_B2 SPI mode
	PM_UCB2SOMI	39	26	I/O	Default mapping: Slave out, master in for eUSCI_B2 SPI mode
	PM_UCB2STE	36	23	I/O	Default mapping: Slave transmit enable for eUSCI_B2 SPI mode
Power	AVCC1	45	32	–	Analog power supply
	AVCC2	87	56	–	Analog power supply
	AVSS1	43	30	–	Analog ground supply
	AVSS2	84	53	–	Analog ground supply
	AVSS3	40	27	–	Analog ground supply
	DVCC1	13	10	–	Digital power supply
	DVCC2	73	48	–	Digital power supply
	DVSS1	15	12	–	Digital ground supply
	DVSS2	72	47	–	Digital ground supply
	DVSS3	82	51	–	Must be connected to ground
	VCORE(5)	12	9	–	Regulated core power supply (internal use only, no external current loading)
	VSW	14	11	–	DC/DC converter switching output
RTC	RTCCLK	59	34	O	RTC_C clock calibration output
Reference	VREF+	70	45	O	Internal shared reference voltage positive terminal
	VREF-	71	46	O	Internal shared reference voltage negative terminal
	VeREF+	70	45	I	Positive terminal of external reference voltage to ADC
	VeREF-	71	46	I	Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground)

(5) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
SPI	UCA0CLK	5	2	I/O	Clock signal input for eUSCI_A0 SPI slave mode Clock signal output for eUSCI_A0 SPI master mode
	UCA0SIMO	7	4	I/O	Slave in, master out for eUSCI_A0 SPI mode
	UCA0SOMI	6	3	I/O	Slave out, master in for eUSCI_A0 SPI mode
	UCA0STE	4	1	I/O	Slave transmit enable for eUSCI_A0 SPI mode
	UCA3CLK	97	N/A	I/O	Clock signal input for eUSCI_A3 SPI slave mode Clock signal output for eUSCI_A3 SPI master mode
	UCA3SIMO	99	N/A	I/O	Slave in, master out for eUSCI_A3 SPI mode
	UCA3SOMI	98	N/A	I/O	Slave out, master in for eUSCI_A3 SPI mode
	UCA3STE	96	N/A	I/O	Slave transmit enable for eUSCI_A3 SPI mode
	UCB0CLK	9	6	I/O	Clock signal input for eUSCI_B0 SPI slave mode Clock signal output for eUSCI_B0 SPI master mode
	UCB0SIMO	10	7	I/O	Slave in, master out for eUSCI_B0 SPI mode
	UCB0SOMI	11	8	I/O	Slave out, master in for eUSCI_B0 SPI mode
	UCB0STE	8	5	I/O	Slave transmit enable for eUSCI_B0 SPI mode
	UCB1CLK	77	N/A	I/O	Clock signal input for eUSCI_B1 SPI slave mode Clock signal output for eUSCI_B1 SPI master mode
	UCB1SIMO	78	N/A	I/O	Slave in, master out for eUSCI_B1 SPI mode
	UCB1SOMI	79	N/A	I/O	Slave out, master in for eUSCI_B1 SPI mode
	UCB1STE	76	N/A	I/O	Slave transmit enable for eUSCI_B1 SPI mode
	UCB3CLK	1 31	18	I/O	Clock signal input for eUSCI_B3 SPI slave mode Clock signal output for eUSCI_B3 SPI master mode
	UCB3SIMO	2 80	49	I/O	Slave in, master out for eUSCI_B3 SPI mode
	UCB3SOMI	3 81	50	I/O	Slave out, master in for eUSCI_B3 SPI mode
	UCB3STE	30 100	17	I/O	Slave transmit enable for eUSCI_B3 SPI mode
System	NMI	83	52	I	External nonmaskable interrupt
	RSTn	83	52	I	External reset (active low)
	SVMHOUT	60	35	O	SVMH output
Thermal	QFN Pad	N/A	Pad	–	QFN package exposed thermal pad. TI recommends connection to VSS.
Timer	PM_TA1.1	29	N/A	I/O	Default mapping: TA1 CCR1 capture: CCI1A input, compare: Out1
	TA1.0	30	17	I/O	TA1 CCR0 capture: CCI0A input, compare: Out0
	TA2.0	31	18	I/O	TA2 CCR0 capture: CCI0A input, compare: Out0
	TA2.1	70	45	I/O	TA2 CCR1 capture: CCI1A input, compare: Out1
	TA2.2	71	46	I/O	TA2 CCR2 capture: CCI2A input, compare: Out2
	TA2.3	80	49	I/O	TA2 CCR3 capture: CCI3A input, compare: Out3
	TA2.4	81	50	I/O	TA2 CCR4 capture: CCI4A input, compare: Out4
	TA2CLK	58	33	I	TA2 input clock
	TA3.0	24	N/A	I/O	TA3 CCR0 capture: CCI0A input, compare: Out0
	TA3.1	25	N/A	I/O	TA3 CCR1 capture: CCI1A input, compare: Out1
	TA3.2	46	N/A	I/O	TA3 CCR2 capture: CCI2A input, compare: Out2
	TA3.3	74	N/A	I/O	TA3 CCR3 capture: CCI3A input, compare: Out3
	TA3.4	75	N/A	I/O	TA3 CCR4 capture: CCI4A input, compare: Out4
	TA3CLK	47	N/A	I	TA3 input clock

Table 4-3. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	SIGNAL NO.(1)		SIGNAL TYPE(2)	DESCRIPTION
		PZ	RGC		
UART	UCA0RXD	6	3	I	Receive data for eUSCI_A0 UART mode
	UCA0TXD	7	4	O	Transmit data for eUSCI_A0 UART mode
	UCA3RXD	98	N/A	I	Receive data for eUSCI_A3 UART mode
	UCA3TXD	99	N/A	O	Transmit data for eUSCI_A3 UART mode

4.5 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and diagrams of the multiplexed ports, see 节 6.12.

4.6 Buffer Types

Table 4-4 describes the buffer types that are referenced in Table 4-1 and Table 4-2.

Table 4-4. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
Analog (1)	3.0 V	N	N/A	N/A	N/A	See analog modules in Section 5 for details.
HVCMOS	13.0 V	Y	N/A	N/A	See the typical characteristics in Section 5.	
LVCMOS	3.0 V	Y(2)	Programmable	See 节 5.26.6.	See the typical characteristics in Section 5.	
Power (DVCC)(3)	3.0 V	N	N/A	N/A	N/A	SVSMH enables hysteresis on DVCC.
Power (AVCC)(3)	3.0 V	N	N/A	N/A	N/A	
Power (DVSS and AVSS)(3)	0 V	N	N/A	N/A	N/A	

(1) This is a switch, not a buffer.
(2) Only for input pins
(3) This is supply input, not a buffer.

4.7 Connections for Unused Pins

Table 4-5 lists the correct termination of all unused pins.

Table 4-5. Connection for Unused Pins(1)

PIN	POTENTIAL	COMMENT
AVCC	DV_{CC}	
AVSS	DV_{SS}	
VSW	Open	Leave VSW pin unconnected if DC/DC regulator operation is not required.
Px.0 to Px.7	Open	Set to port function, output direction, and leave unconnected on the PC board
RSTn/NMI	DV_{CC} or V_{CC}	47-kΩ pullup with 1.1-nF pulldown
PJ.4/TDI	Open	The JTAG TDI pin is shared with general-purpose I/O function (PJ.4). If not being used, this pin should be set to port function, output direction. When used as JTAG TDI pin, it should remain open.
PJ.5/TDO/SWO	DV_{CC} or V_{CC}	The JTAG TDO/SWO pin is shared with general-purpose I/O function (PJ.5). If not being used, this pin should be set to port function, output direction. When used as JTAG TDO/SWO pin, this pin requires an external pulldown.
SWDIOTMS	DV_{CC} or V_{CC}	This pin requires an external pullup.
SWCLKTCK	DV_{CC} or V_{CC}	This pin requires an external pulldown.

(1) For any unused pin with a secondary function that is shared with general-purpose I/O, follow the guidelines for the Px.0 to Px.7 pins.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at DVCC and AVCC pins to V_{SS}	–0.3	4.17	V
Voltage difference between DVCC and AVCC pins(2)		±0.3	V
Voltage applied to any pin(3)	–0.3	V_{CC} + 0.3 V (4.17 V MAX)	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (4)	–40	125	°C
Maximum junction temperature, T_J		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage differences between DVCC and AVCC exceeding the specified limits may cause malfunction of the device.
(3) All voltages referenced to V_{SS}.
(4) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (2)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) All pins pass HBM up to ±1000 V except the DVSS3 pin. The DVSS3 pin is used for TI internal test purposes. Connect the DVSS3 pin to supply ground on the customer application board.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range at all DVCC and AVCC pins (1) (2) (3)	At power up (with internal V_{CC} supervision)	1.71		3.7	V
		Normal operation with internal V_{CC} supervision	1.71		3.7	
		Normal operation without internal V_{CC} supervision	1.62		3.7	
V_{SS}	Supply voltage on all DVSS and AVSS pins			0		V
I_{INRUSH}	Inrush current into the V_{CC} pins(4)				100	mA
f_{MCLK}	Frequency of the CPU and AHB clock in the system(5)		0		24	MHz
T_A	Operating free-air temperature		–40		105(6)	°C
T_J	Operating junction temperature		–40		125	°C

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of ±0.1 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation. See Section 5.4 for decoupling capacitor recommendations.
(2) Supply voltage must not change faster than 1 V/ms. Faster changes can cause the VCCDET to trigger a reset even within the recommended supply voltage range.
(3) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(4) Does not include I/O currents (driven by application requirements).
(5) Operating frequency may require the flash to be accessed with wait states. See Section 5.8 for more details.
(6) T_J can be calculated using the equation $T_J = T_A + \theta_{JA} \times P_{Device}$. Section 5.25 provides the value of θ_{JA} for the different packages.

5.4 Recommended External Components(1) (2) (3)

			MIN	NOM	MAX	UNIT
C_{DVCC}	Capacitor on DVCC pin	For DC/DC operation(4)	3.3	4.7		µF
		For LDO-only operation	3.3	4.7		
C_{VCORE}	Capacitor on VCORE pin	For DC/DC operation, including capacitor tolerance	1.54	4.7	9	µF
		For LDO-only operation, including capacitor tolerance	70	100	9000	nF
C_{AVCC}	Capacitor on AVCC pin		3.3	4.7		µF
L_{VSW}	Inductor between VSW and VCORE pins for DC/DC		3.3	4.7	13	µH
$R_{LVSW-DCR}$	Allowed DCR for L_{VSW}			150	350	mΩ
$I_{SAT-LVSW}$	L_{VSW} saturation current		700			mA

(1) For optimum performance, select components that match the nominal values given in this table.
(2) See 节 7 for more details on component selection, placement, and related PCB design guidelines.
(3) Consider the tolerances of the capacitance and inductance values when choosing a component to ensure that the MIN and MAX limits are never exceeded.
(4) C_{DVCC} must not be smaller than C_{VCORE}.

5.5 Operating Mode V_{CC} Ranges

over operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	TEST CONDITIONS	MIN	MAX	UNIT
V_{CC_LDO} (1) (2)	AM_LDO_VCORE0 AM_LF_VCORE0 LPM0_LDO_VCORE0 LPM0_LF_VCORE0 LPM3_VCORE0 LPM4_VCORE0 LPM3.5	LDO active, SVSMH disabled	1.62	3.7	V
		LDO active, SVSMH enabled(3)	1.71	3.7	
$V_{CC\_DCDC\_DF0}$	AM_DCDC_VCORE0 LPM0_DCDC_VCORE0	DC/DC active, DC/DC operation not forced (DCDC_FORCE = 0), SVSMH enabled or disabled(4) (3)	2.0	3.7	V
$V_{CC\_DCDC\_DF1}$	AM_DCDC_VCORE0 LPM0_DCDC_VCORE0	DC/DC active, DC/DC operation forced (DCDC_FORCE = 1), SVSMH enabled or disabled(3)	1.8	3.7	V
$V_{CC\_VCORE\_OFF}$ (5)	LPM4.5	LDO disabled, SVSMH disabled	1.62	3.7	V
		LDO disabled, SVSMH enabled(3)	1.71	3.7	

(1) Flash remains active only in active modes and LPM0 modes.
(2) Low-frequency active, low-frequency LPM0, LPM3, LPM4, and LPM3.5 modes are based on LDO only.
(3) SVSMH should be enabled in HP mode of operation.
(4) When V_{CC} falls below the specified MIN value, the DC/DC operation switches to LDO automatically, as long as the V_{CC} drop is slower than the rate that is reliably detected. See Table 5-20 for more details.
(5) Core voltage is switched off in LPM4.5 mode.

5.6 Operating Mode CPU Frequency Ranges(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	f_{MCLK}		UNIT
			MIN	MAX	
$f_{AM\_LDO\_VCORE0}$	AM_LDO_VCORE0	Active mode with LDO as the core voltage regulator	0	24	MHz
$f_{AM\_DCDC\_VCORE0}$	AM_DCDC_VCORE0	Active mode with DC/DC as the core voltage regulator	0	24	MHz
$f_{AM\_LF\_VCORE0}$	AM_LF_VCORE0	Low-frequency active mode with LDO as the core voltage regulator	0	128	kHz

(1) The DMA can be operated at the same frequency as the CPU.

5.7 Operating Mode Peripheral Frequency Ranges

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	OPERATING MODE	DESCRIPTION	MIN	MAX	UNIT
$f_{AM\_LPM0\_VCORE0}$	AM_LDO_VCORE0	Peripheral frequency range in LDO or DC/DC-based active or LPM0 modes	0	12	MHz
	AM_DCDC_VCORE0				
	LPM0_LDO_VCORE0				
	LPM0_DCDC_VCORE0				
$f_{AM\_LPM0\_LF}$	AM_LF_VCORE0	Peripheral frequency range in low-frequency active or low-frequency LPM0 modes	0	128	kHz
	LPM0_LF_VCORE0				
f_{LPM3} (1)	LPM3_VCORE0	Peripheral frequency in LPM3 mode	0	128	kHz
f_{LPM4} (2)	LPM4_VCORE0	Peripheral frequency in LPM4 mode	0	128	kHz
$f_{LPM3.5}$ (1)	LPM3.5	Peripheral frequency in LPM3.5 mode	0	32.768	kHz

(1) Only RTC and WDT can be active.
(2) Peripherals available in LPM4 can be operational on external clocks.

5.8 Operating Mode Execution Frequency and Flash Wait-State Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	NUMBER OF FLASH WAIT STATES	FLASH READ MODE	MAXIMUM SUPPORTED MCLK FREQUENCY (1), (2)	UNIT
			AM_LDO_VCORE0, AM_DCDC_VCORE0	
$f_{MAX\_NRM\_FLWAIT0}$	0	Normal read mode	10	MHz
$f_{MAX\_NRM\_FLWAIT1}$	1	Normal read mode	21	MHz
$f_{MAX\_NRM\_FLWAIT2}$	2	Normal read mode	24	MHz
$f_{MAX\_ORM\_FLWAIT0}$	0	Other read modes (3)	6	MHz
$f_{MAX\_ORM\_FLWAIT1}$	1	Other read modes (3)	12	MHz
$f_{MAX\_ORM\_FLWAIT2}$	2	Other read modes (3)	18	MHz
$f_{MAX\_ORM\_FLWAIT3}$	3	Other read modes (3)	24	MHz

(1) Violation of the maximum frequency limitation for a given wait-state configuration results in nondeterministic data or instruction fetches from the flash memory.
(2) In low-frequency active modes, the flash can always be accessed with zero wait states, because the maximum MCLK frequency is limited to 128 kHz.
(3) Other read modes refer to Read Margin 0, Read Margin 1, Program Verify, and Erase Verify.

5.9 Current Consumption During Device Reset of the 100-Pin LQFP Package

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2) (3) (4)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
I_{RESET}	Current during device reset	2.2 V		690		µA
		3.0 V		760	1500	

(1) This parameter does not apply to the 64-pin VQFN package.
(2) Device held in reset through RSTn/NMI pin.
(3) Current measured into V_{CC}.
(4) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.

5.10 Current Consumption in LDO-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_LDO\_VCORE0,Flash}$ (6) (7) (8)	Flash	3.0 V	700	1500	2000	2900	3200	4250	4000	5100	µA
$I_{AM\_LDO\_VCORE0,SRAM}$ (9)	SRAM	3.0 V	640	1450	1600	2500	2675	3650	3750	4850	µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from Flash, stack, and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM, stack and data in SRAM.

5.11 Current Consumption in DC/DC-Based Active Modes – Dhrystone 2.1 Program

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_DCDC\_VCORE0,Flash}$ (6) (7) (8)	Flash	3.0 V	580	1050	1280	1850	1970	2650	2390	3200	µA
$I_{AM\_DCDC\_VCORE0,SRAM}$ (9)	SRAM	3.0 V	550	1000	1040	1750	1600	2350	2170	3000	µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks kept active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from flash. Stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

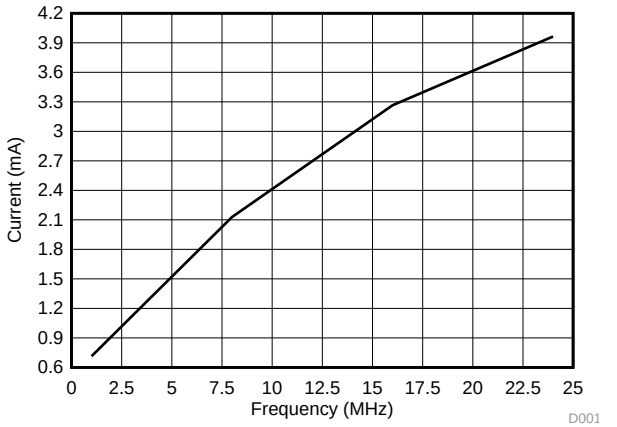
5.12 Current Consumption in Low-Frequency Active Modes – Dhrystone 2.1 Program

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	–40°C		25°C		60°C		105°C		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_LF\_VCORE0,\ Flash}$ (6) (7) (8)	Flash	2.2 V	88		96		108		305		µA
		3.0 V	88		96	120	108		305	600	
$I_{AM\_LF\_VCORE0,\ SRAM}$ (9)	SRAM	2.2 V	88		95		110		373		µA
		3.0 V	90		95	120	111		373	800	

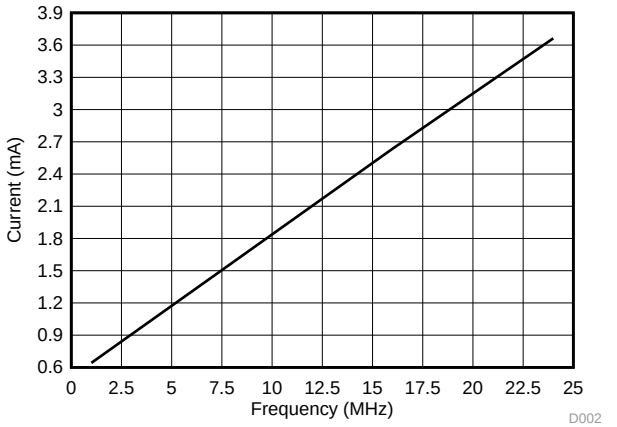
(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK, HSMCLK, and SMCLK sourced by REFO at 128 kHz.
(4) All peripherals are inactive.
(5) SRAM banks 0 and 1 enabled for execution from flash, and SRAM banks 0 to 3 enabled for execution from SRAM.
(6) Flash configured to 0 wait states.
(7) Device executing the Dhrystone 2.1 program. Code execution from Flash. Stack and data in SRAM.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data also in SRAM.

5.13 Typical Characteristics of Active Mode Currents for CoreMark Program



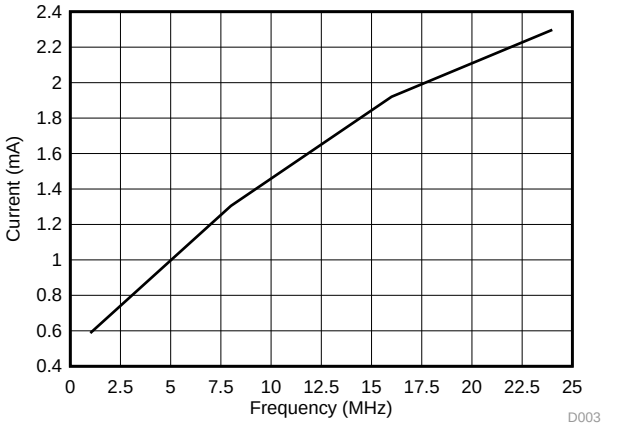
Flash Execution V_{CC} = 3 V T_A = 25°C

Figure 5-1. Frequency vs Current Consumption



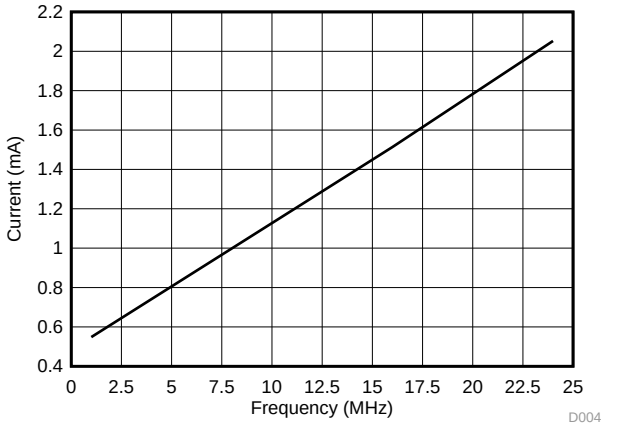
SRAM Execution V_{CC} = 3 V T_A = 25°C

Figure 5-2. Frequency vs Current Consumption



Flash Execution V_{CC} = 3 V T_A = 25°C

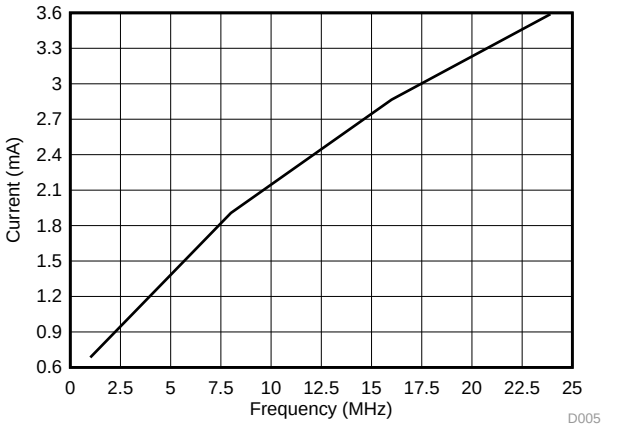
Figure 5-3. Frequency vs Current Consumption



SRAM Execution V_{CC} = 3 V T_A = 25°C

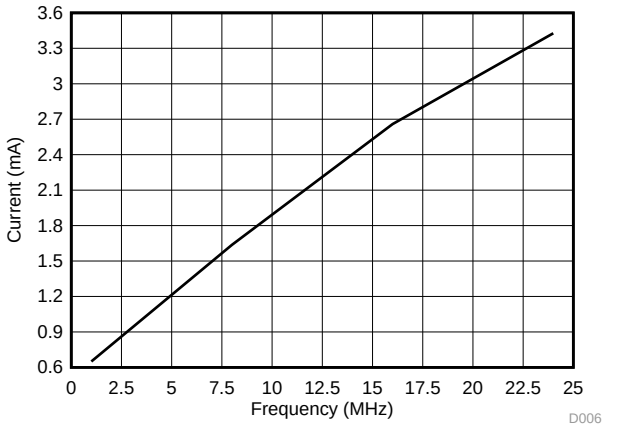
Figure 5-4. Frequency vs Current Consumption

5.14 Typical Characteristics of Active Mode Currents for Prime Number Program



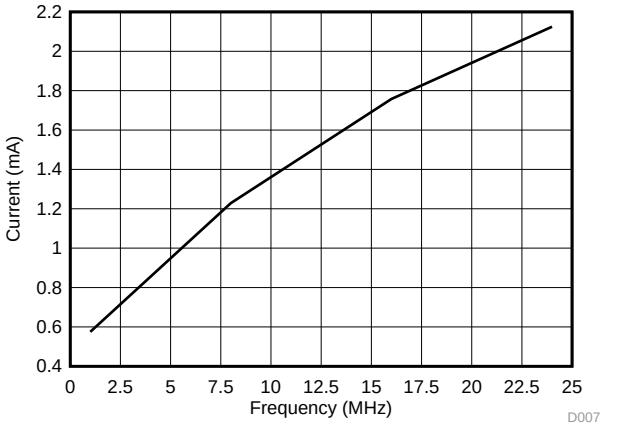
Flash Execution V_{CC} = 3 V T_A = 25°C

Figure 5-5. Frequency vs Current Consumption



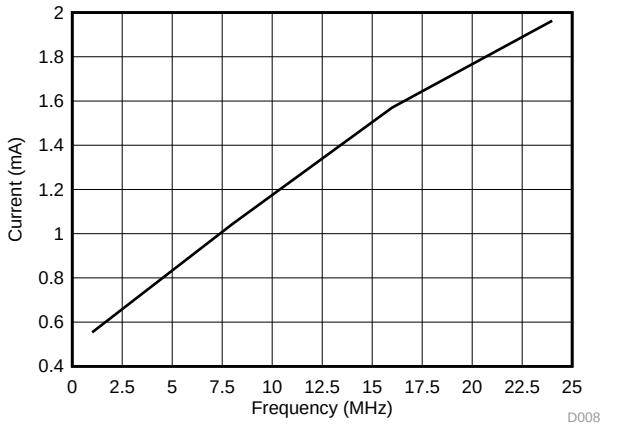
SRAM Execution V_{CC} = 3 V T_A = 25°C

Figure 5-6. Frequency vs Current Consumption



Flash Execution V_{CC} = 3 V T_A = 25°C

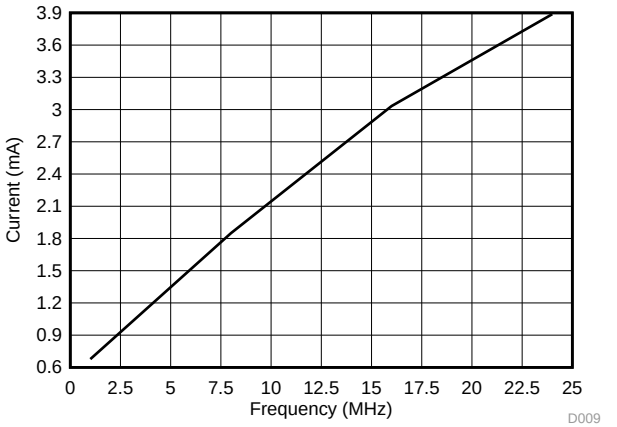
Figure 5-7. Frequency vs Current Consumption



SRAM Execution V_{CC} = 3 V T_A = 25°C

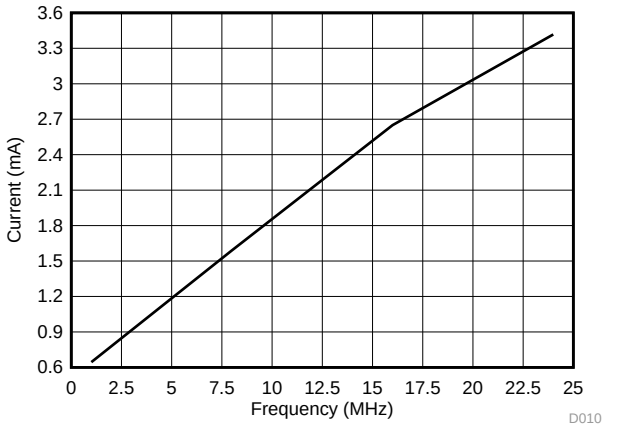
Figure 5-8. Frequency vs Current Consumption

5.15 Typical Characteristics of Active Mode Currents for Fibonacci Program



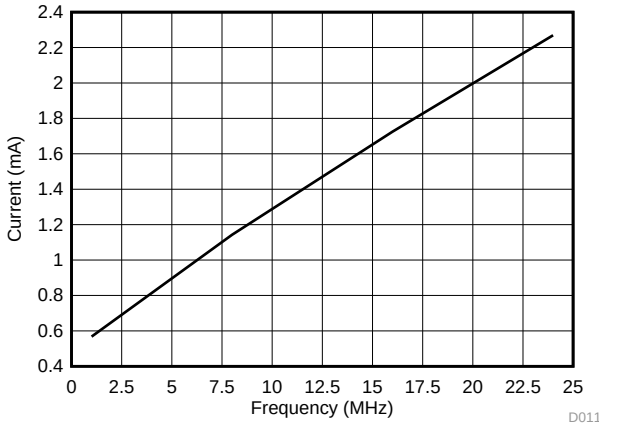
Flash Execution V_{CC} = 3 V T_A = 25°C

Figure 5-9. Frequency vs Current Consumption



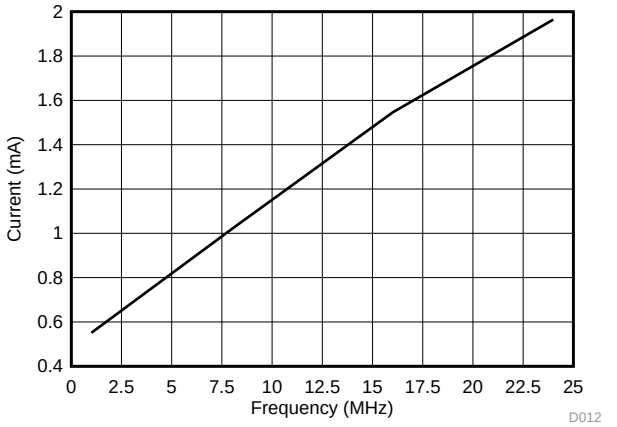
SRAM Execution V_{CC} = 3 V T_A = 25°C

Figure 5-10. Frequency vs Current Consumption



Flash Execution V_{CC} = 3 V T_A = 25°C

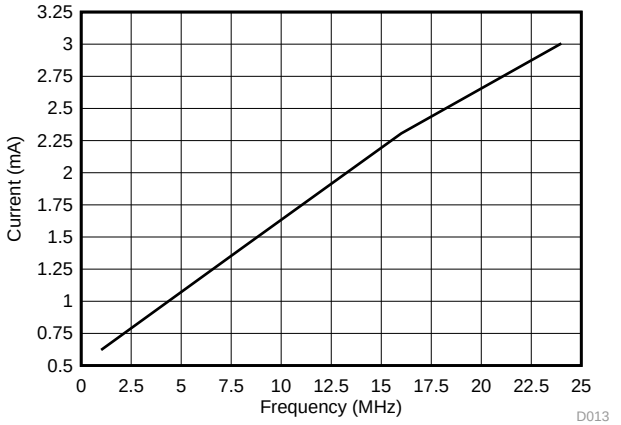
Figure 5-11. Frequency vs Current Consumption



SRAM Execution V_{CC} = 3 V T_A = 25°C

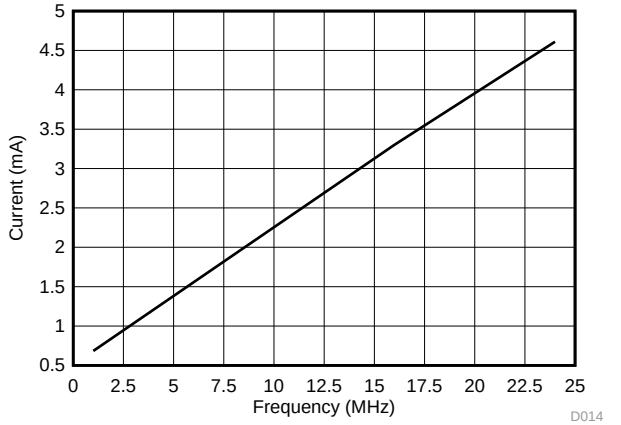
Figure 5-12. Frequency vs Current Consumption

5.16 Typical Characteristics of Active Mode Currents for While(1) Program



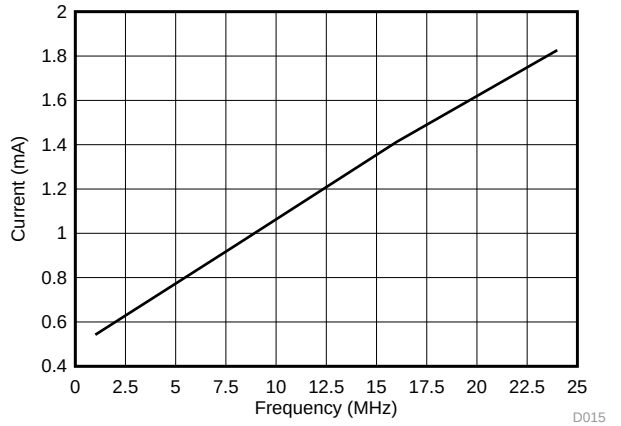
Flash Execution V_{CC} = 3 V T_A = 25°C

Figure 5-13. Frequency vs Current Consumption



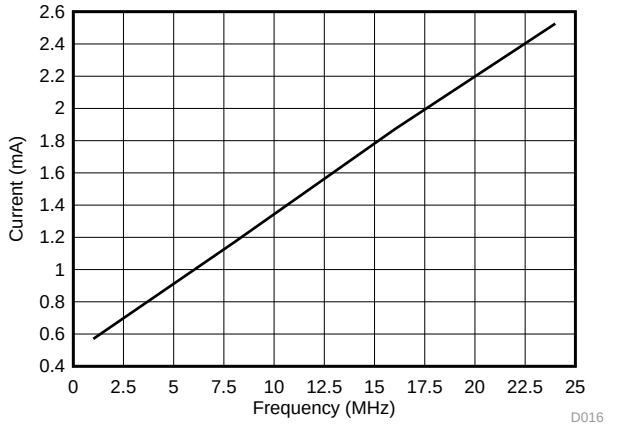
SRAM Execution V_{CC} = 3 V T_A = 25°C

Figure 5-14. Frequency vs Current Consumption



Flash Execution V_{CC} = 3 V T_A = 25°C

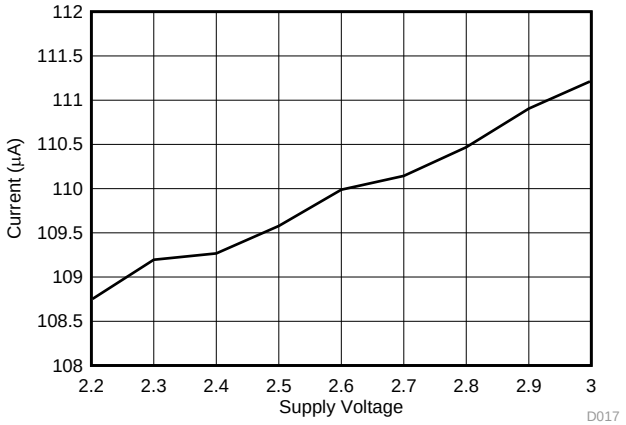
Figure 5-15. Frequency vs Current Consumption



SRAM Execution V_{CC} = 3 V T_A = 25°C

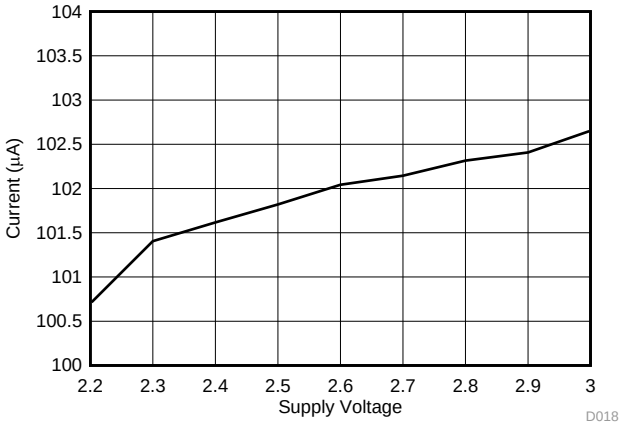
Figure 5-16. Frequency vs Current Consumption

5.17 Typical Characteristics of Low-Frequency Active Mode Currents for CoreMark Program



Flash Execution T_A = 25°C MCLK = 128 kHz

Figure 5-17. Supply Voltage vs Current Consumption



SRAM Execution T_A = 25°C MCLK = 128 kHz

Figure 5-18. Supply Voltage vs Current Consumption

5.18 Current Consumption in LDO-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0\_LDO\_VCORE0}$	2.2 V	520	1300	610	1400	710	1500	810	1600	µA
	3.0 V	520	1300	610	1400	710	1500	810	1600	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is off, flash or SRAM not being accessed.
(5) All SRAM banks are active.
(6) All peripherals are inactive.

5.19 Current Consumption in DC/DC-Based LPM0 Modes

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0\_DCDC\_VCORE0}$	2.2 V	490	1050	550	1150	620	1300	700	1350	µA
	3.0 V	485	950	535	1000	585	1050	650	1150	

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) CPU is off, flash or SRAM not being accessed.
(5) All SRAM banks are active.
(6) All peripherals are inactive.

5.20 Current Consumption in Low-Frequency LPM0 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		105°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0\_LF\_VCORE0}$	2.2 V	73		77		87		255		µA
	3.0 V	73		77	100	87		255	600	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) MCLK, HSMCLK, and SMCLK sourced by REFO at 128 kHz.
(4) All peripherals are inactive.
(5) Bank 0 of SRAM is active. All other banks are powered down.
(6) CPU is off, flash or SRAM not being accessed.

5.21 Current Consumption in LPM3, LPM4 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		105°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3\_VCORE0\_RTCLF}$ (7) (8)	2.2 V	13.1		14.4		15.7		29.5		µA
	3.0 V	13.1		14.4		15.7		29.5		
$I_{LPM3\_VCORE0\_RTCREFO}$ (9) (8)	2.2 V	13.5		14.9		16.2		30.6		µA
	3.0 V	13.6		15	19	16.3		30.7	48	
I_{LPM4_VCORE0} (10)	2.2 V	12.6		14		15.4		30.3		µA
	3.0 V	12.6		14		15.5		30.3		
$I_{IDLE,\ PG1,\ VCORE0}$	2.2 V	0.42		0.49		1.02		11		µA
	3.0 V	0.41		0.49		1.02		11		
$I_{IDLE,\ PG2,\ VCORE0}$	2.2 V	0.47		0.56		1.26		14		µA
	3.0 V	0.45		0.56		1.26		14		
$I_{IDLE,\ PG3,\ VCORE0}$	2.2 V	0.52		0.62		1.38		15.5		µA
	3.0 V	0.50		0.62		1.38		15.6		

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU is OFF, flash powered down.
(4) Bank 0 of SRAM retained, all other banks powered down.
(5) See Table 5-51 for details on additional current consumed for each extra bank that is enabled for retention.
(6) SVSMH is disabled.
(7) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(8) WDT module is disabled.
(9) RTC sourced by REFO.
(10) No peripherals operational in the device.

5.22 Current Consumption in LPM3 Modes With LCD

over operating free-air temperature range (unless otherwise noted) (1) (2) (3) (4) (5) (6)

PARAMETER	V_{CC}	–40°C		25°C		60°C		105°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3\_VCORE0\_LCDEXT}$ (7) (8) (9)	2.4 V	14.2		15.4		17.5		46.3		µA
	3.0 V	14.2		15.5		17.5		46.3		
$I_{LPM3\_VCORE0\_LCDINT}$ (7) (8) (10)	2.4 V	14.5		15.9		17.9		46.6		µA
	3.0 V	14.5		15.9		17.9		46.7		

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU is OFF, flash powered down.
(4) Bank 0 of SRAM retained, all other banks powered down.
(5) See Table 5-51 for details on additional current consumed for each extra Bank that is enabled for retention.
(6) SVSMH is disabled.
(7) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(8) WDT module is disabled.
(9) LCDMx = 11 (4-mux mode), LCDREXT = 1, LCDEXTBIAS = 1 (external biasing), LCD2B = 0 (1/3 bias), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz). Current through external resistors not included (voltage levels are supplied by test equipment). Even segments S0, S2,... = 0, odd segments S1, S3, ... = 1. No LCD panel load.
(10) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz) Even segments S0, S2, ... = 0, odd segments S1, S3, ... = 1. No LCD panel load.

5.23 Current Consumption in LPM3.5, LPM4.5 Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	–40°C		25°C		60°C		105°C		UNIT
		TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5\_RTCLF}$ (3) (4) (5) (6) (7)	2.2 V	9.2		10.5		11.7		26.6		µA
	3.0 V	9.2		10.5		11.7		26.7		
$I_{LPM3.5\_RTCREFO}$ (3) (4) (8) (6) (7)	2.2 V	9.6		10.9		12.2		27.3		µA
	3.0 V	9.7		11		12.3		27.5		
$I_{LPM4.5}$ (9) (7)	2.2 V	13		20		58		1335		nA
	3.0 V	15		24	500	68		1424	3300	

(1) Current measured into V_{CC}.
(2) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(3) CPU and flash are powered down.
(4) Bank 0 of SRAM retained, all other banks powered down.
(5) RTC sourced by LFXT. Effective load capacitance of LF crystal is 3.7 pF.
(6) WDT module is disabled.
(7) SVSMH is disabled.
(8) RTC sourced by REFO.
(9) No core voltage. CPU, flash, and all banks of SRAM powered down.

5.24 Current Consumption of Digital Peripherals

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{TIMER_A}	Timer_A configured as PWM timer with 50% duty cycle	5		µA/MHz
$I_{TIMER32}$	Timer32 enabled	3.5		µA/MHz
I_{UART}	eUSCI_A configured in UART mode	6.5		µA/MHz
I_{SPI}	eUSCI_A configured in SPI master mode	5		µA/MHz
I_{I2C}	eUSCI_B configured in I^2C master mode	5		µA/MHz
I_{WDT_A}	WDT_A configured in interval timer mode	6		µA/MHz
I_{RTC_C}	RTC_C enabled and sourced from 32-kHz LFXT	100		nA
I_{AES256}	AES256 active	19		µA/MHz
I_{CRC32}	CRC32 active	2		µA/MHz

5.25 Thermal Resistance Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

THERMAL METRIC(1)		PACKAGE	VALUE(2) (3)	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	LQFP-100 (PZ)	44.5	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		6.4	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		22.0	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		21.7	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.2	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	QFN-64 (RGC)	28.2	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance		7.7	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance		6.8	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter		6.7	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter		0.1	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance		0.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = Not applicable

5.26 Timing and Switching Characteristics

5.26.1 Reset Timing

Table 5-1 lists the latencies to recover from different types of resets.

Table 5-1. Reset Recovery Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{SOFT}	Latency from release of soft reset to first CPU instruction fetch		5		MCLK cycles
t_{HARD}	Latency from release of hard reset to release of soft reset		25		MCLK cycles
t_{POR}	Latency from release of device POR to release of hard reset		15	25	µs
$t_{COLDPWR, 100\ nF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 100 nF		410	1000	µs
$t_{COLDPWR, 4.7\ µF}$	Latency from a cold power-up condition to release of device POR, C_{VCORE} = 4.7 µF		530	1600	µs

(1) See 节 6.8.1 for details on the various classes of resets on the device

Table 5-2 lists the latencies to recover from an external reset applied on RSTn pin.

Table 5-2. External Reset Recovery Latencies(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{AM_RSTn}	External reset applied when device is in LDO-based or DC/DC-based active modes, MCLK = 1 to 24 MHz		4.5	ms
$t_{AMLF\_RSTn, 128\ kHz}$	External reset applied when device is in low-frequency active mode, MCLK = 128 kHz		5	ms
$t_{AMLF\_RSTn, 32\ kHz}$	External reset applied when device is in low-frequency active mode, MCLK = 32.768 kHz		6	ms
t_{LPM0_RSTn}	External reset applied when device is in LDO-based or DC/DC-based LPM0 modes, MCLK = 1 to 24 MHz		4.5	ms
$t_{LPM0LF\_RSTn, 128\ kHz}$	External reset applied when device is in low-frequency LPM0 mode, MCLK = 128 kHz		5	ms
$t_{LPM0LF\_RSTn, 32\ kHz}$	External reset applied when device is in low-frequency LPM0 mode, MCLK = 32.768 kHz		6	ms
$t_{LPM3\_LPM4\_RSTn}$	External reset applied when device is in LPM3 or LPM4 modes, MCLK = 24 MHz while entering LPM3 or LPM4 modes		4.5	ms
$t_{LPMx.5\_RSTn}$	External reset applied when device is in LPM3.5 or LPM4.5 modes		5	ms

(1) External reset is applied on RSTn pin, and the latency is measured from release of external reset to start of user application code.

5.26.2 Peripheral Register Access Timing

Table 5-3 lists the latency involved when CPU performs read or write access to peripheral registers.

Table 5-3. Peripheral Register Access Latency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t_{reg_access}	Number of CPU clock cycles required for read or write access to peripheral registers	2(1)	5(2)	MCLK cycles

(1) The bridge that connects CPU to peripherals runs at half of the speed of the CPU.
(2) The maximum value depends on the previous opcode executing in the CPU pipeline and the status of the bus (idle or busy performing data access).

5.26.3 Mode Transition Timing

Table 5-4 lists the latencies required to change between different active modes.

Table 5-4. Active Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
t_{OFF_AMLDO0}	Power Off	AM_LDO_VCORE0	From V_{CC} reaching 1.71 V to start of user application code		6	ms
$t_{AMLDO0\_AMDCDC0}$	AM_LDO_VCORE0	AM_DCDC_VCORE0	Transition from AM_LDO_VCORE0 to AM_DCDC_VCORE0 MCLK frequency = 24 MHz	20	30	µs
$t_{AMDCDC0\_AMLDO0}$	AM_DCDC_VCORE0	AM_LDO_VCORE0	Transition from AM_DCDC_VCORE0 to AM_LDO_VCORE0 MCLK frequency = 24 MHz	10	15	µs
t_{AMLDO0_AMLF0}	AM_LDO_VCORE0	AM_LF_VCORE0	Transition from AM_LDO_VCORE0 to AM_LF_VCORE0 SELM = 2, REFO frequency = 128 kHz	90	100	µs
t_{AMLF0_AMLDO0}	AM_LF_VCORE0	AM_LDO_VCORE0	Transition from AM_LF_VCORE0 to AM_LDO_VCORE0 SELM = 2, REFO frequency = 128 kHz	50	60	µs

Table 5-5 lists the latencies required to change between different active and LPM0 modes.

Table 5-5. LPM0 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{AMLDO0\_LPM0LDO0}$ (1)	AM_LDO_VCORE0	LPM0_LDO_VCORE0	Transition from AM_LDO_VCORE0 to LPM0_LDO_VCORE0	1		MCLK cycles
$t_{LPM0LDO0\_AMLDO0}$ (2)	LPM0_LDO_VCORE0	AM_LDO_VCORE0	Transition from LPM0_LDO_VCORE0 to AM_LDO_VCORE0 through I/O interrupt	3	4	MCLK cycles
$t_{AMDCDC0\_LPM0DCDC0}$ (1)	AM_DCDC_VCORE0	LPM0_DCDC_VCORE0	Transition from AM_DCDC_VCORE0 to LPM0_DCDC_VCORE0	1		MCLK cycles
$t_{LPM0DCDC0\_AMDCDC0}$ (2)	LPM0_DCDC_VCORE0	AM_DCDC_VCORE0	Transition from LPM0_DCDC_VCORE0 to AM_DCDC_VCORE0 through I/O interrupt	3	4	MCLK cycles
$t_{AMLF0\_LPM0LF0}$ (1)	AM_LF_VCORE0	LPM0_LF_VCORE0	Transition from AM_LF_VCORE0 to LPM0_LF_VCORE0	1		MCLK cycles
$t_{LPM0LF0\_AMLF0}$ (2)	LPM0_LF_VCORE0	AM_LF_VCORE0	Transition from LPM0_LF_VCORE0 to AM_LF_VCORE0 through I/O interrupt	3	4	MCLK cycles

(1) This is the latency between execution of WFI instruction by CPU to assertion of SLEEPING signal at CPU output.
(2) This is the latency between I/O interrupt event to deassertion of SLEEPING signal at CPU output.

Table 5-6 lists the latencies required to change between different active modes and LPM3 or LPM4 modes.

Table 5-6. LPM3, LPM4 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS		TYP	MAX	UNIT
t_{AMLDO0_LPMx} (1)	AM_LDO_VCORE0	LPM3_LPM4_VCORE0	Transition from AM_LDO_VCORE0 to LPM3 or LPM4 at VCORE0	SELM = 3. DCO frequency = 24 MHz	18	60	µs
$t_{LPMx\_AMLDO0\_NORIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from non-glitch filter type I/O	SELM = 3. DCO frequency = 24 MHz	8	9	µs
$t_{LPMx\_AMLDO0\_GFLTIO}$ (2)	LPM3_LPM4_VCORE0	AM_LDO_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1	SELM = 3. DCO frequency = 24 MHz	9	10	µs
$t_{AMLF0\_LPMx\_128k}$ (1)	AM_LF_VCORE0	LPM3_LPM4_VCORE0	Transition from AM_LF_VCORE0 to LPM3 or LPM4 at VCORE0	SELM = 2. REFO frequency = 128 kHz	255	290	µs
$t_{AMLF0\_LPMx\_32k}$ (1)	AM_LF_VCORE0	LPM3_LPM4_VCORE0	Transition from AM_LF_VCORE0 to LPM3 or LPM4 at VCORE0	SELM = 0. LFXT frequency = 32.768 kHz	980	1025	µs
$t_{LPMx\_AMLF0\_NORIO\_128k}$ (2)	LPM3_LPM4_VCORE0	AM_LF_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LF_VCORE0 through wake-up event from non-glitch filter type I/O	SELM = 2. REFO frequency = 128 kHz	45	55	µs
$t_{LPMx\_AMLF0\_NORIO\_32k}$ (2)	LPM3_LPM4_VCORE0	AM_LF_VCORE0	Transition from LPM3 or LPM4 at VCORE0 to AM_LF_VCORE0 through wake-up event from non-glitch filter type I/O	SELM = 0. LFXT frequency = 32.768 kHz	150	170	µs

(1) This is the latency from WFI instruction execution by CPU to LPM3 or LPM4 entry.
(2) This is the latency from I/O wake-up event to MCLK clock start at device pin.

Table 5-7 lists the latencies required to change to and from LPM3.5 and LPM4.5 modes.

Table 5-7. LPM3.5, LPM4.5 Mode Transition Latencies

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	ORIGINAL OPERATING MODE	FINAL OPERATING MODE	TEST CONDITIONS	TYP	MAX	UNIT
$t_{AMLDO0\_LPM3.5}$ (1)	AM_LDO_VCORE0	LPM3.5	Transition from AM_LDO_VCORE0 to LPM3.5	57	60	µs
$t_{AMDCDC0\_LPM3.5}$ (1)	AM_DCDC_VCORE0	LPM3.5	Transition from AM_DCDC_VCORE0 to LPM3.5	70	83	µs
$t_{AMLF0\_LPM3.5}$ (1)	AM_LF_VCORE0	LPM3.5	Transition from AM_LF_VCORE0 to LPM3.5	224	275	µs
$t_{AMLDO0\_LPM4.5}$ (2)	AM_LDO_VCORE0	LPM4.5	Transition from AM_LDO_VCORE0 to LPM4.5	57	60	µs
$t_{AMDCDC0\_LPM4.5}$ (2)	AM_DCDC_VCORE0	LPM4.5	Transition from AM_DCDC_VCORE0 to LPM4.5	68	81	µs
$t_{AMLF0\_LPM4.5}$ (2)	AM_LF_VCORE0	LPM4.5	Transition from AM_LF_VCORE0 to LPM4.5	230	248	µs
$t_{LPM3.5\_AMLDO0}$ (3)	LPM3.5	AM_LDO_VCORE0	Transition from LPM3.5 to AM_LDO_VCORE0	0.7	0.8	ms
$t_{LPM4.5\_AMLDO0\_SVSMON,\ 100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 100 nF	0.8	0.9	ms
$t_{LPM4.5\_AMLDO0\_SVSMON,\ 4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, C_{VCORE} = 4.7 µF	0.9	1.0	ms
$t_{LPM4.5\_AMLDO0\_SVSMOFF,\ 100\ nF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 100 nF	1.0	1.1	ms
$t_{LPM4.5\_AMLDO0\_SVSMOFF,\ 4.7\ µF}$ (3)	LPM4.5	AM_LDO_VCORE0	Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, C_{VCORE} = 4.7 µF	1.1	1.2	ms

(1) This is the latency from WFI instruction execution by CPU to LPM3.5 mode entry.
(2) This is the latency from WFI instruction execution by CPU to LPM4.5 mode entry.
(3) This is the latency from I/O wake-up event to start of user application code.

5.26.4 Clock Specifications

Table 5-8 lists the input requirement for the low-frequency crystal oscillator, LFXT.

Table 5-8. Low-Frequency Crystal Oscillator, LFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance	f_{OSC} = 32.768 kHz	16	40	65	kΩ
C_{LFXT}	Capacitance from LFXT input to ground and from LFXT output to ground(1)		7.4	12	24	pF
C_{SHUNT}	Crystal shunt capacitance		0.6	0.8	1.6	pF
C_m	Crystal motional capacitance		1	2	10	fF

(1) Does not include board parasitics. Package and board add additional capacitance to C_{LFXT}.

Table 5-9 lists the characteristics of the low-frequency crystal oscillator, LFXT.

Table 5-9. Low-Frequency Crystal Oscillator, LFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{VCC,LFXT}$	Current consumption(1)	f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR, C_{SHUNT}	3.0 V		100		nA
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF, Typical ESR, C_{SHUNT}			120		
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {2}, $C_{L,eff}$ = 9 pF, Typical ESR, C_{SHUNT}			150		
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR, C_{SHUNT}			170		
f_{LFXT}	LFXT oscillator crystal frequency	LFXTBYPASS = 0(2)			32.768		kHz
DC_{LFXT}	LFXT oscillator duty cycle	f_{LFXT} = 32.768 kHz(2)		30%		70%	
$f_{LFXT,SW}$	LFXT oscillator logic-level square-wave input frequency	LFXTBYPASS = 1(3) (4)		10	32.768	50	kHz
$DC_{LFXT, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		30%		70%	
OA_{LFXT}	Oscillation allowance for LF crystals(5)	LFXTBYPASS = 0, LFXTDRIVE = {1}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 6 pF		200	240		kΩ
		LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32.768 kHz, $C_{L,eff}$ = 12 pF		300	340		

(1) Total current measured on both AVCC and DVCC supplies.
(2) Measured at ACLK pin.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{LFXT, SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

Table 5-9. Low-Frequency Crystal Oscillator, LFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{LFXIN}	Integrated load capacitance at LFXIN terminal(6) (7)				2		pF
C_{LFXOUT}	Integrated load capacitance at LFXOUT terminal(6) (7)				2		pF
$t_{START,LFXT}$	Start-up time(8)	f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR, C_{SHUNT}, FCNTLF_EN = 0(2)	3.0 V		1.1		s
		f_{OSC} = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR, C_{SHUNT}, FCNTLF_EN = 0(2)			1.3		
$f_{Fault,LFXT}$	Oscillator fault frequency(9) (10)			1		3	kHz

(6) This represents all the parasitic capacitance present at the LFXIN and LFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} are the total capacitance at the LFXIN and LFXOUT terminals, respectively.
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12 pF. Maximum shunt capacitance of 1.6 pF. Because the PCB adds additional capacitance, so it must also be considered in the overall capacitance. TI recommends verifying that the recommended effective load capacitance of the selected crystal is met.
(8) Does not include programmable start-up counter.
(9) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition will set the fault flag.
(10) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-10 lists the input requirements for the high-frequency crystal oscillator, HFXT.

Table 5-10. High-Frequency Crystal Oscillator, HFXT, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ESR	Crystal equivalent series resistance	f_{OSC} = 1 MHz to ≤ 4 MHz		75	150	Ω
		f_{OSC} = > 4 MHz to ≤ 8 MHz		75	150	
		f_{OSC} = > 8 MHz to ≤ 16 MHz		40	80	
		f_{OSC} = > 16 MHz to ≤ 24 MHz		30	60	
C_{HFXT}	Capacitance from HFXT input to ground and from HFXT output to ground	f_{OSC} = 1 MHz to 24 MHz	28	32	36	pF
C_{SHUNT}	Crystal shunt capacitance	f_{OSC} = 1 MHz to 24 MHz	1	3	7	pF
C_m	Crystal motional capacitance	f_{OSC} = 1 MHz to 24 MHz	3	7	30	fF

Table 5-11 lists the characteristics of the high-frequency crystal oscillator, HFXT.

Table 5-11. High-Frequency Crystal Oscillator, HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,HFXT}$	HFXT oscillator crystal current HF mode at typical ESR	f_{OSC} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}	3.0 V		40		µA
		f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}			60		
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}			100		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}			180		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}			260		
f_{HFXT}	HFXT oscillator crystal frequency, crystal mode	HFXTBYPASS = 0, HFFREQ = 0 (1)		1		4	MHz
		HFXTBYPASS = 0, HFFREQ = 1 (1)		4.01		8	
		HFXTBYPASS = 0, HFFREQ = 2 (1)		8.01		16	
		HFXTBYPASS = 0, HFFREQ = 3 (1)		16.01		24	
DC_{HFXT}	HFXT oscillator duty cycle	Measured at MCLK or HSMCLK, f_{HFXT} = 1 MHz to 24 MHz		40%	50%	60%	
$f_{HFXT,SW}$	HFXT oscillator logic-level square-wave input frequency, bypass mode	HFXTBYPASS = 1 (1) (2)		0.8		24	MHz
$DC_{HFXT,\ SW}$	HFXT oscillator logic-level square-wave input duty cycle	HFXTBYPASS = 1, External clock used as a direct source to MCLK or HSMCLK with no divider (DIVM = 0 or DIVHS = 0).		45%		55%	
		HFXTBYPASS = 1, External clock used as a direct source to MCLK or HSMCLK with divider (DIVM > 0 or DIVHS > 0) or not used as a direct source to MCLK or HSMCLK.		40%		60%	
OA_{HFXT}	Oscillation allowance for HFXT crystals (3)	HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $f_{HFXT,HF}$ = 1 MHz, $C_{L,eff}$ = 16 pF		1225	5000		Ω
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $f_{HFXT,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF		640	1250		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $f_{HFXT,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF		360	750		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF		200	425		
		HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF		135	275		

(1) Maximum frequency of operation of the entire device cannot be exceeded.
(2) When HFXTBYPASS is set, HFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet. Duty cycle requirements are defined by $DC_{HFXT,\ SW}$.
(3) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

Table 5-11. High-Frequency Crystal Oscillator, HFXT (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{START,HFXT}$	Start-up time(4)	f_{OSC} = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}, FCNTHF_EN = 0	3.0 V		4		ms
		f_{OSC} = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}, FCNTHF_EN = 0			1.8		
		f_{OSC} = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}, FCNTHF_EN = 0			0.7		
		f_{OSC} = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}, FCNTHF_EN = 0			0.6		
		f_{OSC} = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR , C_{SHUNT}, FCNTHF_EN = 0			450		µs
C_{HFXIN}	Integrated load capacitance at HFXIN terminal(5) (6)				2		pF
C_{HFXOUT}	Integrated load capacitance at HFXOUT terminal(5) (6)				2		pF
$f_{Fault,HFXT}$	Oscillator fault frequency(7) (8)			400		700	kHz

(4) Does not include programable start-up counter.
(5) This represents all the parasitic capacitance present at the HFXIN and HFXOUT terminals, respectively, including parasitic bond and package capacitance. The effective load capacitance, $C_{L,eff}$ can be computed as $C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT})$, where C_{IN} and C_{OUT} is the total capacitance at the HFXIN and HFXOUT terminals, respectively.
(6) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 14 pF, 16 pF, and 18 pF. Maximum shunt capacitance of 7 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. TI recommends verifying that the recommended effective load capacitance of the selected crystal is met.
(7) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX might set the flag. A static condition or stuck at fault condition will set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-12 lists the characteristics of the DCO.

Table 5-12. DCO

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, T_J	MIN	TYP	MAX	UNIT
f_{RSEL0_CTR}	DCO center frequency accuracy for range 0 with calibrated factory settings	Internal resistor mode, DCORSEL = 0, DCOTUNE = 0		1.427	1.5	1.573	MHz
		External resistor mode, DCORSEL = 0, DCOTUNE = 0		1.479	1.5	1.521	
f_{RSEL1_CTR}	DCO center frequency accuracy for range 1 with calibrated factory settings	Internal resistor mode, DCORSEL = 1, DCOTUNE = 0		2.855	3	3.145	MHz
		External resistor mode, DCORSEL = 1, DCOTUNE = 0		2.959	3	3.041	
f_{RSEL2_CTR}	DCO center frequency accuracy for range 2 with calibrated factory settings	Internal resistor mode, DCORSEL = 2, DCOTUNE = 0		5.710	6	6.290	MHz
		External resistor mode, DCORSEL = 2, DCOTUNE = 0		5.918	6	6.082	
f_{RSEL3_CTR}	DCO center frequency accuracy for range 3 with calibrated factory settings	Internal resistor mode, DCORSEL = 3, DCOTUNE = 0		11.421	12	12.579	MHz
		External resistor mode, DCORSEL = 3, DCOTUNE = 0		11.836	12	12.164	
f_{RSEL4_CTR}	DCO center frequency accuracy for range 4 with calibrated factory settings	Internal resistor mode, DCORSEL = 4, DCOTUNE = 0		22.842	24	25.158	MHz
		External resistor mode, DCORSEL = 4, DCOTUNE = 0		23.673	24	24.327	
df_{DCO}/dT	DCO frequency drift with temperature (1)	Internal resistor mode, At fixed voltage	1.62 V to 3.7 V			250	ppm/°C
		External resistor mode (2) At fixed voltage	1.62 V to 3.7 V			60	
df_{DCO}/dV_{CC}	DCO frequency voltage drift with voltage (3)	At fixed temperature, applicable for both DCO Internal and External resistor modes	–40°C to 125 °C			0.1	%/V
f_{RSEL0}	DCO frequency range 0	DCORSEL = 0 DCO internal or external resistor mode	3.0 V, 25℃	0.98		2.26	MHz
f_{RSEL1}	DCO frequency range 1	DCORSEL = 1 DCO internal or external resistor mode	3.0 V, 25℃	1.96		4.51	MHz
f_{RSEL2}	DCO frequency range 2	DCORSEL = 2 DCO internal or external resistor mode	3.0 V, 25℃	3.92		9.02	MHz
f_{RSEL3}	DCO frequency range 3	DCORSEL = 3 DCO internal or external resistor mode	3.0 V, 25℃	7.84		18.04	MHz
f_{RSEL4}	DCO frequency range 4	DCORSEL = 4 DCO internal or external resistor mode	3.0 V, 25℃	15.68		36.07	MHz
f_{DCO_DC}	Duty cycle			47%	50%	53%	
t_{DCO_JITTER}	DCO period jitter	DCORSEL = 4, DCOTUNE = 0			80	120	ps
		DCORSEL = 3, DCOTUNE = 0			115	170	
		DCORSEL = 2, DCOTUNE = 0			160	240	
		DCORSEL = 1, DCOTUNE = 0			225	340	
		DCORSEL = 0, DCOTUNE = 0			450	550	
t_{DCO_STEP}	Step size	Step size of the DCO			0.2%		

(1) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(2) Does not include temperature coefficient of external resistor.
The recommended value of external resistor at DCOR pin: 91 kΩ, 0.1%, ±25 ppm/℃.
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-12. DCO (continued)

over recommended ranges of supply voltage and operating junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}, T_J	MIN	TYP	MAX	UNIT
$t_{DCO\_SETTLE\_RANGE}$	DCO settling from worst case DCORSELn to DCORSELm	DCO settled to within 1.5% of steady state frequency				10	µs
$t_{DCO\_SETTLE\_TUNE}$	DCO settling worst case DCOTUNEn to DCOTUNEm within any DCORSEL setting	DCO settled to within 1.5% of steady state frequency				10	µs
t_{START}	DCO start-up time(4)	DCO settled to within 0.5% of steady state frequency			5		µs

(4) The maximum parasitic capacitance at the DCO external resistance pin (DCOR) should not exceed 5 pF to ensure the specified DCO start-up time.

Table 5-13 lists the overall tolerance of the DCO.

Table 5-13. DCO Overall Tolerance

RESISTOR OPTION	TEMPERATURE CHANGE(1)	TEMPERATURE DRIFT (%)	VOLTAGE CHANGE	VOLTAGE DRIFT (%)	OVERALL DRIFT (%)	OVERALL ACCURACY (%)
Internal resistor	–40°C to 125 °C	±4.125	1.62 V to 3.7 V	±0.2	±4.325	±4.825
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 125 °C	±4.125	0 V	0	±4.125	±4.625
External resistor with 25-ppm TCR	–40°C to 125 °C	±0.66	1.62 V to 3.7 V	±0.2	±0.86	±1.36
	0°C	0	1.62 V to 3.7 V	±0.2	±0.2	±0.7
	–40°C to 125 °C	±0.66	0 V	0	±0.66	±1.16

(1) Corresponds to junction temperature T_J.

Table 5-14 lists the characteristics of the internal very-low-power low-frequency oscillator (VLO).

Table 5-14. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VLO}	Current consumption(1)			50		nA
f_{VLO}	VLO frequency		6	9.4	18	kHz
df_{VLO}/d_T	VLO frequency temperature drift(2)			0.1		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift(3)			0.2		%/V
DC_{VLO}	Duty cycle		40%	50%	60%	

(1) Current measured on DVCC supply
(2) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-15 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 32.768-kHz mode.

Table 5-15. Internal-Reference Low-Frequency Oscillator (REFO) – 32.768-kHz Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO current consumption(2)				0.6		µA
f_{REFO}	REFO frequency calibrated				32.768		kHz
	REFO absolute tolerance calibrated	T_A = –40°C to 105°C				±4%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift(3)				0.012		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift(4)				0.2		%/V
DC_{REFO}	REFO duty cycle			40%	50%	60%	

(1) REFO is configured to 32.768-kHz mode with REFOFSEL = 0.
(2) Total current measured on both AVCC and DVCC supplies.
(3) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-16 lists the characteristics of the internal-reference low-frequency oscillator (REFO) in 128-kHz mode.

Table 5-16. Internal-Reference Low-Frequency Oscillator (REFO) – 128-kHz Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
REFO	REFO current consumption(2)				1		µA
f_{REFO}	REFO frequency calibrated				128		kHz
	REFO absolute tolerance calibrated	T_A = –40°C to 105°C				±6%	
		T_A = 25°C	3 V			±1.5%	
df_{REFO}/d_T	REFO frequency temperature drift(3)				0.018		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift(4)				0.4		%/V
DC_{REFO}	REFO duty cycle			40%	50%	60%	

(1) REFO is configured to 128-kHz mode with REFOFSEL = 1.
(2) Total current measured on both AVCC and DVCC supplies.
(3) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-17 lists the characteristics of the module oscillator (MODOSC).

Table 5-17. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{MODOSC}	Current consumption (1)				50		µA
f_{MODOSC}	MODOSC frequency			23	25	27	MHz
df_{MODOSC}/dT	MODOSC frequency temperature drift (2)				0.02		%/°C
df_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift (3)				0.3		%/V
DC_{MODOSC}	Duty cycle			40%	50%	60%	

(1) Total current measured on both AVCC and DVCC supplies.
(2) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

Table 5-18 lists the characteristics of the system oscillator (SYSOSC).

Table 5-18. System Oscillator (SYSOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SYSOSC}	Current consumption (1)				30		µA
f_{SYSOSC}	SYSOSC frequency			4.25	5.0	5.75	MHz
df_{SYSOSC}/dT	SYSOSC frequency temperature drift (2)				0.03		%/°C
$df_{SYSOSC}/dVCC$	SYSOSC frequency supply voltage drift (3)				0.5		%/V
DC_{SYSOSC}	Duty cycle			40%	50%	60%	

(1) Current measured on AVCC supply.
(2) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C) / (125°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

5.26.5 Power Supply System

Table 5-19 lists the LDO V_{CORE} regulator characteristics.

Table 5-19. V_{CORE} Regulator (LDO) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CORE0-HP}$	Static VCORE voltage level 0 in active and LPM0 modes	Device power modes AM_LDO_VCORE0 and LPM0_LDO_VCORE0	1.12	1.2	1.28	V
$V_{CORE0-LF}$	Static VCORE voltage level 0 in low-frequency active and low-frequency LPM0 modes	Device power mode AM_LF_VCORE0	1.12	1.2	1.28	V
$V_{CORE0-LPM34}$	Static VCORE voltage level 0 in LPM3 and LPM4	Device power modes LPM3 and LPM4	1.08	1.2	1.32	V
$V_{CORE0-LPM35}$	Static VCORE voltage level 0 in LPM3.5 mode	Device power mode LPM3.5	1.08	1.2	1.32	V
$I_{INRUSH-ST}$	Inrush current at start-up	Device power up			200	mA
$I_{PEAK-LDO}$	Peak current drawn by LDO from DV_{CC}				350	mA
$I_{SC-coreLDO}$	Short-circuit current limit for core LDO	Measured when output is shorted to ground			300	mA

Table 5-20 lists the DC/DC V_{CORE} regulator characteristics.

Table 5-20. V_{CORE} Regulator (DC/DC) Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC-DCDC}$	Allowed DV_{CC} range for DC/DC operation	DCDC_FORCE = 1	1.8		3.7	V
V_{DCDC_SO} (1)	DC/DC to LDO switch over voltage	dDV_{CC}/dt = 1 V/ms, DCDC_FORCE = 0	1.8		2.0	V
$V_{CORE0-DCDC}$	Static VCORE voltage level 0 in DC/DC high-performance modes	Device power modes AM_DCDC_VCORE0, LPM0_DCDC_VCORE0	1.12	1.2	1.28	V
$I_{PEAK-DCDC}$	Peak current drawn by DC/DC from DVCC				300	mA
$I_{SC-DCDC}$	Short-circuit current limit for DC/DC	Measured when output is shorted to ground			500	mA

(1) When DV_{CC} falls below this voltage, internally the regulator switches over to LDO from DC/DC.

Table 5-21 lists the VCCDET characteristics.

Table 5-21. PSS, VCCDET

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC\_VCCDET-}$	VCCDET power-down level (trip point with falling V_{CC})	dDV_{CC}/d_t < 3 V/s (1)	0.64	1.12	1.55	V
$V_{VCC\_VCCDET+}$	VCCDET power-up level (trip point with rising V_{CC})	dDV_{CC}/d_t < 3 V/s (1)	0.70	1.18	1.59	V
$V_{VCC\_VCC\_hys}$	VCCDET hysteresis		30	65	100	mV

(1) The VCCDET levels are measured with a slow-changing supply. Faster slopes can result in different levels.

Table 5-22 lists the SVSMH characteristics.

Table 5-22. PSS, SVSMH

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SVSMH}	$SVSM_H$ current consumption, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0		7	10	µA
$V_{SVSMH-,HP}$	$SVSM_H$ threshold level during high-performance mode (falling DV_{CC})	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.59	1.64	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.0	2.06	2.12	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.2	2.26	2.32	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.4	2.47	2.54	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.7	2.79	2.88	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.9	3.0	3.1	
$V_{SVSMH+,HP}$	$SVSM_H$ threshold level; High Performance Mode [rising DV_{CC}]	SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	V
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC (dDV_{CC}/dt < 1V/s)	1.6	1.66	1.71	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC (dDV_{CC}/dt < 1V/s)	2.02	2.07	2.14	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC (dDV_{CC}/dt < 1V/s)	2.22	2.27	2.34	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC (dDV_{CC}/dt < 1V/s)	2.42	2.48	2.56	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC (dDV_{CC}/dt < 1V/s)	2.72	2.8	2.9	
		SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC (dDV_{CC}/dt < 1V/s)	2.92	3.01	3.12	
V_{SVSMH_hys}	$SVSM_H$ hysteresis			15	30	mV
$t_{PD,SVSMH}$	SVS_H propagation delay, high-performance mode	SVSMHOFF = 0, SVSMHLP = 0, very fast dV_{DVCC}/dt		3	10	µs
$t_{(SVSMH)}$	$SVSM_H$ on or off delay time	SVSMHOFF = 1 → 0, SVSMHLP = 0 (1)		17	40	µs

(1) If the $SVSM_H$ is disabled in active mode and is enabled before entering a low-power mode of the device (LPM3, LPM4, LPM3.5, or LPM4.5) ensure that sufficient time has elapsed since enabling of the module before entry into the device low-power mode to allow for successful wake up of the SVSMH module per the $SVSM_H$ on or off delay time specification. Otherwise, $SVSM_H$ may trip, causing the device to reset and wake up from the low-power mode.

5.26.6 Digital I/Os

Table 5-23 lists the characteristics of the digital inputs.

Table 5-23. Digital Inputs (Applies to Both Normal and High-Drive I/Os)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2.2 V	0.99		1.65	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2.2 V	0.55		1.21	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2.2 V	0.32		0.84	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$		20	30	40	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			11		pF
$C_{I,ana}$	Input capacitance, port pins shared with analog functions	$V_{IN} = V_{SS}$ or V_{CC}			11		pF
$I_{lkg,ndio}$	Normal I/O high-impedance input leakage current	See (1)(2)	2.2 V, 3 V			±30	nA
$I_{lkg,hdio}$	High-drive I/O high-impedance input leakage current	See (1)(2)	2.2 V, 3 V			±20	nA
t_{int}	External interrupt timing (external trigger pulse duration to set interrupt flag)	Ports with interrupt capability and without glitch filter (3)	2.2 V, 3 V	20			ns
		Ports with interrupt capability and with glitch filter but glitch filter disabled (GLTFLT_EN = 0) (3)	2.2 V, 3 V	20			
		Ports with interrupt capability and with glitch filter, glitch filter enabled (GLTFTL_EN = 1) (4)	2.2 V, 3 V	0.25		1	µs
t_{RST}	External reset pulse duration on RSTn pin(5)		2.2 V, 3 V	1			µs

(1) The input leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The input leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_{int} is met. It may be set by trigger signals shorter than t_{int}.
(4) A trigger pulse duration less than the MIN value is always filtered, and a trigger pulse duration greater than the MAX value is always passed. The trigger pulse may or may not be filtered if the duration is between the MIN and MAX values.
(5) Not applicable if the RSTn/NMI pin configured as NMI.

Table 5-24 lists the output characteristics of the normal-drive digital I/Os. See 图 5-19, 图 5-20, 图 5-21, and 图 5-22 for the typical characteristics graphs.

Table 5-24. Digital Outputs, Normal I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(2)		V_{SS}	V_{SS} + 0.60	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.2 V, C_L = 20 pF, R_L (4) (5)	1.62 V	12		MHz
			2.2 V	12		
			3.0 V	12		
$d_{Px.y}$	Port output duty cycle (with RC load)	VCORE = 1.2 V, C_L = 20 pF, R_L (4) (5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.2 V, C_L = 20 pF(5)	1.62 V	12		MHz
			2.2 V	12		
			3.0 V	12		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.2 V, C_L = 20 pF(5)	1.62 V	40%	60%	
			2.2 V	40%	60%	
			3.0 V	45%	55%	
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{rise,ana}$	Port output rise time, port pins with shared analog functions	C_L = 20 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
$t_{fall,ana}$	Port output fall time, port pins with shared analog functions	C_L = 20 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		4	

(1) The maximum total current ($I_{(OHmax)}$ and $I_{(OLmax)}$) for all outputs combined must not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current ($I_{(OHmax)}$ and $I_{(OLmax)}$) for all outputs combined must not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies up to at least the specified limit and might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured from 20% of V_{CC} to 80% of V_{CC}.
(7) Measured from 80% of V_{CC} to 20% of V_{CC}.

Table 5-25 lists the output characteristics of the high-drive digital I/Os. See 图 5-23, 图 5-24, 图 5-25, and 图 5-26 for the typical characteristics graphs.

Table 5-25. Digital Outputs, High-Drive I/Os

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –5 mA(1)	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –10 mA(1)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –20 mA(2)		V_{CC} – 0.50	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 5 mA(1)	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 10 mA(1)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 20 mA(2)		V_{SS}	V_{SS} + 0.50	
$f_{Px.y}$	Port output frequency (with RC load)(3)	VCORE = 1.2 V, C_L = 80 pF, R_L (4) (5)	1.62 V	12		MHz
			2.2 V	12		
			3.0 V	12		
$d_{Px.y}$	Port output duty cycle (with RC load)	VCORE = 1.2 V, C_L = 80 pF, R_L (4) (5)	1.62 V	45%	55%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
f_{Port_CLK}	Clock output frequency(3)	VCORE = 1.2 V, C_L = 80 pF(5)	1.62 V	12		MHz
			2.2 V	12		
			3.0 V	12		
d_{Port_CLK}	Clock output duty cycle	VCORE = 1.2 V, C_L = 80 pF(5)	1.62 V	45%	55%	
			2.2 V	45%	55%	
			3.0 V	45%	55%	
t_{rise}	Port output rise time	C_L = 80 pF (6)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	
t_{fall}	Port output fall time	C_L = 80 pF (7)	1.62 V		8	ns
			2.2 V		5	
			3.0 V		3	

(1) The maximum total current ($I_{(OHmax)}$ and $I_{(OLmax)}$) for all outputs combined must not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current ($I_{(OHmax)}$ and $I_{(OLmax)}$) for all outputs combined must not exceed ±100 mA to hold the maximum voltage drop specified.
(3) The port can output frequencies at least up to the specified limit, and it might support higher frequencies.
(4) A resistive divider with 2 × R1 and R1 = 3.2 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 80 pF is connected to the output to V_{SS}.
(5) The output voltage reaches at least 20% and 80% V_{CC} at the specified toggle frequency.
(6) Measured from 20% of V_{CC} to 80% of V_{CC}.
(7) Measured from 80% of V_{CC} to 20% of V_{CC}.

Table 5-26 lists the frequencies of the pin-oscillator ports. See 图 5-27 and 图 5-28 for the typical characteristics graphs.

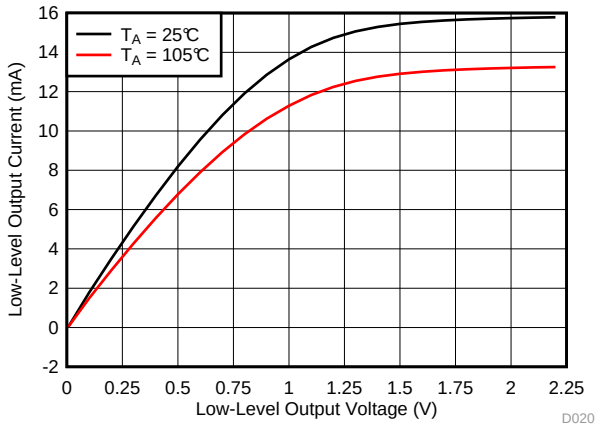
Table 5-26. Pin-Oscillator Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{Px.y}$	Pin-oscillator frequency	Px.y, C_L = 10 pF(1)	3.0 V		1900		kHz
		Px.y, C_L = 20 pF(1)	3.0 V		1150		

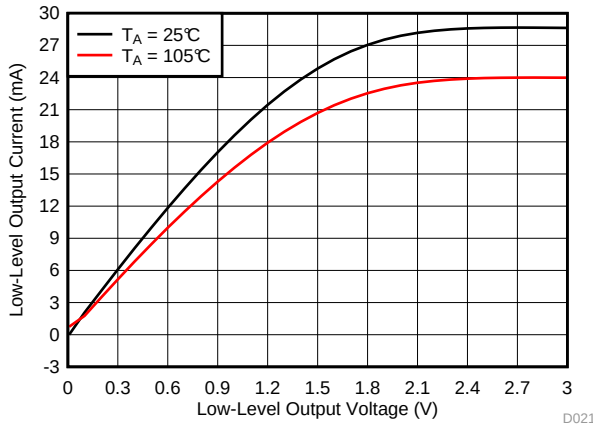
(1) C_L is the external load capacitance connected from the output to VSS and includes all parasitic effects such as PCB traces.

5.26.6.1 Typical Characteristics, Normal-Drive I/O Outputs at 3.0 V and 2.2 V



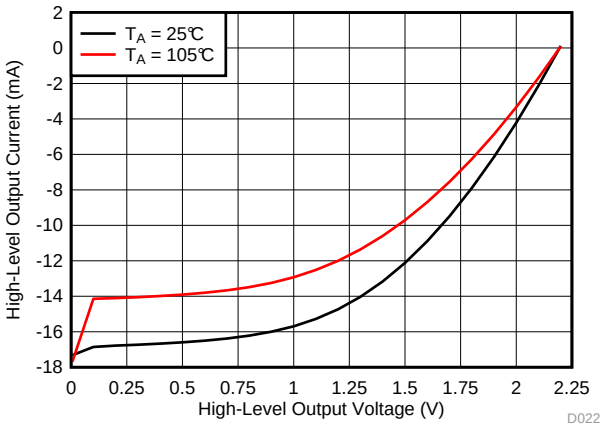
V_{CC} = 2.2 V P7.0

图 5-19. Low-Level Output Voltage vs Low-Level Output Current



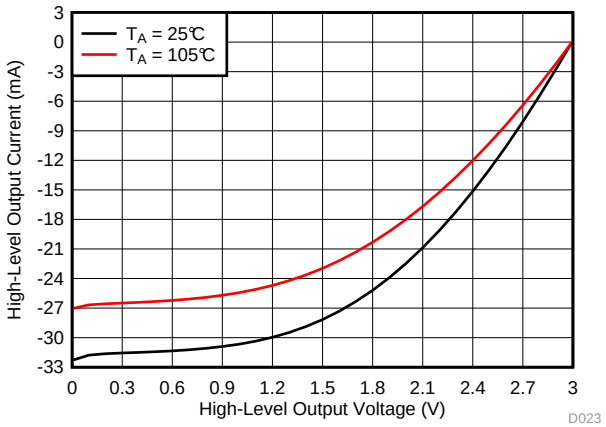
V_{CC} = 3.0 V P7.0

图 5-20. Low-Level Output Voltage vs Low-Level Output Current



V_{CC} = 2.2 V P7.0

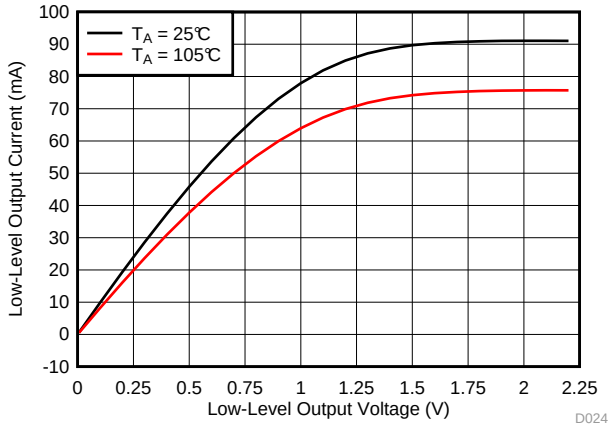
图 5-21. High-Level Output Voltage vs High-Level Output Current



V_{CC} = 3.0 V P7.0

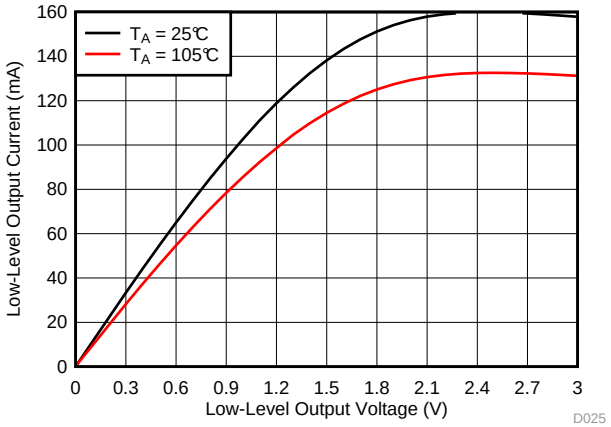
图 5-22. High-Level Output Voltage vs High-Level Output Current

5.26.6.2 Typical Characteristics, High-Drive I/O Outputs at 3.0 V and 2.2 V



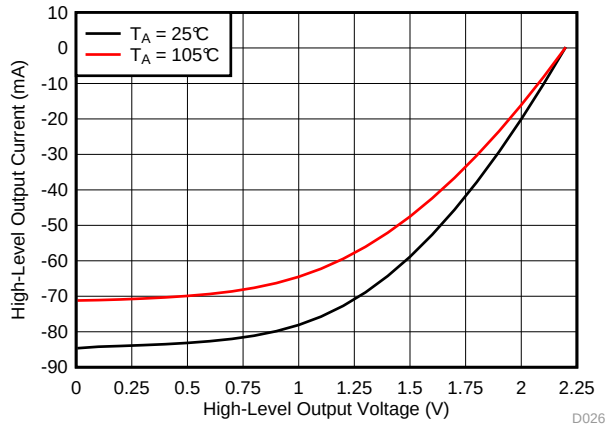
V_{CC} = 2.2 V P2.1

图 5-23. Low-Level Output Voltage vs Low-Level Output Current



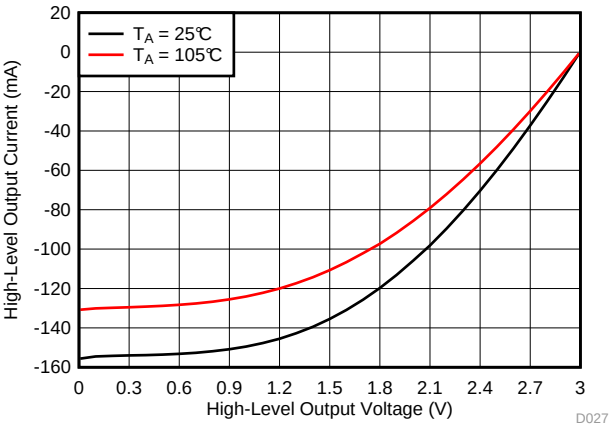
V_{CC} = 3.0 V P2.1

图 5-24. Low-Level Output Voltage vs Low-Level Output Current



V_{CC} = 2.2 V P2.1

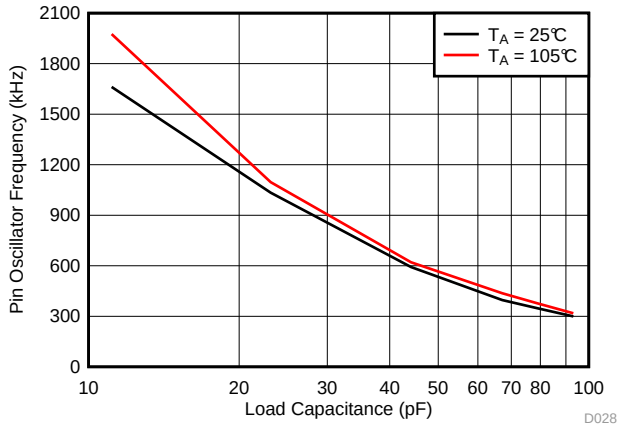
图 5-25. High-Level Output Voltage vs High-Level Output Current



V_{CC} = 3.0 V P2.1

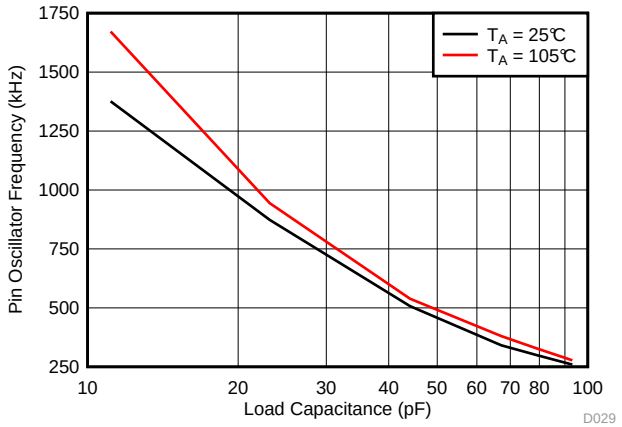
图 5-26. High-Level Output Voltage vs High-Level Output Current

5.26.6.3 Typical Characteristics, Pin-Oscillator Frequency



One output active at a time V_{CC} = 3.0 V

图 5-27. Load Capacitance vs Pin Oscillator Frequency



One output active at a time V_{CC} = 2.2 V

图 5-28. Load Capacitance vs Pin Oscillator Frequency

5.26.7 Precision ADC

Table 5-27 lists the power supply and input range conditions for the ADC.

Table 5-27. 14-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V, ADC14PWRMD = 2		1.62		3.7	V
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V, ADC14PWRMD = 0		1.8		3.7	V
V(Ax)	Analog input voltage range(1)	All ADC analog input pins Ax		0		AVCC	V
V_{CM}	Input common-mode range	All ADC analog input pins Ax (ADC14DIF = 1)		0	VREF / 2	VREF	V
$I_{(ADC14)}$ single-ended mode	Operating supply current into AVCC plus DVCC terminal(2)	$f_{ADC14CLK}$ = 12.5 MHz, 500 ksps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		320	450	µA
			2.2 V		305	430	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		215	310	
			2.2 V		210	300	
$I_{(ADC14)}$ differential mode	Operating supply current into AVCC plus DVCC terminal(2)	$f_{ADC14CLK}$ = 12.5 MHz, 500 ksps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		435	650	µA
			2.2 V		400	630	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		275	390	
			2.2 V		260	370	
C_I	Input capacitance into a single terminal(3)				12	15	pF
R_I	Input MUX ON-resistance	0 V ≤ $V_{(Ax)}$ ≤ AVCC	1.8 V to 3.7 V		0.135	1	kΩ
			1.62 V to <1.8 V		0.15	1.5	

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(2) The internal reference supply current is not included in current consumption parameter $I_{(ADC14)}$.
(3) Represents only the ADC switching capacitance. See the digital inputs electrical specification for internal parasitic pin capacitance.

Table 5-28 lists the timing parameters of the ADC.

Table 5-28. 14-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC14CLK}$	ADC clock frequency(1)	ADC14PWRMD = 0	1.8 V to 3.7 V	0.128		12.5	MHz
		ADC14PWRMD = 2	1.62 V to 3.7 V	0.128		5.75	
$N_{CONVERT}$	Clock cycles for conversion	ADC14RES = 11			16		cycles
		ADC14RES = 10			14		
		ADC14RES = 01			11		
		ADC14RES = 00			9		
$t_{ADC14ON}$	Turnon settling time of ADC	See (2)				1.5	µs
t_{Sample}	Sampling time(3) (4)	R_S = 200 Ω, C_{pext} = 10 pF, R_I = 1 kΩ, C_I = 15 pF, C_{pint} = 5 pF		0.215			µs

(1) MODOSC can be used for 500 ksps and SYSOSC can be used for 200 ksps sampling rate operations of ADC. MODOSC clock should be divided by 2 when it is used for 500 ksps operation of ADC.
(2) The condition is that the error in a conversion started after $t_{ADC14ON}$ is less than ±1 LSB. The reference and input signal are already settled.
(3) Sampling time should be at least 4 × (1 / $f_{ADC14CLK}$).
(4) $t_{sample} \geq (n + 1) \times \ln(2) \times [(R_S + R_I) \times C_I + R_S \times (C_{pext} + C_{pint})]$, where n = ADC resolution =14, R_S = external source resistance, C_{pext} = external parasitic capacitance.

Table 5-29 lists the linearity parameters of the ADC.

Table 5-29. 14-Bit ADC, Linearity Parameters(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		bits
E_I	Integral linearity error (INL)				±2.3	LSB
E_D	Differential linearity error (DNL)		–0.99		1	LSB
E_O	Offset error	ADC14VRSEL = 0xE, 0xF		±0.2	±1	mV
		ADC14VRSEL = 0x1		±1.2	±2	
E_G	Gain error	ADC14VRSEL = 0xE		±2	±4	LSB
		ADC14VRSEL = 0xF		±20	±60	
		ADC14VRSEL = 0x1		±50	±180	
E_T	Total unadjusted error	ADC14VRSEL = 0xE		±4	±15	LSB
		ADC14VRSEL = 0xF		±22	±62	
		ADC14VRSEL = 0x1		±55	±185	

(1) Minimum reference voltage of 1.45 V is necessary to meet the specified accuracy. Lower reference voltage down to 1.2 V can be applied for 500 ksps sampling rate with reduced accuracy requirements.
(2) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 0xE.

Table 5-30 lists the dynamic parameters of the ADC.

Table 5-30. 14-Bit ADC, Dynamic Parameters(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD(2)	Signal-to-noise and distortion	500 ksps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO-based operation	71	73		dB
		500 ksps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC/DC-based operation	62	70		
		500 ksps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine	79	81		
ENOB(2)	Effective number of bits	500 ksps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO-based operation	11.5	11.8		bit
		500 ksps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC/DC-based operation	10	11.3		
		500 ksps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine	12.8	13.2		
CMRR_DC	Common-mode rejection ratio, DC	Common-mode input signal = 0 to VREF pp at DC, ADC14DIF = 1	70	85		dB
CMRR_AC	Common-mode rejection ratio, AC	Common-mode input signal = 0 to VREF pp at 1 MHz, ADC14DIF = 1	55	65		dB
PSRR_DC	Power supply rejection ratio, DC	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 0, ADC14VRSEL = 0xE		1	2.5	mV/V
		AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 1, ADC14VRSEL = 0xE		50	190	µV/V
PSRR_AC	Power supply rejection ratio, AC	dAV_{CC} = 0.1 V at 1 kHz, ADC14DIF = 0, ADC14VRSEL = 0xE		1		mV/V
		dAV_{CC} = 0.1 V at 1 kHz, ADC14DIF = 1, ADC14VRSEL = 0xE		50		µV/V

(1) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 0xE.
(2) ADC clock derived from HFXT oscillator.

Table 5-31 lists the characteristics of the temperature sensor and built-in $V_{1/2}$.

Table 5-31. 14-Bit ADC, Temperature Sensor and Built-In $V_{1/2}$

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	Temperature sensor voltage(1) (2) (see Figure 5-29)	ADC14ON = 1, ADC14TCMAP = 1, T_A = 0°C			685		mV
TC_{SENSOR}	Change in voltage per °C(2)	ADC14ON = 1, ADC14TCMAP = 1			1.9		mV/°C
t_{SENSOR} (sample)	Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected(3)	ADC14ON = 1, ADC14TCMAP = 1, Error of conversion result ≤ 1 LSB		5			µs
$V_{1/2}$	AVCC voltage divider for ADC14BATMAP = 1 on MAX input channel	ADC14ON = 1, ADC14BATMAP = 1		48%	50%	52%	
$t_{V\ 1/2}$ (sample)	Sample time required if ADC14BATMAP = 1 and channel MAX is selected(4)	ADC14ON = 1, ADC14BMAP = 1		1			µs

(1) The temperature sensor offset can be as much as ±35°C. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(2) The TLV structure contains calibration values for 30°C ±3°C and 105°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (Temperature,°C) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
(3) The typical equivalent impedance of the sensor is 250 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{V1/2(on)}$ is included in the sampling time $t_{V\ 1/2\ (sample)}$. No additional on time is needed.

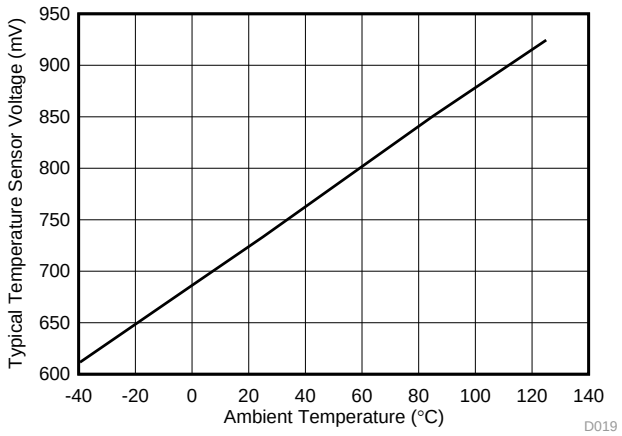


Figure 5-29. Typical Temperature Sensor Voltage

Table 5-32 lists the characteristics of the internal reference buffers of the ADC.

Table 5-32. 14-Bit ADC, Internal Reference Buffers

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REF+}	Operating supply current into AVCC terminal(1)	ADC ON, REFOUT = 0, ADC14PWRMD = 0, REFVSEL = {0, 1, 3}	3 V		600	850	µA
		ADC ON, REFOUT = 0, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}			200	325	
		ADC ON, REFOUT = 1, ADC14PWRMD = 2, REFVSEL = {0, 1, 3}			650	925	
t_{on}	Turnon time		3 V			5	µs

(1) The internal reference current is supplied through terminal AVCC.

Table 5-33 lists the characteristics of the ADC external reference.

Table 5-33. 14-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input(1)		1.45		AV_{CC}	V
V_{eREF-}	Negative external reference voltage input				0	V
(V_{eREF+} - V_{eREF-})	Differential external reference voltage input(1)		1.45		AV_{CC}	V
I_{VeREF+} I_{VeREF-}	Static input current in single ended input mode	1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 12.5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0			±75	µA
		1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0			±15	
I_{VeREF+} I_{VeREF-}	Static input current in differential input mode	1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC14CLK}$ = 12.5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1			±150	µA
		1.45 V ≤ V_{eREF+}≤ V_{AVCC}, V_{eREF-} = 0 V $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1			±30	
C_{VeREF+}	Capacitance at VeREF+ terminal	See (2)	5			µF

(1) Lower reference voltage down to 1.2 V can be applied for 500-ksps sampling rate with reduced accuracy requirements of linearity parameters.
(2) Connect two decoupling capacitors, 5 µF and 50 nF, to the VeREF+ terminal to decouple the dynamic current required for an external reference source, if it is used for the ADC14.

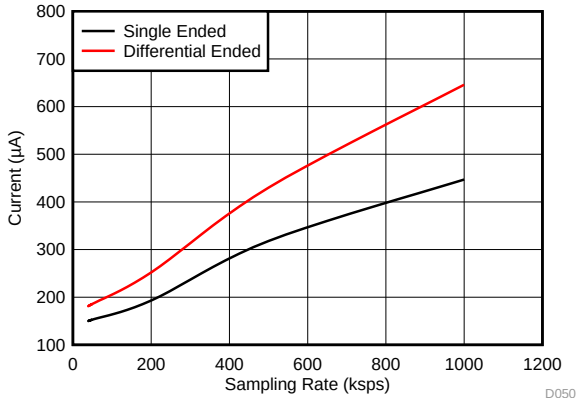
5.26.7.1 Typical Characteristics of ADC

typical characteristics at 3 V, 25°C, and 1-Msps sampling rate of ADC (unless otherwise specified)

表 5-34 lists the ADC typical characteristics graphs.

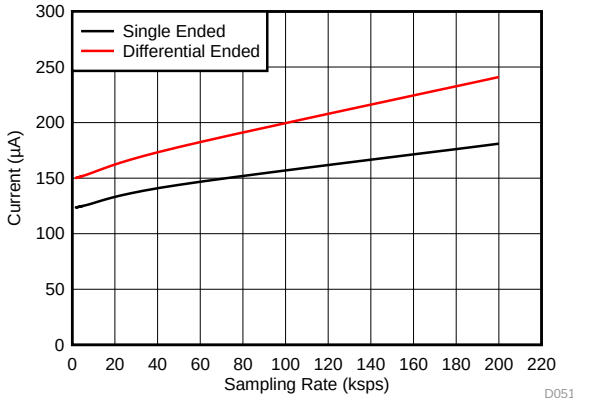
表 5-34. ADC Typical Characteristics Graphs

TITLE	TEST CONDITIONS	FIGURE
Current vs Sampling Rate	VRSEL = 14, VREF = 2.5 V, Resolution = 14 Bit, ADC14PWRMD = 0	图 5-30
	VRSEL = 14, VREF = 2.5 V, Resolution = 12 Bit, ADC14PWRMD = 2	图 5-31
	VRSEL = 1, VREF = 2.5 V, REFOUT = 0, ADC14PWRMD = 0, Resolution = 14 Bit	图 5-32
	VRSEL = 1, VREF = 2.5 V, REFOUT = 0, ADC14PWRMD = 2, Resolution = 12 Bit	图 5-33
	VRSEL = 1, VREF = 2.5 V, REFOUT = 1, ADC14PWRMD = 2, Resolution = 12 Bit	图 5-34
INL vs ADC Output Code	VRSEL = 1, VREF = 2.5 V, Input Mode = Single Ended	图 5-35
	VRSEL = 1, VREF = 2.5 V, Input Mode = Differential	图 5-36
	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-37
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-38
	VRSEL = 15, VREF = 2.5 V, Input Mode = Single Ended	图 5-39
	VRSEL = 15, VREF = 2.5 V, Input Mode = Differential	图 5-40
DNL vs ADC Output Code	VRSEL = 1, VREF = 2.5 V, Input Mode = Single Ended	图 5-41
	VRSEL = 1, VREF = 2.5 V, Input Mode = Differential	图 5-42
	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-43
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-44
	VRSEL = 15, VREF = 2.5 V, Input Mode = Single Ended	图 5-45
	VRSEL = 15, VREF = 2.5 V, Input Mode = Differential	图 5-46
Power vs Input Frequency	f_{in} = 20 kHz, VRSEL = 1, VREF = 2.5 V, SINAD = 69 dB, THD = –86 dB, Input Mode = Single Ended	图 5-47
	f_{in} = 20 kHz, VRSEL = 1, VREF = 2.5 V, SINAD = 74 dB, THD = –91 dB, Input Mode = Differential	图 5-48
	f_{in} = 20 kHz, VRSEL = 14, VREF = 2.5 V, SINAD = 73 dB, THD = –92 dB, Input Mode = Single Ended	图 5-49
	f_{in} = 20 kHz, VRSEL = 14, VREF = 2.5 V, SINAD = 82 dB, THD = –100 dB, Input Mode = Differential	图 5-50
	f_{in} = 20 kHz, VRSEL = 15, VREF = 2.5 V, SINAD = 72 dB, THD = –90 dB, Input Mode = Single Ended	图 5-51
	f_{in} = 20 kHz, VRSEL = 15, VREF = 2.5 V, SINAD = 80 dB, THD = –100 dB, Input Mode = Differential	图 5-52
SINAD vs Reference Voltage	f_{in} = 20 kHz, VRSEL = 14	图 5-53
ENOB vs Reference Voltage	f_{in} = 20 kHz, VRSEL = 14	图 5-54
THD vs Reference Voltage	f_{in} = 20 kHz, VRSEL = 14	图 5-55
SFDR vs Reference Voltage	f_{in} = 20 kHz, VRSEL = 14	图 5-56
SINAD vs Temperature	f_{in} = 20 kHz, VRSEL = 14	图 5-57
ENOB vs Temperature	f_{in} = 20 kHz, VRSEL = 14	图 5-58
THD vs Temperature	f_{in} = 20 kHz, VRSEL = 14	图 5-59
SFDR vs Temperature	f_{in} = 20 kHz, VRSEL = 14	图 5-60
INL vs Temperature	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-61
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-62
DNL vs Temperature	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-63
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-64
Offset Voltage vs Temperature	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-65
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-66
Gain Error vs Temperature	VRSEL = 14, VREF = 2.5 V, Input Mode = Single Ended	图 5-67
	VRSEL = 14, VREF = 2.5 V, Input Mode = Differential	图 5-68



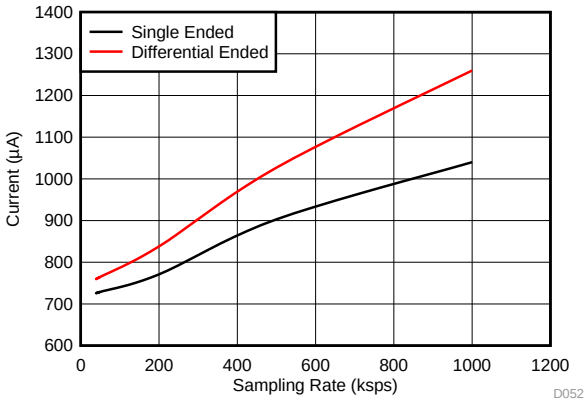
VRSEL = 14 VREF = 2.5 V
Resolution = 14 Bit ADC14PWRMD = 0

图 5-30. Current vs Sampling Rate



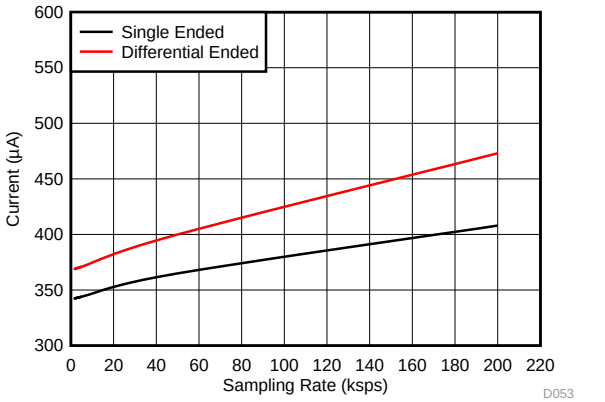
VRSEL = 14 VREF = 2.5 V
Resolution = 12 Bit ADC14PWRMD = 2

图 5-31. Current vs Sampling Rate



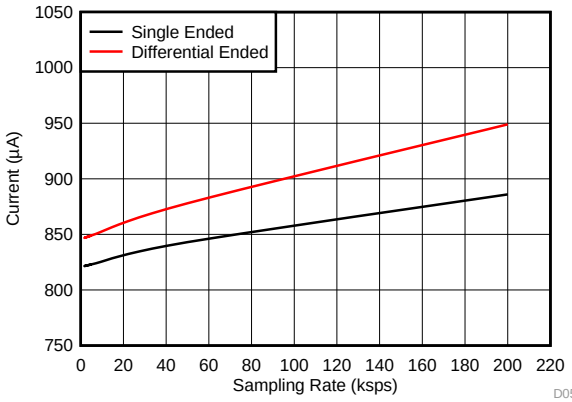
VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 0
Resolution = 14 Bit

图 5-32. Current vs Sampling Rate



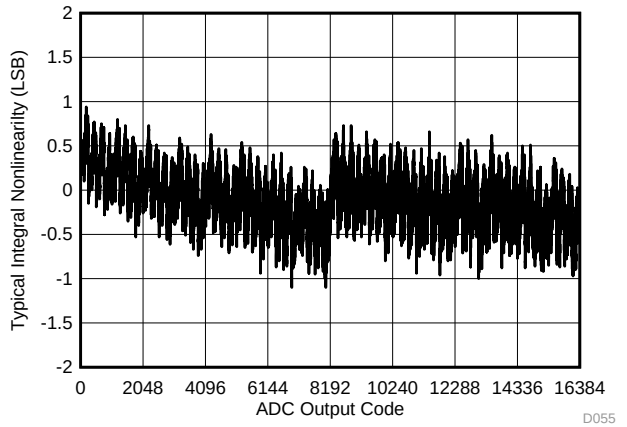
VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 2
Resolution = 12 Bit

图 5-33. Current vs Sampling Rate



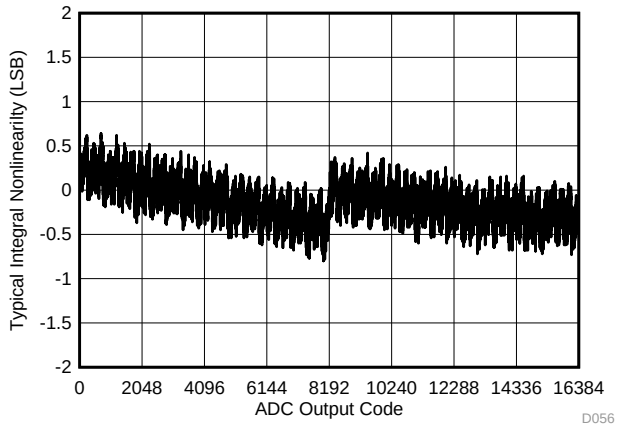
VRSEL = 1 VREF = 2.5 V
REFOUT = 1 ADC14PWRMD = 2
Resolution = 12 Bit

图 5-34. Current vs Sampling Rate



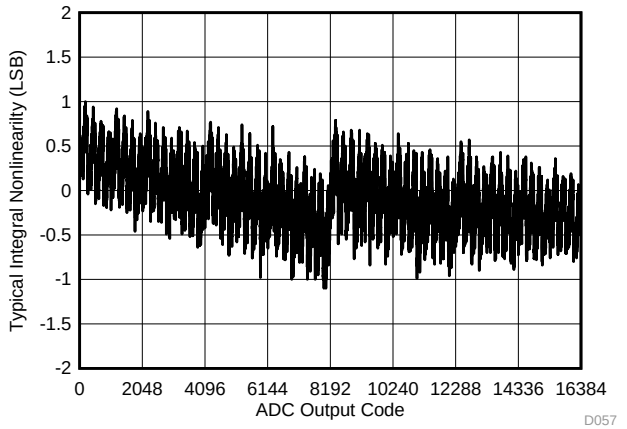
VRSEL = 1 VREF = 2.5 V
Input Mode = Single Ended

图 5-35. INL vs ADC Output Code



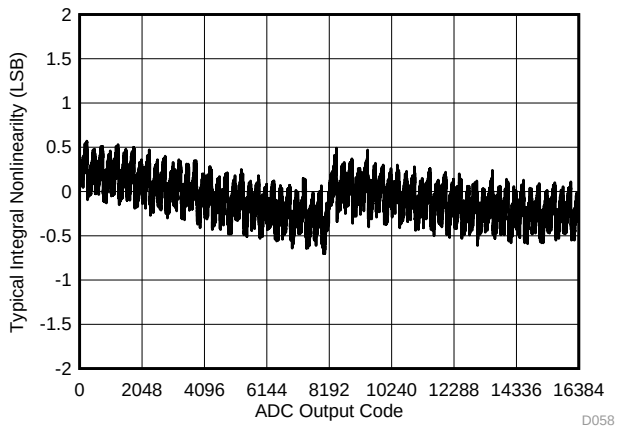
VRSEL = 1 VREF = 2.5 V
Input Mode = Differential

图 5-36. INL vs ADC Output Code



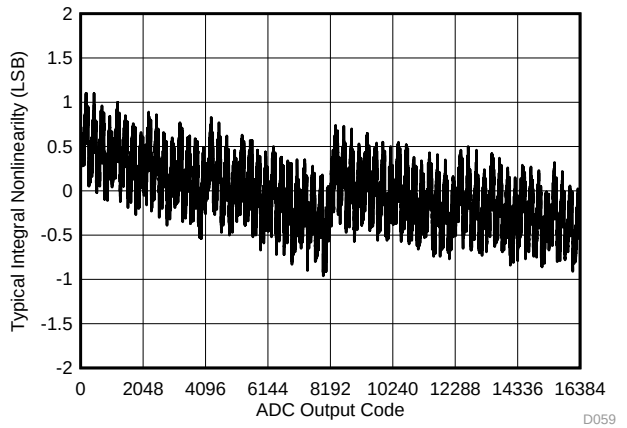
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-37. INL vs ADC Output Code



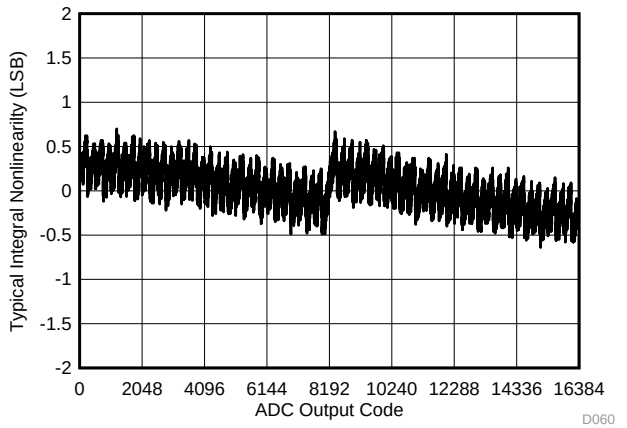
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-38. INL vs ADC Output Code



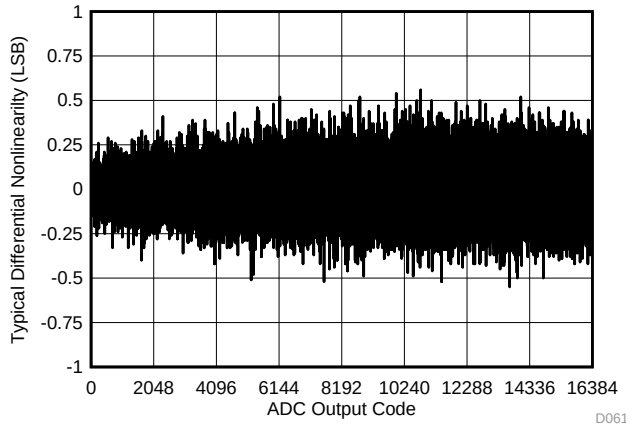
VRSEL = 15 VREF = 2.5 V
Input Mode = Single Ended

图 5-39. INL vs ADC Output Code



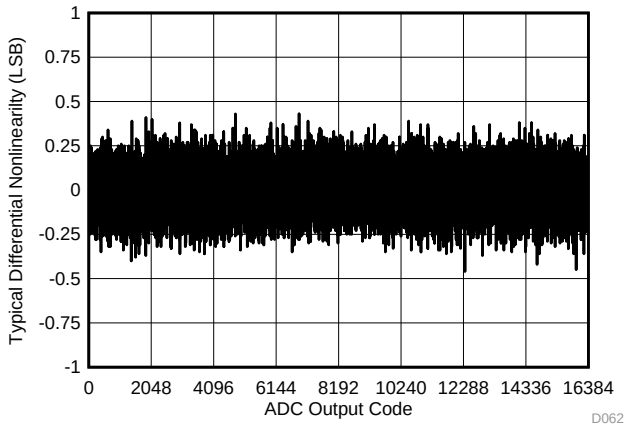
VRSEL = 15 VREF = 2.5 V
Input Mode = Differential

图 5-40. INL vs ADC Output Code



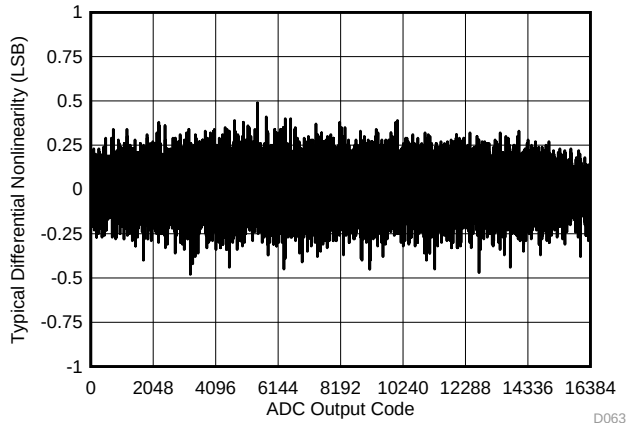
VRSEL = 1 VREF = 2.5 V
Input Mode = Single Ended

图 5-41. DNL vs ADC Output Code



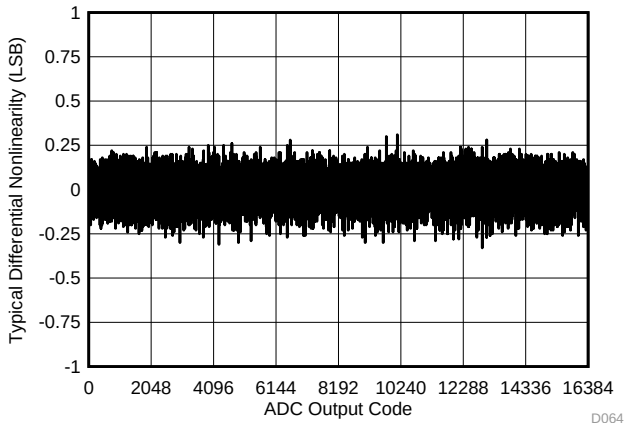
VRSEL = 1 VREF = 2.5 V
Input Mode = Differential

图 5-42. DNL vs ADC Output Code



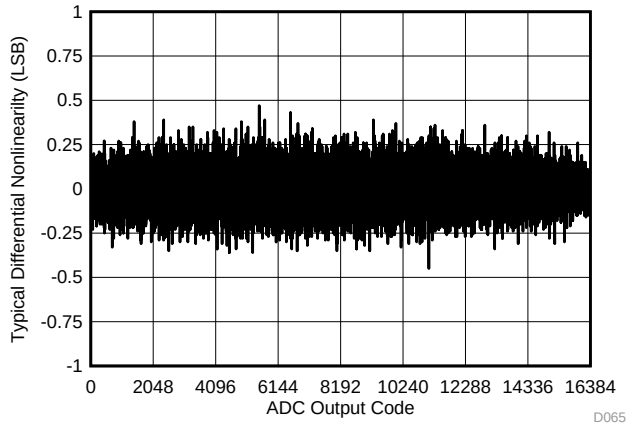
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-43. DNL vs ADC Output Code



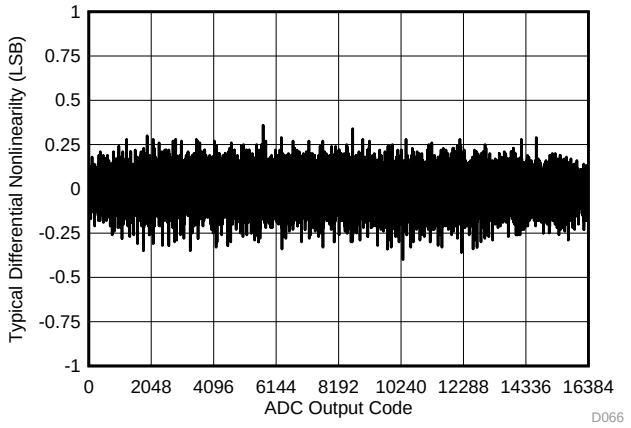
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-44. DNL vs ADC Output Code



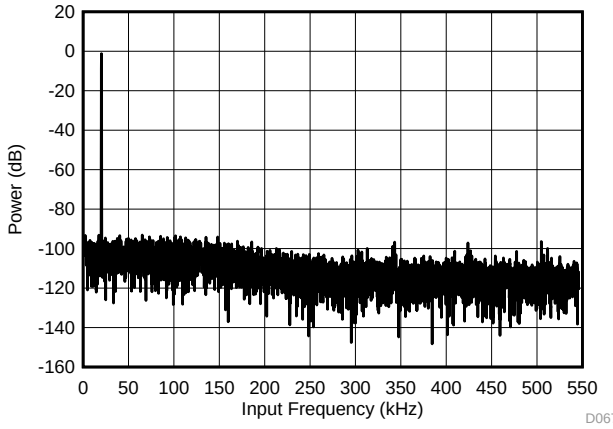
VRSEL = 15 VREF = 2.5 V
Input Mode = Single Ended

图 5-45. DNL vs ADC Output Code



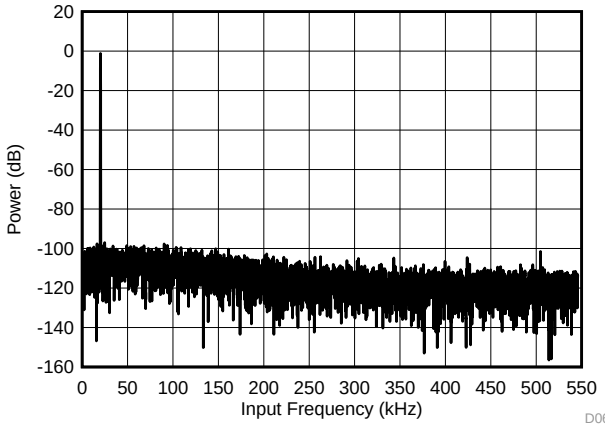
VRSEL = 15 VREF = 2.5 V
Input Mode = Differential

图 5-46. DNL vs ADC Output Code



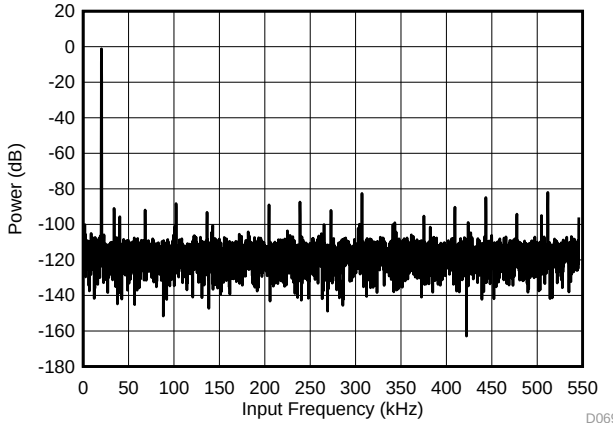
f_{in} = 20 kHz VRSEL = 1
VREF = 2.5 V SINAD = 69 dB
THD = –86 dB Input Mode = Single Ended

图 5-47. Power vs Input Frequency



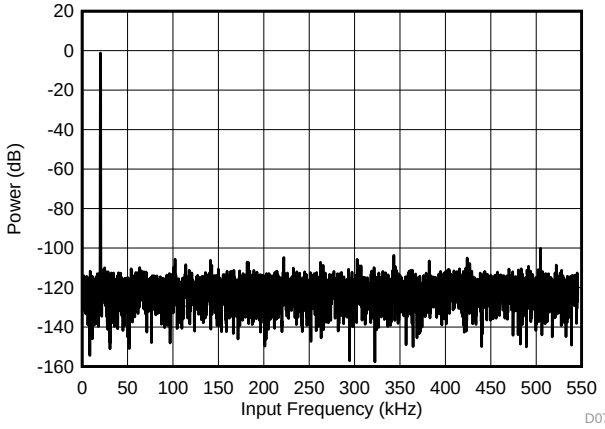
f_{in} = 20 kHz VRSEL = 1
VREF = 2.5 V SINAD = 74 dB
THD = –91 dB Input Mode = Differential

图 5-48. Power vs Input Frequency



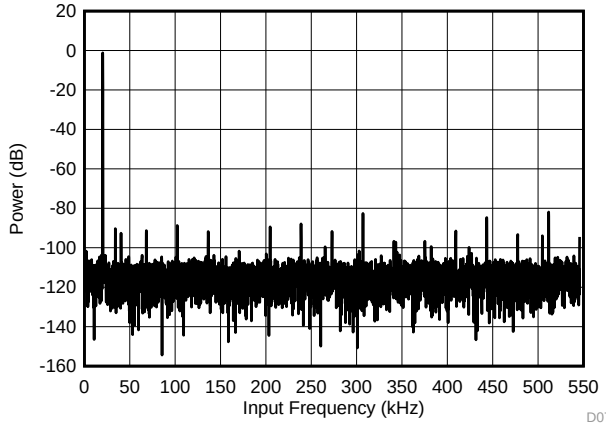
f_{in} = 20 kHz VRSEL = 14
VREF = 2.5 V SINAD = 73 dB
THD = –92 dB Input Mode = Single Ended

图 5-49. Power vs Input Frequency



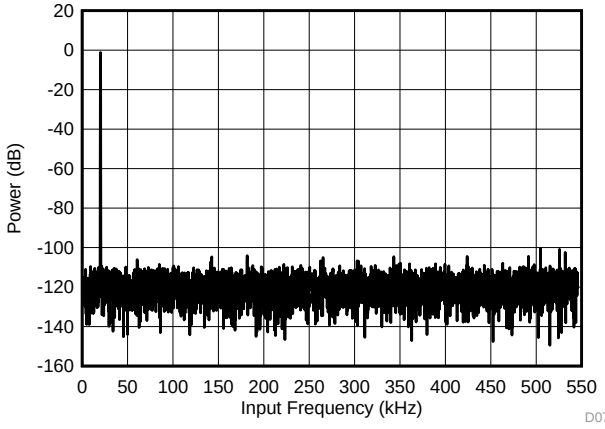
f_{in} = 20 kHz VRSEL = 14
VREF = 2.5 V SINAD = 82 dB
THD = –100 dB Input Mode = Differential

图 5-50. Power vs Input Frequency



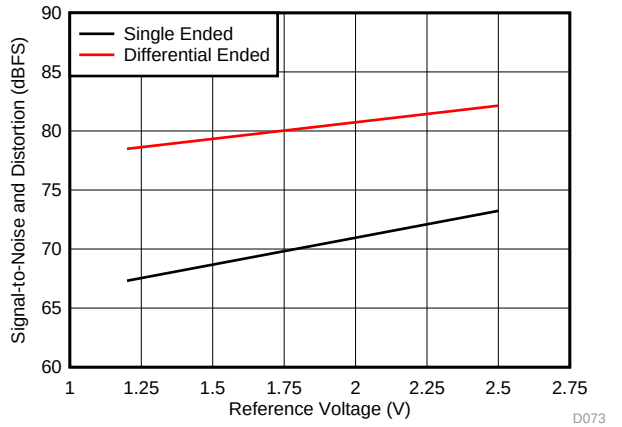
f_{in} = 20 kHz VRSEL = 15
VREF = 2.5 V SINAD = 72 dB
THD = –90 dB Input Mode = Single Ended

图 5-51. Power vs Input Frequency



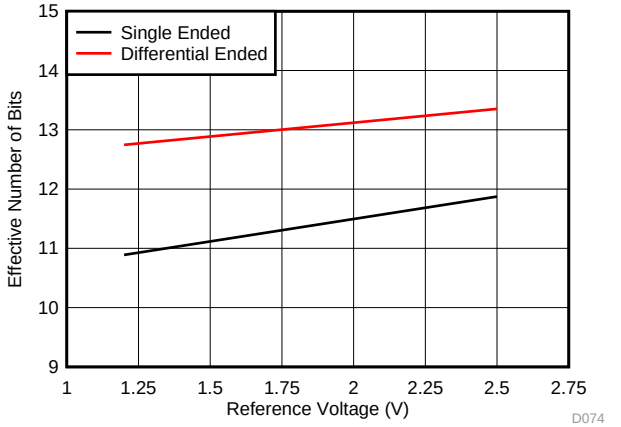
f_{in} = 20 kHz VRSEL = 15
VREF = 2.5 V SINAD = 80 dB
THD = –100 dB Input Mode = Differential

图 5-52. Power vs Input Frequency



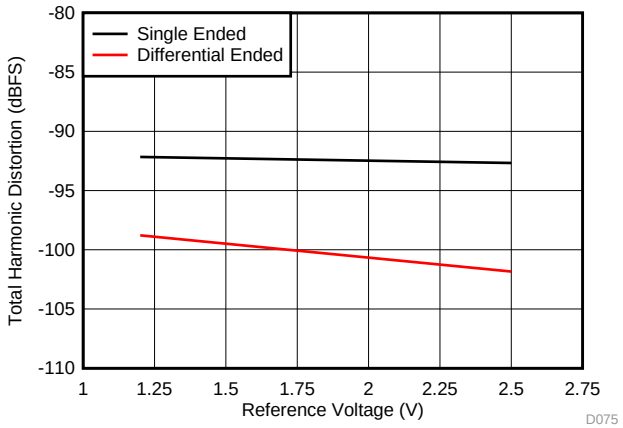
f_{in} = 20 kHz VRSEL = 14

图 5-53. SINAD vs Reference Voltage



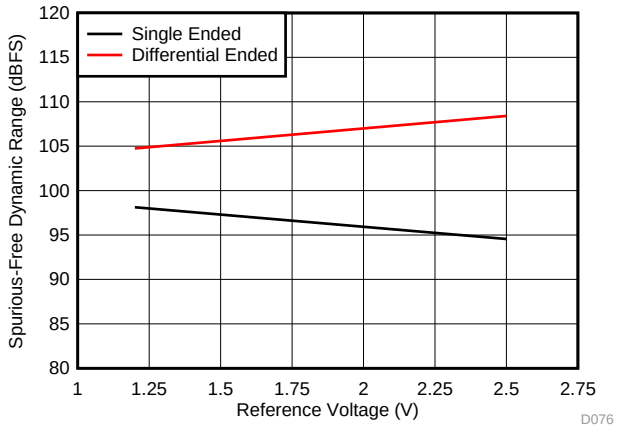
f_{in} = 20 kHz VRSEL = 14

图 5-54. ENOB vs Reference Voltage



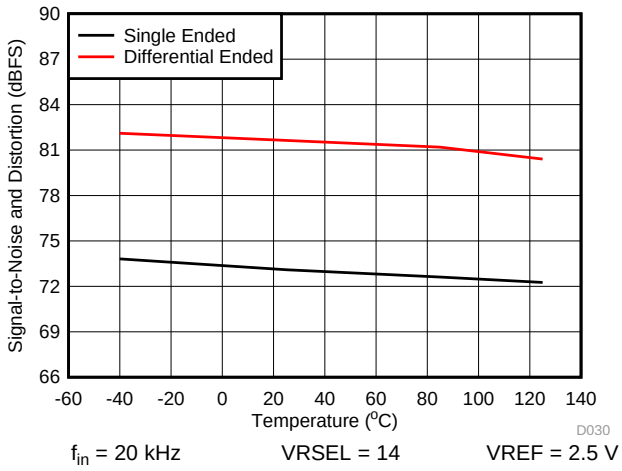
f_{in} = 20 kHz VRSEL = 14

图 5-55. THD vs Reference Voltage



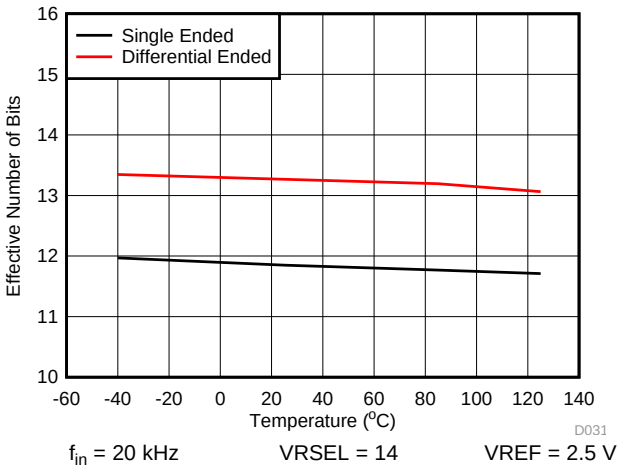
f_{in} = 20 kHz VRSEL = 14

图 5-56. SFDR vs Reference Voltage



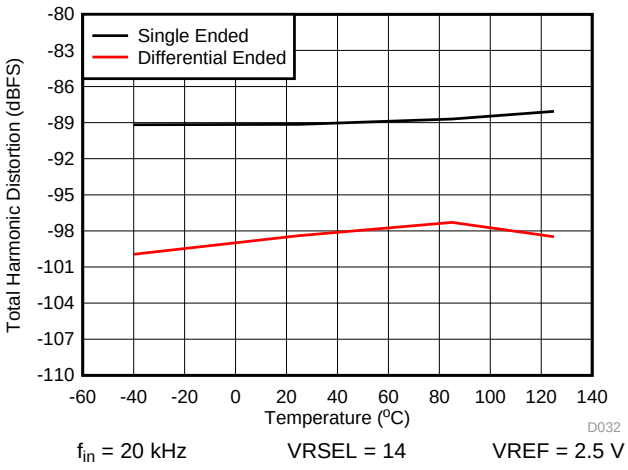
f_{in} = 20 kHz VRSEL = 14 VREF = 2.5 V

图 5-57. SINAD vs Temperature



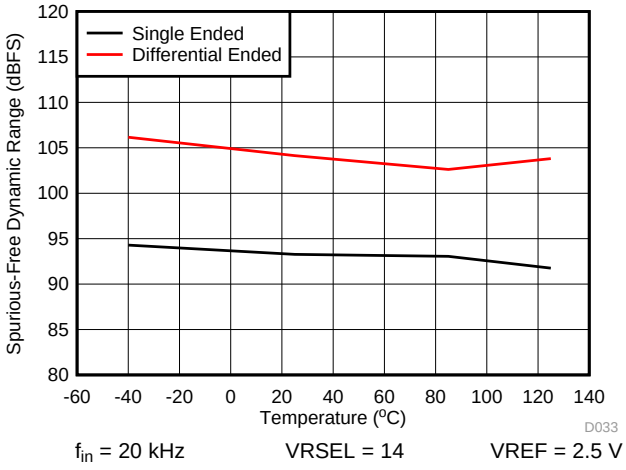
f_{in} = 20 kHz VRSEL = 14 VREF = 2.5 V

图 5-58. ENOB vs Temperature



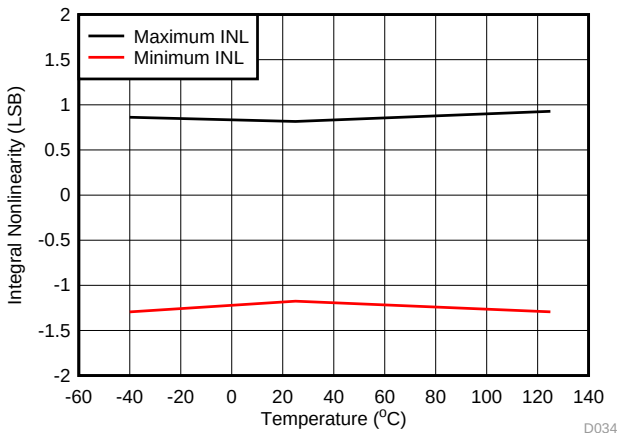
f_{in} = 20 kHz VRSEL = 14 VREF = 2.5 V

图 5-59. THD vs Temperature



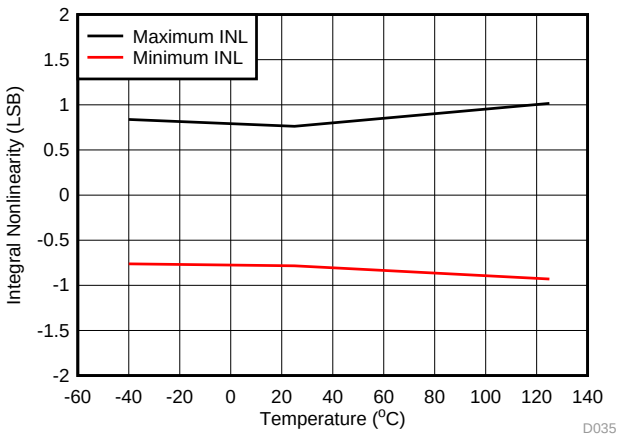
f_{in} = 20 kHz VRSEL = 14 VREF = 2.5 V

图 5-60. SFDR vs Temperature



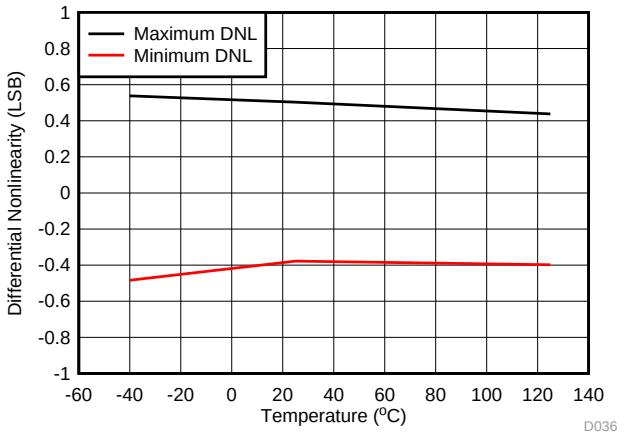
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-61. INL vs Temperature



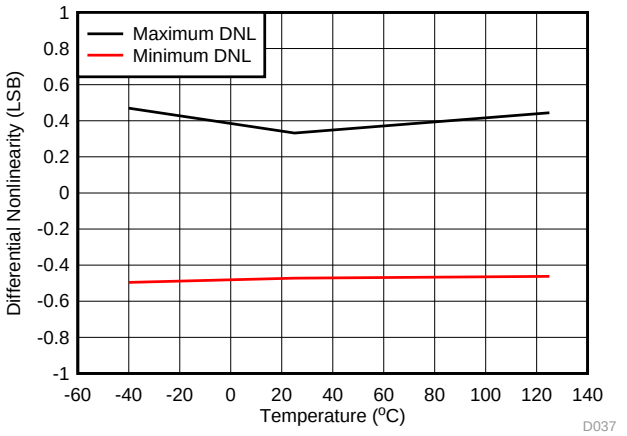
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-62. INL vs Temperature



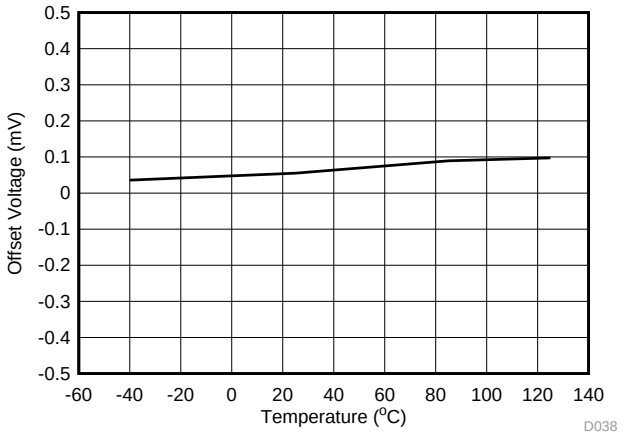
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-63. DNL vs Temperature



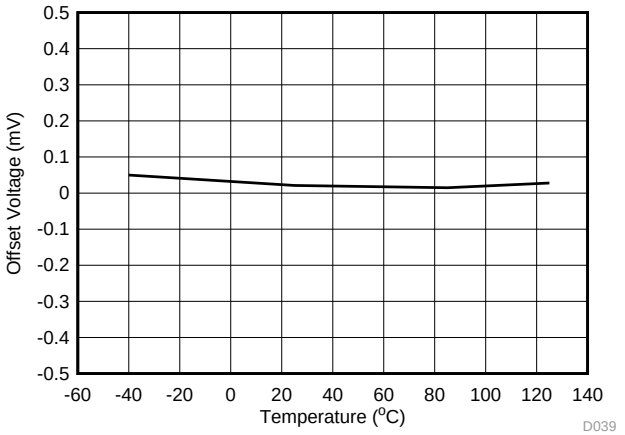
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-64. DNL vs Temperature



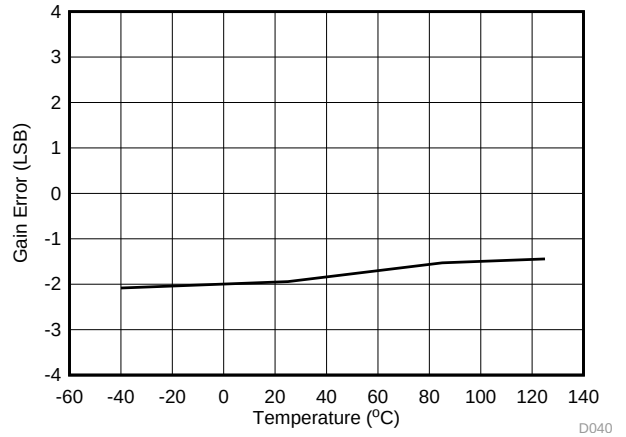
VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-65. Offset Voltage vs Temperature



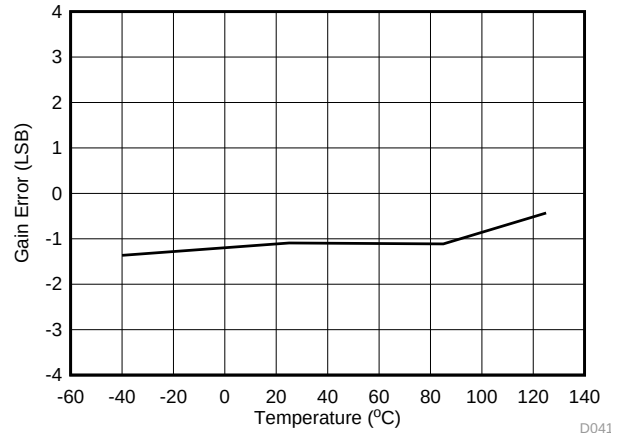
VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-66. Offset Voltage vs Temperature



VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

图 5-67. Gain Error vs Temperature



VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

图 5-68. Gain Error vs Temperature

5.26.8 REF_A

Table 5-35 lists the characteristics of the REF_A built-in reference.

Table 5-35. REF_A, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {0} for 1.2 V, REFON = 1	1.62 V		1.2	±1%	V
		REFVSEL = {1} for 1.45 V, REFON = 1	1.75 V		1.45	±1%	
		REFVSEL = {3} for 2.5 V, REFON = 1	2.8 V		2.5	±1%	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.2 V		1.62			V
		REFVSEL = {1} for 1.45 V		1.75			
		REFVSEL = {3} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal(1)	REFON = 1	3 V		15	20	µA
$I_{O(VREF+)}$	VREF maximum load current, VREF+ terminal	REFVSEL = {0, 1, 3}, AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1		–1000		+10	µA
$I_{L(VREF+)}$	Load-current regulation, VREF+ terminal	REFVSEL = {0, 1, 3}, I(VREF+) = +10 µA or –1000 µA, AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1				2500	µV/mA
$C_{VREF±}$	Capacitance at VREF+, VREF- terminals	REFON = REFOUT = 1		0		100	pF
$PSRR\_DC_{REFOUT0}$	Power supply rejection ratio (DC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 0			50	350	µV/V
$PSRR\_DC_{REFOUT1}$	Power supply rejection ratio (DC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 1			50	250	µV/V
$PSRR\_AC_{REFOUT0}$	Power supply rejection ratio (AC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, dAVCC = 0.1 V at 1 kHz, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 0			2	10	mV/V
$PSRR\_AC_{REFOUT1}$	Power supply rejection ratio (AC) after ADC buffer	AV_{CC} = $AV_{CC\ (min)}$ for each reference level, dAVCC = 0.1 V at 1 kHz, REFVSEL = {0, 1, 3}, REFON = 1, REFOUT = 1			2	5	mV/V
TC_{REF+} (2)	Temperature coefficient of built-in reference	REFVSEL = {0, 1, 3}, REFON = 1, T_A = –40°C to 105°C			25	60	ppm/°C
t_{SETTLE}	Settling time of reference voltage(3)	AV_{CC} = $AV_{CC\ (min)}$ to $AV_{CC(max)}$ REFVSEL = {0, 1, 3}, REFON = 0 → 1			70	80	µs

(1) The internal reference current is supplied from terminal AVCC.
(2) Calculated using the box method: (MAX(–40°C to 125°C) – MIN(–40°C to 125°C)) / MIN(–40°C to 125°C)/(125°C – (–40°C)).
(3) The condition is that the error in a ADC conversion started after t_{SETTLE} is less than ±0.5 LSB.

5.26.9 Comparator_E

Table 5-36 lists the characteristics of the comparator.

Table 5-36. Comparator_E Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.62		3.7	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, excludes reference resistor ladder	CEPWRMD = 00, CEON = 1, CERSx = 00 (fast)	2.2 V, 3 V		10	15	µA
		CEPWRMD = 01, CEON = 1, CERSx = 00 (medium)	2.2 V, 3 V		8	10	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 30°C	2.2 V, 3 V			0.5	
		CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), T_A = 105°C	2.2 V, 3 V			0.5	
I_{AVCC_REF}	Quiescent current of resistor ladder into AVCC, includes REF_A module current	CEREFACC = 0, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0	2.2 V, 3 V		25	35	µA
		CEREFACC = 1, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0	2.2 V, 3 V		10	15	
V_{REF}	Reference voltage level	CERSx = 11, CEREFLx = 01, CEREFACC = 0	1.62 V	1.17	1.2	1.23	V
		CERSx = 11, CEREFLx = 10, CEREFACC = 0	2.2 V	1.95	2.0	2.05	
		CERSx = 11, CEREFLx = 11, CEREFACC = 0	2.7 V	2.40	2.5	2.60	
		CERSx = 11, CEREFLx = 01, CEREFACC = 1	1.62 V	1.15	1.2	1.23	
		CERSx = 11, CEREFLx = 10, CEREFACC = 1	2.2 V	1.92	2.0	2.05	
		CERSx = 11, CEREFLx = 11, CEREFACC = 1	2.7 V	2.4	2.5	2.6	
V_{IC}	Common-mode input range			0		VCC–1	V
V_{OFFSET}	Input offset voltage	CEPWRMD = 00		–10		+10	mV
		CEPWRMD = 01		–20		+20	
		CEPWRMD = 10		–20		+20	
C_{IN}	Input capacitance	CEPWRMD = 00 or CEPWRMD = 01			8		pF
		CEPWRMD = 10			8		
R_{SIN}	Series input resistance	On (switch closed)			2	4	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV			330	550	ns
		CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV			410	650	
		CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV				30	µs
$t_{PD,filter}$	Propagation delay with filter active	CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00			0.6	0.9	µs
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01			1.1	1.6	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10			2	3	
		CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11			4	6	

Table 5-36. Comparator_E Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{EN_CMP}	Comparator enable time	CEON = 0 to 1, CEPWRMD = 00, VIN+, VIN- from pins, Overdrive ≥ 20 mV			0.8	1	µs
		CEON = 0 to 1, CEPWRMD = 01, VIN+, VIN- from pins, Overdrive ≥ 20 mV			0.9	1.2	
		CEON = 0 to 1, CEPWRMD = 10, VIN+, VIN- from pins, Overdrive ≥ 20 mV			15	25	
$t_{EN\_CMP\_VREF}$	Comparator and reference ladder and reference voltage enable time	CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	µs
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV			90	120	
		CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			90	180	
$t_{EN\_CMP\_RL}$	Comparator and reference ladder enable time	CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			1.5	2	µs
		CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			1.5	2	
		CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV			15	25	
V_{CMP_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n + 0.9) / 32	VIN × (n + 1) / 32	VIN × (n + 1.1) / 32	V

5.26.10 LCD_F

Table 5-37. LCD Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD}$	Supply voltage range, internal or external biasing		2.4		3.7	V
$f_{ACLK,in}$	ACLK input frequency range		10	32.768	128	kHz
f_{LCD}	LCD frequency range	f_{FRAME} = 1 / (2 × mux) × f_{LCD} with mux = 1 (Static) to 8			1024	Hz
$f_{FRAME,4mux}$	LCD frame frequency range	$f_{FRAME,4mux}$ (MAX) = 1 / (2 × 4) × f_{LCD} (MAX) = 1 / (2 × 4) × 1024 Hz			128	Hz
$f_{FRAME,8mux}$	LCD frame frequency range	$f_{FRAME,8mux}$ (MAX) = 1/(2 × 8) × f_{LCD} (MAX) = 1 / (2 × 8) × 1024 Hz			64	Hz
C_{Panel}	Panel capacitance	f_{LCD} = 1024 Hz, all common lines equally loaded			10000	pF
$V_{R23,1/3bias}$	Analog input voltage at R23 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	V_{R03} + 2/3 × (V_{CC} – V_{R03})	V_{CC}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	V_{R03} + 1/3 × (V_{CC} – V_{R03})	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing, 1- to 4-mux modes	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1, LCDMXx(2) = 0	V_{R03}	V_{R03} + 1/2 × (V_{CC} – V_{R03})	V_{CC}	V
$V_{R23,1/4bias}$	Analog input voltage at R23 with 1/4 biasing, 4- to 8-mux modes	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1, LCDMXx(2) = 1	V_{R13}	3/4 × V_{CC}	V_{CC}	V
$V_{R13,1/4bias}$	Analog input voltage at R13 with 1/4 biasing, 4- to 8-mux modes	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1, LCDMXx(2) = 1	V_{R03}	1/2 × V_{CC}	V_{R23}	V
$V_{R03,1/4bias}$	Analog input voltage at R03 with 1/4 biasing, 4- to 8-mux modes	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1, LCDMXx(2) = 1	V_{SS}	1/4 × V_{CC}	V_{R13}	V
$V_{R03,EXT}$	Analog input voltage at R03 in 1/2 and 1/3-bias modes	R0EXT = 1	V_{SS}		V_{CC}	V

Table 5-38. LCD Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	I_{LOAD} = ±10 µA	2.4 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	I_{LOAD} = ±10 µA	2.4 V			10	kΩ

5.26.11 eUSCI

Table 5-39 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-39. eUSCI Clock Frequency (UART Mode)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, External: UCLK, Duty cycle = 50% ±10%	1.2 V			12	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)		1.2 V			5	MHz

Table 5-40 lists the characteristics of the eUSCI in UART mode.

Table 5-40. eUSCI Switching Characteristics (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time(1)	UCGLITx = 0		5		20	ns
		UCGLITx = 1		20		60	
		UCGLITx = 2		30		100	
		UCGLITx = 3		50		150	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. Thus the selected deglitch time can limit the maximum useable baud rate. To ensure that pulses are correctly recognized, their duration must exceed the maximum specification of the deglitch time.

Table 5-41 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-41. eUSCI Clock Frequency (SPI Master Mode)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	SMCLK, Duty cycle = 50% ±10%	V_{CORE} = 1.2 V				12	MHz

Table 5-42 lists the characteristics of the eUSCI in SPI master mode.

Table 5-42. eUSCI Switching Characteristics (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10	1.2 V		1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10	1.2 V		1		UCxCLK cycles
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	1.2 V	1.62 V		30	ns
				3.7 V		20	ns
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	1.2 V	1.62 V		20	ns
				3.7 V		15	ns
$t_{SU,MI}$	SOMI input data setup time		1.2 V	1.62 V	45		ns
				3.7 V	35		ns
$t_{HD,MI}$	SOMI input data hold time		1.2 V	1.62 V	0		ns
				3.7 V	0		ns
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	1.2 V	1.62 V		14	ns
				3.7 V		7	ns
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	1.2 V	1.62 V	0		ns
				3.7 V	0		ns

(1) f_{UCxCLK} = 1/2 $t_{LO/HI}$ with $t_{LO/HI}$ = max($t_{VALID,MO(eUSCI)}$ + $t_{SU,SI(Slave)}$, $t_{SU,MI(eUSCI)}$ + $t_{VALID,SO(Slave)}$)
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-69 and Figure 5-70.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-69 and Figure 5-70.

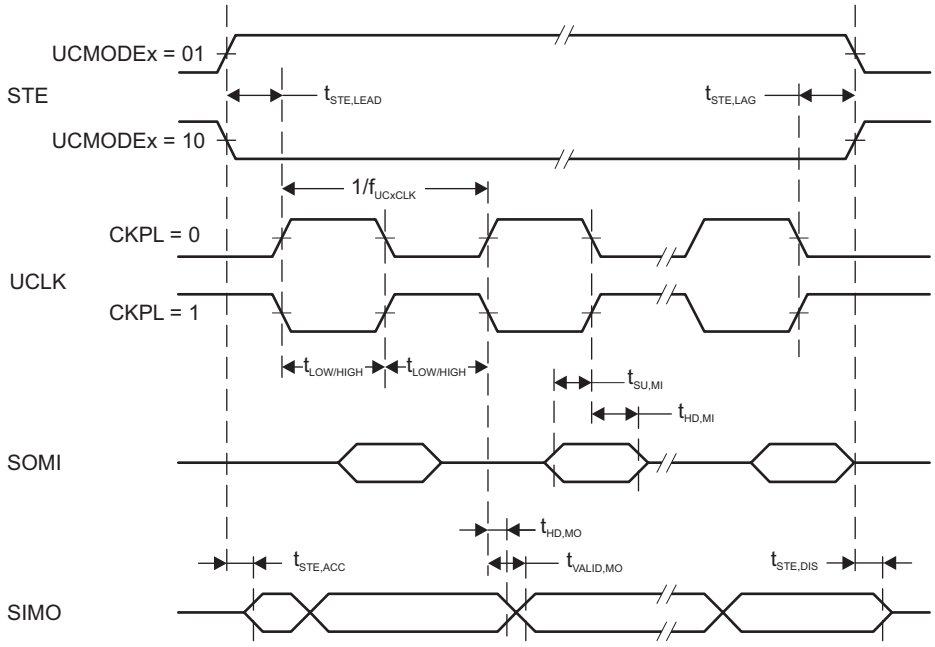


Figure 5-69. SPI Master Mode, CKPH = 0

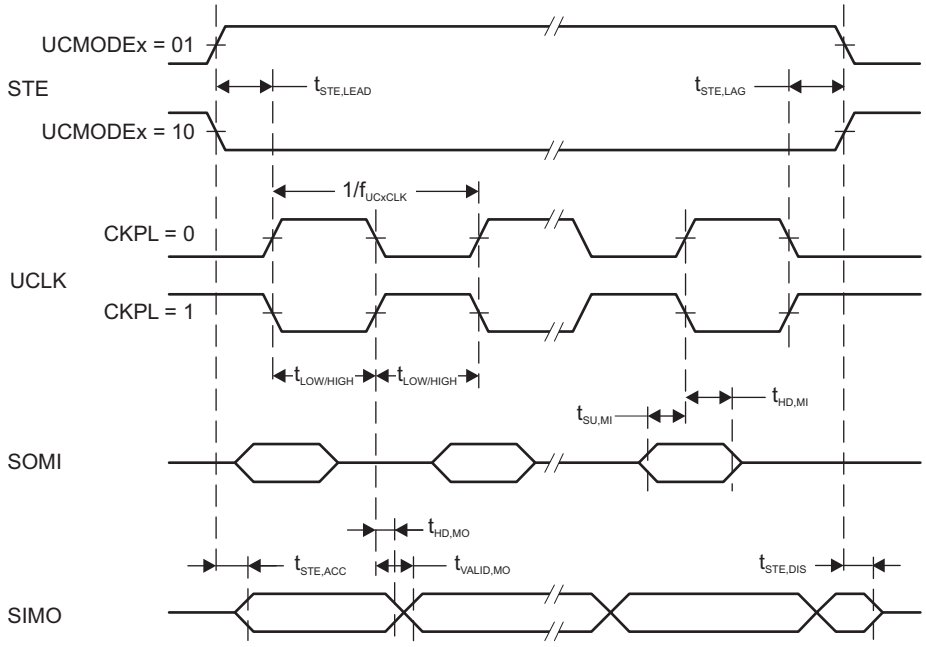


Figure 5-70. SPI Master Mode, CKPH = 1

Table 5-43 lists the characteristics of the eUSCI in SPI slave mode.

Table 5-43. eUSCI Switching Characteristics (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note (1))

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		1.62 V	45		ns
			3.7 V	20		
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		1.62 V	1		ns
			3.7 V	1		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		1.62 V		25	ns
			3.7 V		15	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		1.62 V		18	ns
			3.7 V		14	
$t_{SU,SI}$	SIMO input data setup time		1.62 V	3		ns
			3.7 V	2		
$t_{HD,SI}$	SIMO input data hold time		1.62 V	0		ns
			3.7 V	0		
$t_{VALID,SO}$	SOMI output data valid time (2)	UCLK edge to SOMI valid, C_L = 20 pF	1.62 V		35	ns
			3.7 V		18	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	1.62 V	10		ns
			3.7 V	6		

(1) $f_{UCxCLK} = 1/2\ t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-71 and Figure 5-72.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-71 and Figure 5-72.

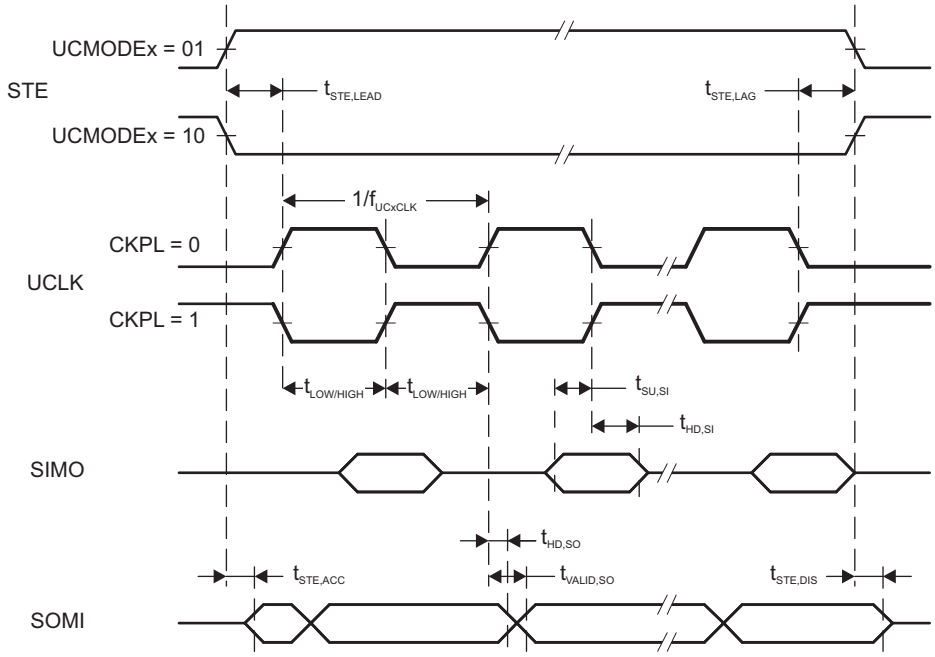


Figure 5-71. SPI Slave Mode, CKPH = 0

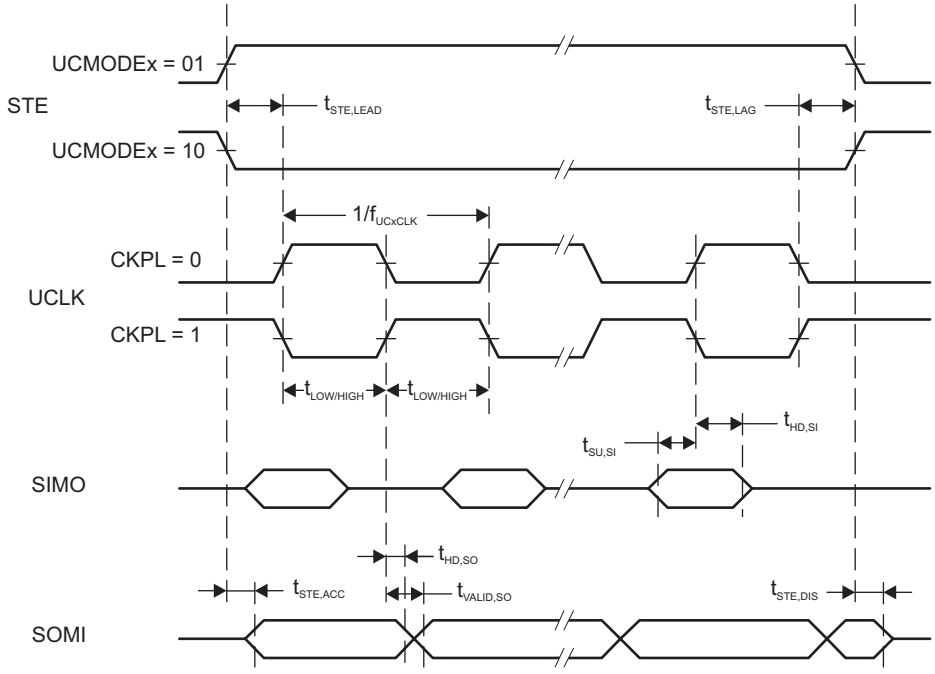


Figure 5-72. SPI Slave Mode, CKPH = 1

Table 5-44 lists the supported clock frequencies of the eUSCI in I²C mode.

Table 5-44. eUSCI Clock Frequency (I²C Mode)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, External: UCLK, Duty cycle = 50% ±10%	1.2 V			12	MHz
f_{SCL}	SCL clock frequency		1.2 V			1	MHz

Table 5-45 lists the characteristics of the eUSCI in I²C mode.

Table 5-45. eUSCI Switching Characteristics (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-73)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	4.8			µs
		f_{SCL} = 400 kHz	1.21			
		f_{SCL} = 1 MHz	0.48			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	4.9			µs
		f_{SCL} = 400 kHz	1.22			
		f_{SCL} = 1 MHz	0.47			
$t_{HD,DAT}$	Data hold time	f_{SCL} = 100 kHz	60			ns
		f_{SCL} = 400 kHz	60			
		f_{SCL} = 1 MHz	60			
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	4.7			µs
		f_{SCL} = 400 kHz	1.1			
		f_{SCL} = 1 MHz	0.35			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	4.9			µs
		f_{SCL} = 400 kHz	1.25			
		f_{SCL} = 1 MHz	0.5			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	50		120	ns
		UCGLITx = 1	25		60	
		UCGLITx = 2	10		35	
		UCGLITx = 3	5		20	
$t_{TIMEOUT}$	Clock low time-out	UCCLTOx = 1		27		ms
		UCCLTOx = 2		30		
		UCCLTOx = 3		33		

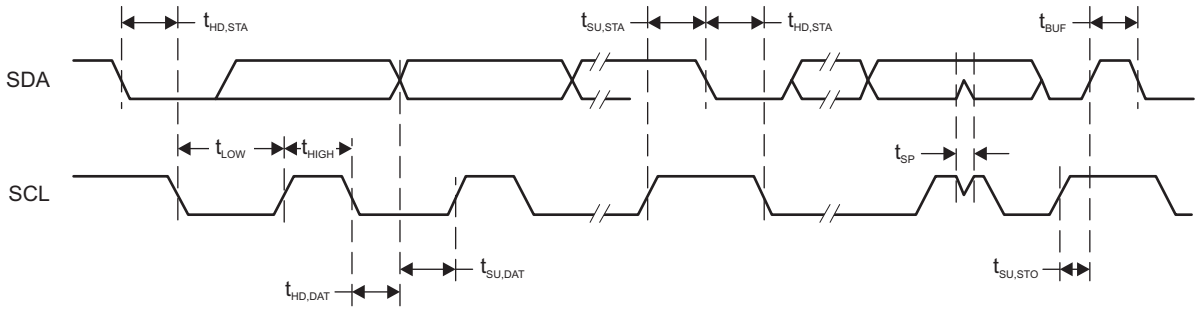


Figure 5-73. I²C Mode Timing

5.26.12 Timer_A

Table 5-46 lists the characteristics of Timer_A.

Table 5-46. Timer_A Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK External: TACLK Duty cycle = 50% ±10%	1.2 V			12	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.2 V		20		ns

Table 5-47 lists the characteristics of Timer32.

Table 5-47. Timer32 Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CORE}	V_{CC}	MIN	MAX	UNIT
f_{T32}	Timer32 operating clock frequency(1)		1.2 V			24	MHz

(1) Timer32 operates on the same clock as the Cortex-M4 CPU.

5.26.13 Memories

Table 5-48 lists the general characteristics of the flash memory.

Table 5-48. Flash Memory Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$DVCC_{PGM/ERS}$	Supply voltage for program or erase	1.62	3.7	V
$I_{PGM/ERS, PEAK}$	Peak supply current from DVCC during program or erase		10	mA
$N_{Endurance}$	Program or erase endurance(1)	20000		cycles
$t_{Retention}$	Data retention duration	20		years
$N_{PGM\_TO\_ERS}$	Number of program operations supported between erases per sector		2000	

(1) Program or erase cycle for a bit is defined as the value of bit changing from 1 to 0 to 1.

Table 5-49 lists the characteristics of the flash memory using MSP432 peripheral driver libraries.

Table 5-49. Flash Characteristics for Operations Using MSP432 Peripheral Driver Libraries(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PGM\_API, Word}$	Program time for 32-bit data using ROM_FlashCtl_programMemory() API	VCORE = 1.2 V, MCLK = 24 MHz		77	460	µs
$t_{PGM\_API, Sector}$	Program time for 4KB data (one sector) using ROM_FlashCtl_programMemory() API	VCORE = 1.2 V, MCLK = 24 MHz		6.6	90	ms
$t_{ERS\_API, Sector}$	Sector erase time using ROM_FlashCtl_eraseSector() API	VCORE = 1.2 V, MCLK = 24 MHz, Number of erase or program cycles <1000		9	315(2)	ms
		VCORE = 1.2 V, MCLK = 24 MHz, Number of erase or program cycles >1000 and <20000		9	3080(2)	
$t_{ERS\_API, Mass-Erase}$	Mass erase time using ROM_FlashCtl_performMassErase() API	VCORE = 1.2 V, MCLK = 24 MHz, Number of erase or program cycles <1000, Devices with 2MB of flash memory		57	1938(3)	ms
		VCORE = 1.2 V, MCLK = 24 MHz, Number of erase or program cycles <1000, Devices with 1MB of flash memory		33	1122(3)	
		VCORE = 1.2 V, MCLK = 24 MHz, Number of erase or program cycles <1000, Devices with 512KB of flash memory		21	714(3)	
I_{AVGPGM_API}	Average supply current from DVCC during program using ROM_FlashCtl_programMemory() API	VCORE = 1.2 V, MCLK = 3 MHz		5	7	mA
I_{AVGERS_API}	Average supply current from DVCC during erase using ROM_FlashCtl_eraseSector() API	VCORE = 1.2 V, MCLK = 3 MHz		2	3	mA

(1) MSP432 peripheral driver libraries executed from ROM.
(2) The maximum value is calculated by multiplying the typical value by N_{MAX_ERS} for the specific erase or program endurance.
(3) The maximum value is calculated by multiplying the typical value by N_{MAX_ERS} for the specific erase or program endurance and the total number of sectors in the flash main memory.

Table 5-50 lists the characteristics of the flash memory for stand-alone operations.

Table 5-50. Flash Characteristics for Stand-Alone Operations

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PGM,\ Immediate}$	Program time for one 32-bit data using immediate write mode	VER_PRE = 0, VER_PST = 1		52		µs
		VER_PRE = 1, VER_PST = 1		63		
$t_{PGM,\ Full\text{-}word}$	Program time for one 128-bit word using full word write mode	VER_PRE = 0, VER_PST = 1		49		µs
		VER_PRE = 1, VER_PST = 1		70		
$t_{PGM,\ Burst}$	Program time for 4×128-bit burst using burst write mode	AUTO_PRE = 0, AUTO_PST = 1		43		µs
		AUTO_PRE = 1, AUTO_PST = 1		64		
t_{ERS}	Time for sector erase or mass erase			9		ms
N_{MAX_PGM}	Maximum number of pulses to complete program operation				5	
N_{MAX_ERS}	Maximum number of pulses to complete erase operation	Number of erase or program cycles <1000			34	
		Number of erase or program cycles >1000 and <20000			334	

Table 5-51 lists the characteristics of the SRAM.

Table 5-51. SRAM Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SRAM_EN}	Current consumption of one SRAM bank when enabled	VCORE = 1.2 V		0.55	70	µA
I_{SRAM_RET}	Current consumption of one SRAM block under retention	VCORE = 1.2 V		29	5820	nA
$t_{SRAM\_EN,\ one}$	Time to enable one SRAM bank			8	10	µs
$t_{SRAM\_DIS,\ one}$	Time to disable one SRAM bank			8	10	µs
$t_{SRAM\_EN,\ all}$	Time to enable all SRAM banks except Bank 0			18	21	µs
$t_{SRAM\_DIS,\ all}$	Time to disable all SRAM banks except Bank 0			8	10	µs

5.26.14 Emulation and Debug

Table 5-52 lists the characteristics of the JTAG interface.

Table 5-52. JTAG Timing Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{TCK}	TCK clock frequency	0		10	MHz
t_{TCK}	TCK clock period	100			ns
t_{TCK_LOW}	TCK clock low time		$t_{TCK}/2$		ns
t_{TCK_HIGH}	TCK clock high time		$t_{TCK}/2$		ns
t_{TCK_RISE}	TCK rise time	0		10	ns
t_{TCK_FALL}	TCK fall time	0		10	ns
t_{TMS_SU}	TMS setup time to TCK rise	30			ns
t_{TMS_HLD}	TMS hold time from TCK rise	9			ns
t_{TDI_SU}	TDI setup time to TCK rise	20			ns
t_{TDI_HLD}	TDI hold time from TCK rise	7			ns
t_{TDO_ZDV}	TCK fall to data valid from high impedance		9	44	ns
t_{TDO_DV}	TCK fall to data valid from data valid		9	44	ns
t_{TDO_DVZ}	TCK fall to high impedance from data valid		8	38	ns

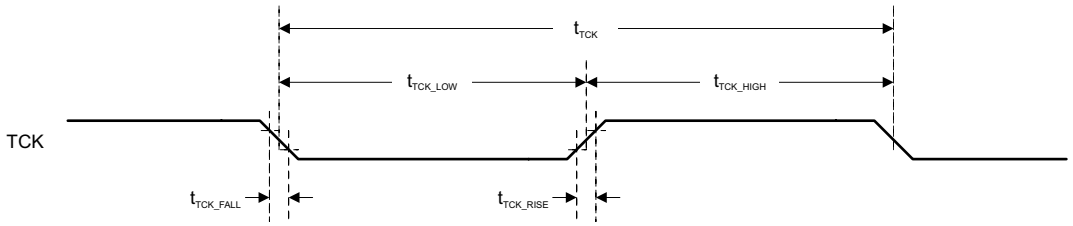


图 5-74. JTAG Test Clock Input Timing

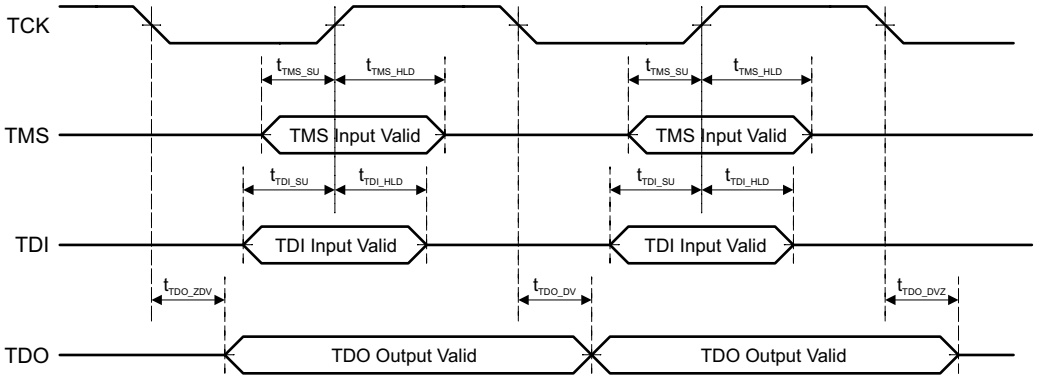


图 5-75. JTAG Test Access Port (TAP) Timing

6 Detailed Description

6.1 Overview

The MSP432P4x1xT microcontroller is an ideal combination of the TI MSP430 low-power DNA, advanced mixed-signal features, and the processing capabilities of the Arm 32-bit Cortex-M4 RISC engine. The microcontrollers ship with bundled driver libraries and are compatible with standard components of the Arm ecosystem.

6.2 Processor and Execution Features

The Arm Cortex-M4 processor provides a high-performance low-cost platform that meets system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. The Thumb®-2 mixed 16- and 32-bit instruction set of the processor delivers the high performance that is expected of a 32-bit Arm core in a compact memory size usually associated with 8- and 16-bit devices (typically in the range of a few kilobytes of memory needed for microcontroller-class applications).

In MSP432P4x1xT devices, the Cortex-M4 processor can run up to 24 MHz, delivering high performance for the targeted class of applications, while at the same time maintaining ultra-low active power consumption.

6.2.1 Floating-Point Unit (FPU)

The Cortex-M4 processor on MSP432P4x1xT devices includes a tightly coupled FPU. The FPU is an IEEE 754 compliant single-precision floating-point module that supports add, subtract, multiply, divide, accumulate, and square-root operations. The FPU also provides conversion between fixed-point and floating-point data formats and floating-point constant instructions.

6.2.2 Memory Protection Unit (MPU)

The Cortex-M4 processor on MSP432P4x1xT devices includes a tightly coupled MPU that supports up to eight protection regions. Applications can use the MPU to enforce memory privilege rules that isolate processes from each other or enforce memory access rules. These features are typically required for operating system purposes.

6.2.3 Nested Vectored Interrupt Controller (NVIC)

The NVIC supports up to 64 interrupts with eight levels of interrupt priority. The Cortex-M4 NVIC architecture allows for low latency, efficient interrupt and event handling, and seamless integration to device-level power-control strategies.

6.2.4 SysTick

The Cortex-M4 includes an integrated system timer, SysTick, that provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, and it is typically deployed either for operating-system-related purposes or as a general-purpose alarm mechanism.

6.2.5 Debug and Trace Features

The Cortex-M4 processor implements a complete hardware debug solution and provides high system visibility of the processor and memory through either a traditional 4-pin JTAG port or a 2-pin Serial Wire Debug (SWD) port, which is ideal for microcontrollers and other small-package devices. The SWJ-DP interface combines the SWD and JTAG debug ports into one module, which allows a seamless switch between the 2-pin and 4-pin modes of operation, depending on application needs.

For system trace, the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system trace events, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

注

For detailed specifications and information on the programmer's model for the Cortex-M4 CPU and the associated peripherals mentioned throughout 节 6.2, see the appropriate reference manual at www.arm.com.

6.3 Memory Map

The device supports a 4-GB address space that is divided into eight 512-MB zones (see 图 6-1).

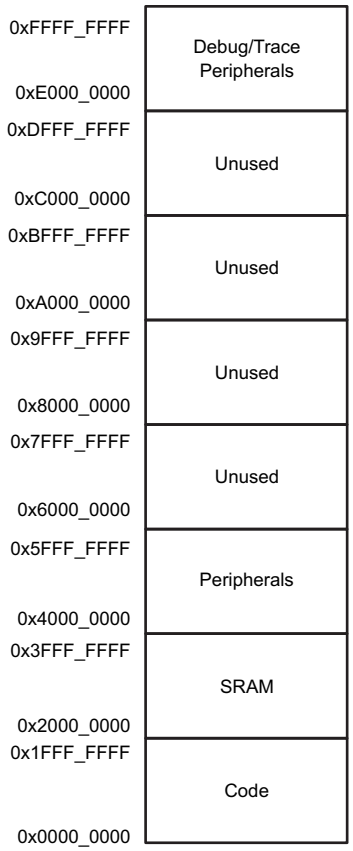


图 6-1. Device Memory Zones

6.3.1 Code Zone Memory Map

The region from 0x0000_0000 to 0x1FFF_FFFF is defined as the Code zone, and is accessible through the ICODE and DCODE buses of the Cortex-M4 processor and through the system DMA. This region maps the flash, the ROM, and the internal SRAM (permitting optimal single-cycle execution from the SRAM).

图 6-2 shows MSP432P4x1xT-specific memory map of the Code zone, as visible to the user code.

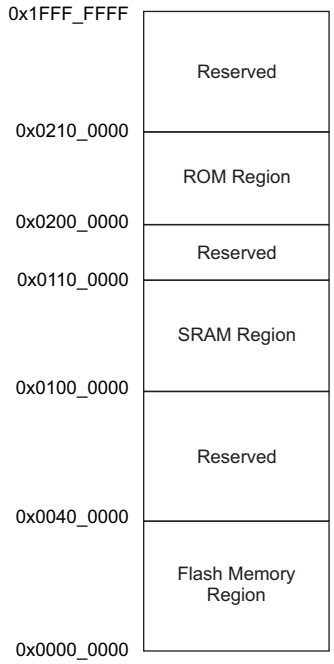


图 6-2. Code Zone Memory Map

6.3.1.1 Flash Memory Region

The 4-MB region from 0x0000_0000 to 0x003F_FFFF is defined as the flash memory region. This region is further divided into different types of flash memory regions, which are explained in 节 6.4.1.

6.3.1.2 SRAM Region

The 1-MB region from 0x0100_0000 to 0x010F_FFFF is defined as the SRAM region. This region is also aliased in the SRAM *zone* of the device, thereby allowing efficient access to the SRAM, both for instruction fetches and data reads. See 节 6.4.2 for more details.

6.3.1.3 ROM Region

The 1-MB region from 0x0200_0000 to 0x020F_FFFF is defined as the ROM region. See 节 6.4.3 for details about the ROM.

6.3.2 SRAM Zone Memory Map

The SRAM zone of the device is in the address range of 0x2000_0000 to 0x3FFF_FFFF. This range is further divided as shown in 图 6-3.

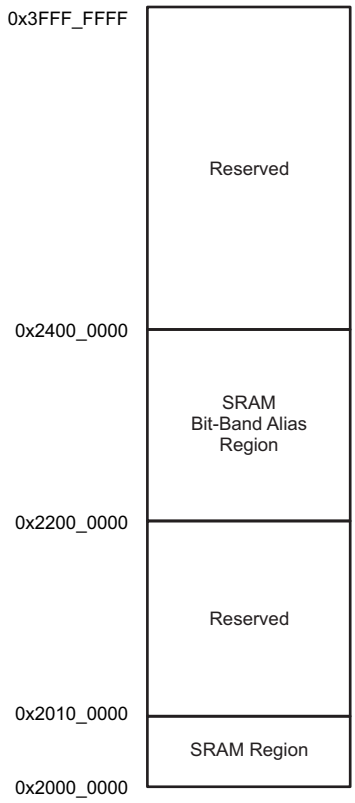


图 6-3. SRAM Zone Memory Map

6.3.2.1 SRAM Region

The 1-MB region of 0x2000_0000 to 0x200F_FFFF is defined as the SRAM region. The SRAM accessible in this region is also aliased in the Code zone of the device, thereby allowing efficient access to the SRAM for both instruction fetches and data reads. See 节 6.4.2 for details about the SRAM.

6.3.2.2 SRAM Bit-Band Alias Region

The 32-MB region of 0x2200_0000 to 0x23FF_FFFF forms the bit-band alias region for the 1-MB SRAM region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the SRAM space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

6.3.3 Peripheral Zone Memory Map

The Peripheral zone of the device is in the address range of 0x4000_0000 to 0x5FFF_FFFF. This range is further divided as shown in 图 6-4.

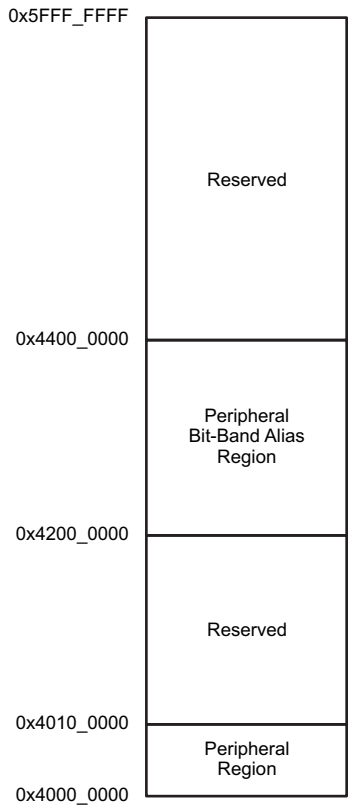


图 6-4. Peripheral Zone Memory Map

6.3.3.1 Peripheral Region

The 1-MB region of 0x4000_0000 to 0x400F_FFFF is dedicated to the system and application control peripherals of the device. On MSP432P4x1xT devices, a total of 128KB of this region is dedicated for peripherals, while the rest is reserved. lists the peripheral allocation within this 128-KB space.

注

Peripherals that are marked as 16-bit must be accessed through byte or half-word size read or write only. Any 32-bit access to these peripherals results in a bus error response.

表 6-1. Peripheral Address Offsets

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_0000 to 0x4000_03FF	Timer_A0	表 6-2	16-bit peripheral
0x4000_0400 to 0x4000_07FF	Timer_A1	表 6-3	16-bit peripheral
0x4000_0800 to 0x4000_0BFF	Timer_A2	表 6-4	16-bit peripheral
0x4000_0C00 to 0x4000_0FFF	Timer_A3	表 6-5	16-bit peripheral
0x4000_1000 to 0x4000_13FF	eUSCI_A0	表 6-6	16-bit peripheral
0x4000_1400 to 0x4000_17FF	eUSCI_A1	表 6-7	16-bit peripheral
0x4000_1800 to 0x4000_1BFF	eUSCI_A2	表 6-8	16-bit peripheral
0x4000_1C00 to 0x4000_1FFF	eUSCI_A3	表 6-9	16-bit peripheral
0x4000_2000 to 0x4000_23FF	eUSCI_B0	表 6-10	16-bit peripheral

表 6-1. Peripheral Address Offsets (continued)

ADDRESS RANGE	PERIPHERAL	TABLE	REMARKS
0x4000_2400 to 0x4000_27FF	eUSCI_B1	表 6-11	16-bit peripheral
0x4000_2800 to 0x4000_2BFF	eUSCI_B2	表 6-12	16-bit peripheral
0x4000_2C00 to 0x4000_2FFF	eUSCI_B3	表 6-13	16-bit peripheral
0x4000_3000 to 0x4000_33FF	REF_A	表 6-14	16-bit peripheral
0x4000_3400 to 0x4000_37FF	COMP_E0	表 6-15	16-bit peripheral
0x4000_3800 to 0x4000_3BFF	COMP_E1	表 6-16	16-bit peripheral
0x4000_3C00 to 0x4000_3FFF	AES256	表 6-17	16-bit peripheral
0x4000_4000 to 0x4000_43FF	CRC32	表 6-18	16-bit peripheral
0x4000_4400 to 0x4000_47FF	RTC_C	表 6-19	16-bit peripheral
0x4000_4800 to 0x4000_4BFF	WDT_A	表 6-20	16-bit peripheral
0x4000_4C00 to 0x4000_4FFF	Port Module	表 6-21	16-bit peripheral
0x4000_5000 to 0x4000_53FF	Port Mapping Controller	表 6-22	16-bit peripheral
0x4000_5400 to 0x4000_57FF	Capacitive Touch I/O 0	表 6-23	16-bit peripheral
0x4000_5800 to 0x4000_5BFF	Capacitive Touch I/O 1	表 6-24	16-bit peripheral
0x4000_5C00 to 0x4000_8FFF	Reserved		Read only, always reads 0h
0x4000_9000 to 0x4000_BFFF	Reserved		Read only, always reads 0h
0x4000_C000 to 0x4000_CFFF	Timer32	表 6-25	
0x4000_D000 to 0x4000_D7FF	Reserved		Read only, always reads 0h
0x4000_D800 to 0x4000_DFFF	Utility SRAM		
0x4000_E000 to 0x4000_FFFF	DMA	表 6-26	
0x4001_0000 to 0x4001_03FF	PCM	表 6-27	
0x4001_0400 to 0x4001_07FF	CS	表 6-28	
0x4001_0800 to 0x4001_0FFF	PSS	表 6-29	
0x4001_1000 to 0x4001_17FF	FLCTL_A	表 6-30	
0x4001_1800 to 0x4001_1BFF	Reserved		Read only, always reads 0h
0x4001_1C00 to 0x4001_1FFF	Reserved		Read only, always reads 0h
0x4001_2000 to 0x4001_23FF	Precision ADC	表 6-31	
0x4001_2400 to 0x4001_27FF	LCD_F	表 6-32	
0x4001_2800 to 0x4001_2BFF	Reserved		Read only, always reads 0h
0x4001_2C00 to 0x4001_FFFF	Reserved		Read only, always reads 0h

表 6-2. Timer_A0 Registers (Base Address: 0x4000_0000)

REGISTER NAME	ACRONYM	OFFSET
Timer_A0 Control	TA0CTL	00h
Timer_A0 Capture/Compare Control 0	TA0CCTL0	02h
Timer_A0 Capture/Compare Control 1	TA0CCTL1	04h
Timer_A0 Capture/Compare Control 2	TA0CCTL2	06h
Timer_A0 Capture/Compare Control 3	TA0CCTL3	08h
Timer_A0 Capture/Compare Control 4	TA0CCTL4	0Ah
Timer_A0 Counter	TA0R	10h
Timer_A0 Capture/Compare 0	TA0CCR0	12h
Timer_A0 Capture/Compare 1	TA0CCR1	14h
Timer_A0 Capture/Compare 2	TA0CCR2	16h
Timer_A0 Capture/Compare 3	TA0CCR3	18h
Timer_A0 Capture/Compare 4	TA0CCR4	1Ah
Timer_A0 Interrupt Vector	TA0IV	2Eh
Timer_A0 Expansion 0	TA0EX0	20h

表 6-3. Timer_A1 Registers (Base Address: 0x4000_0400)

REGISTER NAME	ACRONYM	OFFSET
Timer_A1 Control	TA1CTL	00h
Timer_A1 Capture/Compare Control 0	TA1CCTL0	02h
Timer_A1 Capture/Compare Control 1	TA1CCTL1	04h
Timer_A1 Capture/Compare Control 2	TA1CCTL2	06h
Timer_A1 Capture/Compare Control 3	TA1CCTL3	08h
Timer_A1 Capture/Compare Control 4	TA1CCTL4	0Ah
Timer_A1 Counter	TA1R	10h
Timer_A1 Capture/Compare 0	TA1CCR0	12h
Timer_A1 Capture/Compare 1	TA1CCR1	14h
Timer_A1 Capture/Compare 2	TA1CCR2	16h
Timer_A1 Capture/Compare 3	TA1CCR3	18h
Timer_A1 Capture/Compare 4	TA1CCR4	1Ah
Timer_A1 Interrupt Vector	TA1IV	2Eh
Timer_A1 Expansion 0	TA1EX0	20h

表 6-4. Timer_A2 Registers (Base Address: 0x4000_0800)

REGISTER NAME	ACRONYM	OFFSET
Timer_A2 Control	TA2CTL	00h
Timer_A2 Capture/Compare Control 0	TA2CCTL0	02h
Timer_A2 Capture/Compare Control 1	TA2CCTL1	04h
Timer_A2 Capture/Compare Control 2	TA2CCTL2	06h
Timer_A2 Capture/Compare Control 3	TA2CCTL3	08h
Timer_A2 Capture/Compare Control 4	TA2CCTL4	0Ah
Timer_A2 Counter	TA2R	10h
Timer_A2 Capture/Compare 0	TA2CCR0	12h
Timer_A2 Capture/Compare 1	TA2CCR1	14h
Timer_A2 Capture/Compare 2	TA2CCR2	16h
Timer_A2 Capture/Compare 3	TA2CCR3	18h
Timer_A2 Capture/Compare 4	TA2CCR4	1Ah
Timer_A2 Interrupt Vector	TA2IV	2Eh
Timer_A2 Expansion 0	TA2EX0	20h

表 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Control	TA3CTL	00h
Timer_A3 Capture/Compare Control 0	TA3CCTL0	02h
Timer_A3 Capture/Compare Control 1	TA3CCTL1	04h
Timer_A3 Capture/Compare Control 2	TA3CCTL2	06h
Timer_A3 Capture/Compare Control 3	TA3CCTL3	08h
Timer_A3 Capture/Compare Control 4	TA3CCTL4	0Ah
Timer_A3 Counter	TA3R	10h
Timer_A3 Capture/Compare 0	TA3CCR0	12h
Timer_A3 Capture/Compare 1	TA3CCR1	14h
Timer_A3 Capture/Compare 2	TA3CCR2	16h
Timer_A3 Capture/Compare 3	TA3CCR3	18h
Timer_A3 Capture/Compare 4	TA3CCR4	1Ah
Timer_A3 Interrupt Vector	TA3IV	2Eh

表 6-5. Timer_A3 Registers (Base Address: 0x4000_0C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Timer_A3 Expansion 0	TA3EX0	20h

表 6-6. eUSCI_A0 Registers (Base Address: 0x4000_1000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A0 Control Word 0	UCA0CTLW0	00h
eUSCI_A0 Control Word 1	UCA0CTLW1	02h
eUSCI_A0 Baud Rate Control	UCA0BRW	06h
eUSCI_A0 Modulation Control	UCA0MCTLW	08h
eUSCI_A0 Status	UCA0STATW	0Ah
eUSCI_A0 Receive Buffer	UCA0RXBUF	0Ch
eUSCI_A0 Transmit Buffer	UCA0TXBUF	0Eh
eUSCI_A0 Auto Baud Rate Control	UCA0ABCTL	10h
eUSCI_A0 IrDA Control	UCA0IRCTL	12h
eUSCI_A0 Interrupt Enable	UCA0IE	1Ah
eUSCI_A0 Interrupt Flag	UCA0IFG	1Ch
eUSCI_A0 Interrupt Vector	UCA0IV	1Eh

表 6-7. eUSCI_A1 Registers (Base Address: 0x4000_1400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A1 Control Word 0	UCA1CTLW0	00h
eUSCI_A1 Control Word 1	UCA1CTLW1	02h
eUSCI_A1 Baud Rate Control	UCA1BRW	06h
eUSCI_A1 Modulation Control	UCA1MCTLW	08h
eUSCI_A1 Status	UCA1STATW	0Ah
eUSCI_A1 Receive Buffer	UCA1RXBUF	0Ch
eUSCI_A1 Transmit Buffer	UCA1TXBUF	0Eh
eUSCI_A1 Auto Baud Rate Control	UCA1ABCTL	10h
eUSCI_A1 IrDA Control	UCA1IRCTL	12h
eUSCI_A1 Interrupt Enable	UCA1IE	1Ah
eUSCI_A1 Interrupt Flag	UCA1IFG	1Ch
eUSCI_A1 Interrupt Vector	UCA1IV	1Eh

表 6-8. eUSCI_A2 Registers (Base Address: 0x4000_1800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A2 Control Word 0	UCA2CTLW0	00h
eUSCI_A2 Control Word 1	UCA2CTLW1	02h
eUSCI_A2 Baud Rate Control	UCA2BRW	06h
eUSCI_A2 Modulation Control	UCA2MCTLW	08h
eUSCI_A2 Status	UCA2STATW	0Ah
eUSCI_A2 Receive Buffer	UCA2RXBUF	0Ch
eUSCI_A2 Transmit Buffer	UCA2TXBUF	0Eh
eUSCI_A2 Auto Baud Rate Control	UCA2ABCTL	10h
eUSCI_A2 IrDA Control	UCA2IRCTL	12h
eUSCI_A2 Interrupt Enable	UCA2IE	1Ah
eUSCI_A2 Interrupt Flag	UCA2IFG	1Ch
eUSCI_A2 Interrupt Vector	UCA2IV	1Eh

表 6-9. eUSCI_A3 Registers (Base Address: 0x4000_1C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_A3 Control Word 0	UCA3CTLW0	00h
eUSCI_A3 Control Word 1	UCA3CTLW1	02h
eUSCI_A3 Baud Rate Control	UCA3BRW	06h
eUSCI_A3 Modulation Control	UCA3MCTLW	08h
eUSCI_A3 Status	UCA3STATW	0Ah
eUSCI_A3 Receive Buffer	UCA3RXBUF	0Ch
eUSCI_A3 Transmit Buffer	UCA3TXBUF	0Eh
eUSCI_A3 Auto Baud Rate Control	UCA3ABCTL	10h
eUSCI_A3 IrDA Control	UCA3IRCTL	12h
eUSCI_A3 Interrupt Enable	UCA3IE	1Ah
eUSCI_A3 Interrupt Flag	UCA3IFG	1Ch
eUSCI_A3 Interrupt Vector	UCA3IV	1Eh

表 6-10. eUSCI_B0 Registers (Base Address: 0x4000_2000)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B0 Control Word 0	UCB0CTLW0	00h
eUSCI_B0 Control Word 1	UCB0CTLW1	02h
eUSCI_B0 Bit Rate Control Word	UCB0BRW	06h
eUSCI_B0 Status Word	UCB0STATW	08h
eUSCI_B0 Byte Counter Threshold	UCB0TBCNT	0Ah
eUSCI_B0 Receive Buffer	UCB0RXBUF	0Ch
eUSCI_B0 Transmit Buffer	UCB0TXBUF	0Eh
eUSCI_B0 I2C Own Address 0	UCB0I2COA0	14h
eUSCI_B0 I2C Own Address 1	UCB0I2COA1	16h
eUSCI_B0 I2C Own Address 2	UCB0I2COA2	18h
eUSCI_B0 I2C Own Address 3	UCB0I2COA3	1Ah
eUSCI_B0 Received Address	UCB0ADDRX	1Ch
eUSCI_B0 Address Mask	UCB0ADDMASK	1Eh
eUSCI_B0 I2C Slave Address	UCB0I2CSA	20h
eUSCI_B0 Interrupt Enable	UCB0IE	2Ah
eUSCI_B0 Interrupt Flag	UCB0IFG	2Ch
eUSCI_B0 Interrupt Vector	UCB0IV	2Eh

表 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Control Word 0	UCB1CTLW0	00h
eUSCI_B1 Control Word 1	UCB1CTLW1	02h
eUSCI_B1 Bit Rate Control Word	UCB1BRW	06h
eUSCI_B1 Status Word	UCB1STATW	08h
eUSCI_B1 Byte Counter Threshold	UCB1TBCNT	0Ah
eUSCI_B1 Receive Buffer	UCB1RXBUF	0Ch
eUSCI_B1 Transmit Buffer	UCB1TXBUF	0Eh
eUSCI_B1 I2C Own Address 0	UCB1I2COA0	14h
eUSCI_B1 I2C Own Address 1	UCB1I2COA1	16h
eUSCI_B1 I2C Own Address 2	UCB1I2COA2	18h
eUSCI_B1 I2C Own Address 3	UCB1I2COA3	1Ah
eUSCI_B1 Received Address	UCB1ADDRX	1Ch

表 6-11. eUSCI_B1 Registers (Base Address: 0x4000_2400) (continued)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B1 Address Mask	UCB1ADDMASK	1Eh
eUSCI_B1 I2C Slave Address	UCB1I2CSA	20h
eUSCI_B1 Interrupt Enable	UCB1IE	2Ah
eUSCI_B1 Interrupt Flag	UCB1IFG	2Ch
eUSCI_B1 Interrupt Vector	UCB1IV	2Eh

表 6-12. eUSCI_B2 Registers (Base Address: 0x4000_2800)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B2 Control Word 0	UCB2CTLW0	00h
eUSCI_B2 Control Word 1	UCB2CTLW1	02h
eUSCI_B2 Bit Rate Control Word	UCB2BRW	06h
eUSCI_B2 Status Word	UCB2STATW	08h
eUSCI_B2 Byte Counter Threshold	UCB2TBCNT	0Ah
eUSCI_B2 Receive Buffer	UCB2RXBUF	0Ch
eUSCI_B2 Transmit Buffer	UCB2TXBUF	0Eh
eUSCI_B2 I2C Own Address 0	UCB2I2COA0	14h
eUSCI_B2 I2C Own Address 1	UCB2I2COA1	16h
eUSCI_B2 I2C Own Address 2	UCB2I2COA2	18h
eUSCI_B2 I2C Own Address 3	UCB2I2COA3	1Ah
eUSCI_B2 Received Address	UCB2ADDRX	1Ch
eUSCI_B2 Address Mask	UCB2ADDMASK	1Eh
eUSCI_B2 I2C Slave Address	UCB2I2CSA	20h
eUSCI_B2 Interrupt Enable	UCB2IE	2Ah
eUSCI_B2 Interrupt Flag	UCB2IFG	2Ch
eUSCI_B2 Interrupt Vector	UCB2IV	2Eh

表 6-13. eUSCI_B3 Registers (Base Address: 0x4000_2C00)

REGISTER NAME	ACRONYM	OFFSET
eUSCI_B3 Control Word 0	UCB3CTLW0	00h
eUSCI_B3 Control Word 1	UCB3CTLW1	02h
eUSCI_B3 Bit Rate Control Word	UCB3BRW	06h
eUSCI_B3 Status Word	UCB3STATW	08h
eUSCI_B3 Byte Counter Threshold	UCB3TBCNT	0Ah
eUSCI_B3 Receive Buffer	UCB3RXBUF	0Ch
eUSCI_B3 Transmit Buffer	UCB3TXBUF	0Eh
eUSCI_B3 I2C Own Address 0	UCB3I2COA0	14h
eUSCI_B3 I2C Own Address 1	UCB3I2COA1	16h
eUSCI_B3 I2C Own Address 2	UCB3I2COA2	18h
eUSCI_B3 I2C Own Address 3	UCB3I2COA3	1Ah
eUSCI_B3 Received Address	UCB3ADDRX	1Ch
eUSCI_B3 Address Mask	UCB3ADDMASK	1Eh
eUSCI_B3 I2C Slave Address	UCB3I2CSA	20h
eUSCI_B3 Interrupt Enable	UCB3IE	2Ah
eUSCI_B3 Interrupt Flag	UCB3IFG	2Ch
eUSCI_B3 Interrupt Vector	UCB3IV	2Eh

表 6-14. REF_A Registers (Base Address: 0x4000_3000)

REGISTER NAME	ACRONYM	OFFSET
REF_A Control 0	REFCTL0	00h

表 6-15. COMP_E0 Registers (Base Address: 0x4000_3400)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E0 Control 0	CE0CTL0	00h
Comparator_E0 Control 1	CE0CTL1	02h
Comparator_E0 Control 2	CE0CTL2	04h
Comparator_E0 Control 3	CE0CTL3	06h
Comparator_E0 Interrupt	CE0INT	0Ch
Comparator_E0 Interrupt Vector Word	CE0IV	0Eh

表 6-16. COMP_E1 Registers (Base Address: 0x4000_3800)

REGISTER NAME	ACRONYM	OFFSET
Comparator_E1 Control 0	CE1CTL0	00h
Comparator_E1 Control 1	CE1CTL1	02h
Comparator_E1 Control 2	CE1CTL2	04h
Comparator_E1 Control 3	CE1CTL3	06h
Comparator_E1 Interrupt	CE1INT	0Ch
Comparator_E1 Interrupt Vector Word	CE1IV	0Eh

表 6-17. AES256 Registers (Base Address: 0x4000_3C00)

REGISTER NAME	ACRONYM	OFFSET
AES Accelerator Control 0	AESACTL0	00h
AES Accelerator Control 1	AESACTL1	02h
AES Accelerator Status	AESASTAT	04h
AES Accelerator Key	AESAKEY	06h
AES Accelerator Data In	AESADIN	08h
AES Accelerator Data Out	AESADOUT	0Ah
AES Accelerator XORed Data In	AESAXDIN	0Ch
AES Accelerator XORed Data In (no trigger)	AESAXIN	0Eh

表 6-18. CRC32 Registers (Base Address: 0x4000_4000)

REGISTER NAME	ACRONYM	OFFSET
CRC32 Data Input Low	CRC32DI	000h
CRC32 Data In Reverse Low	CRC32DIRB	004h
CRC32 Initialization and Result Low	CRC32INIRES_LO	008h
CRC32 Initialization and Result High	CRC32INIRES_HI	00Ah
CRC32 Result Reverse Low	CRC32RESR_LO	00Ch
CRC32 Result Reverse High	CRC32RESR_HI	00Eh
CRC16 Data Input Low	CRC16DI	010h
CRC16 Data In Reverse Low	CRC16DIRB	014h
CRC16 Initialization and Result	CRC16INIRES	018h
CRC16 Result Reverse	CRC16RESR	01Eh

表 6-19. RTC_C Registers (Base Address: 0x4000_4400)

REGISTER NAME	ACRONYM	OFFSET
Real-Time Clock Control 0	RTCCTL0	00h
Real-Time Clock Control 1, 3	RTCCTL13	02h
Real-Time Clock Offset Calibration	RTCOCAL	04h
Real-Time Clock Temperature Compensation	RTCTCMP	06h
Real-Time Prescale Timer 0 Control	RTCPS0CTL	08h
Real-Time Prescale Timer 1 Control	RTCPS1CTL	0Ah
Real-Time Prescale Timer 0, 1 Counter	RTCPS	0Ch
Real Time Clock Interrupt Vector	RTCIV	0Eh
Real-Time Clock Seconds, Minutes	RTCTIM0	10h
Real-Time Clock Hour, Day of Week	RTCTIM1	12h
Real-Time Clock Date	RTCDATE	14h
Real-Time Clock Year	RTCYEAR	16h
Real-Time Clock Minutes, Hour Alarm	RTCAMINHR	18h
Real-Time Clock Day of Week, Day of Month Alarm	RTCADOWDAY	1Ah
Binary-to-BCD Conversion	RTCBIN2BCD	1Ch
BCD-to-Binary Conversion	RTCBCD2BIN	1Eh

表 6-20. WDT_A Registers (Base Address: 0x4000_4800)

REGISTER NAME	ACRONYM	OFFSET
Watchdog Timer Control	WDTCTL	0Ch

表 6-21. Port Registers (Base Address: 0x4000_4C00)

REGISTER NAME	ACRONYM	OFFSET
Port 1 Input	P1IN	000h
Port 2 Input	P2IN	001h
Port 1 Output	P1OUT	002h
Port 2 Output	P2OUT	003h
Port 1 Direction	P1DIR	004h
Port 2 Direction	P2DIR	005h
Port 1 Resistor Enable	P1REN	006h
Port 2 Resistor Enable	P2REN	007h
Port 2 Drive Strength	P2DS	009h
Port 1 Select 0	P1SEL0	00Ah
Port 2 Select 0	P2SEL0	00Bh
Port 1 Select 1	P1SEL1	00Ch
Port 2 Select 1	P2SEL1	00Dh
Port 1 Interrupt Vector	P1IV	00Eh
Port 1 Complement Selection	P1SELC	016h
Port 2 Complement Selection	P2SELC	017h
Port 1 Interrupt Edge Select	P1IES	018h
Port 2 Interrupt Edge Select	P2IES	019h
Port 1 Interrupt Enable	P1IE	01Ah
Port 2 Interrupt Enable	P2IE	01Bh
Port 1 Interrupt Flag	P1IFG	01Ch
Port 2 Interrupt Flag	P2IFG	01Dh
Port 2 Interrupt Vector	P2IV	01Eh
Port 3 Input	P3IN	020h

表 6-21. Port Registers (Base Address: 0x4000_4C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port 4 Input	P4IN	021h
Port 3 Output	P3OUT	022h
Port 4 Output	P4OUT	023h
Port 3 Direction	P3DIR	024h
Port 4 Direction	P4DIR	025h
Port 3 Resistor Enable	P3REN	026h
Port 4 Resistor Enable	P4REN	027h
Port 3 Select 0	P3SEL0	02Ah
Port 4 Select 0	P4SEL0	02Bh
Port 3 Select 1	P3SEL1	02Ch
Port 4 Select 1	P4SEL1	02Dh
Port 3 Interrupt Vector	P3IV	02Eh
Port 3 Complement Selection	P3SELC	036h
Port 4 Complement Selection	P4SELC	037h
Port 3 Interrupt Edge Select	P3IES	038h
Port 4 Interrupt Edge Select	P4IES	039h
Port 3 Interrupt Enable	P3IE	03Ah
Port 4 Interrupt Enable	P4IE	03Bh
Port 3 Interrupt Flag	P3IFG	03Ch
Port 4 Interrupt Flag	P4IFG	03Dh
Port 4 Interrupt Vector	P4IV	03Eh
Port 5 Input	P5IN	040h
Port 6 Input	P6IN	041h
Port 5 Output	P5OUT	042h
Port 6 Output	P6OUT	043h
Port 5 Direction	P5DIR	044h
Port 6 Direction	P6DIR	045h
Port 5 Resistor Enable	P5REN	046h
Port 6 Resistor Enable	P6REN	047h
Port 5 Select 0	P5SEL0	04Ah
Port 6 Select 0	P6SEL0	04Bh
Port 5 Select 1	P5SEL1	04Ch
Port 6 Select 1	P6SEL1	04Dh
Port 5 Interrupt Vector	P5IV	04Eh
Port 5 Complement Selection	P5SELC	056h
Port 6 Complement Selection	P6SELC	057h
Port 5 Interrupt Edge Select	P5IES	058h
Port 6 Interrupt Edge Select	P6IES	059h
Port 5 Interrupt Enable	P5IE	05Ah
Port 6 Interrupt Enable	P6IE	05Bh
Port 5 Interrupt Flag	P5IFG	05Ch
Port 6 Interrupt Flag	P6IFG	05Dh
Port 6 Interrupt Vector	P6IV	05Eh
Port 7 Input	P7IN	060h
Port 8 Input	P8IN	061h
Port 7 Output	P7OUT	062h
Port 8 Output	P8OUT	063h

表 6-21. Port Registers (Base Address: 0x4000_4C00) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port 7 Direction	P7DIR	064h
Port 8 Direction	P8DIR	065h
Port 7 Resistor Enable	P7REN	066h
Port 8 Resistor Enable	P8REN	067h
Port 7 Select 0	P7SEL0	06Ah
Port 8 Select 0	P8SEL0	06Bh
Port 7 Select 1	P7SEL1	06Ch
Port 8 Select 1	P8SEL1	06Dh
Port 7 Complement Selection	P7SELC	076h
Port 8 Complement Selection	P8SELC	077h
Port 9 Input	P9IN	080h
Port 10 Input	P10IN	081h
Port 9 Output	P9OUT	082h
Port 10 Output	P10OUT	083h
Port 9 Direction	P9DIR	084h
Port 10 Direction	P10DIR	085h
Port 9 Resistor Enable	P9REN	086h
Port 10 Resistor Enable	P10REN	087h
Port 9 Select 0	P9SEL0	08Ah
Port 10 Select 0	P10SEL0	08Bh
Port 9 Select 1	P9SEL1	08Ch
Port 10 Select 1	P10SEL1	08Dh
Port 9 Complement Selection	P9SELC	096h
Port 10 Complement Selection	P10SELC	097h
Port J Input	PJIN	120h
Port J Output	PJOUT	122h
Port J Direction	PJDIR	124h
Port J Resistor Enable	PJREN	126h
Port J Select 0	PJSEL0	12Ah
Port J Select 1	PJSEL1	12Ch
Port J Complement Select	PJSELC	136h

表 6-22. PMAP Registers (Base Address: 0x4000_5000)

REGISTER NAME	ACRONYM	OFFSET
Port Mapping Key	PMAPKEYID	00h
Port Mapping Control	PMAPCTL	02h
Port Mapping P2.0	P2MAP0	10h
Port Mapping P2.1	P2MAP1	11h
Port Mapping P2.2	P2MAP2	12h
Port Mapping P2.3	P2MAP3	13h
Port Mapping P2.4	P2MAP4	14h
Port Mapping P2.5	P2MAP5	15h
Port Mapping P2.6	P2MAP6	16h
Port Mapping P2.7	P2MAP7	17h
Port Mapping P3.0	P3MAP0	18h
Port Mapping P3.1	P3MAP1	19h
Port Mapping P3.2	P3MAP2	1Ah

表 6-22. PMAP Registers (Base Address: 0x4000_5000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Port Mapping P3.3	P3MAP3	1Bh
Port Mapping P3.4	P3MAP4	1Ch
Port Mapping P3.5	P3MAP5	1Dh
Port Mapping P3.6	P3MAP6	1Eh
Port Mapping P3.7	P3MAP7	1Fh
Port Mapping P7.0	P7MAP0	38h
Port Mapping P7.1	P7MAP1	39h
Port Mapping P7.2	P7MAP2	3Ah
Port Mapping P7.3	P7MAP3	3Bh
Port Mapping P7.4	P7MAP4	3Ch
Port Mapping P7.5	P7MAP5	3Dh
Port Mapping P7.6	P7MAP6	3Eh
Port Mapping P7.7	P7MAP7	3Fh

表 6-23. Capacitive Touch I/O 0 Registers (Base Address: 0x4000_5400)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 0 Control	CAPTIO0CTL	0Eh

表 6-24. Capacitive Touch I/O 1 Registers (Base Address: 0x4000_5800)

REGISTER NAME	ACRONYM	OFFSET
Capacitive Touch I/O 1 Control	CAPTIO1CTL	0Eh

表 6-25. Timer32 Registers (Base Address: 0x4000_C000)

REGISTER NAME	ACRONYM	OFFSET
Timer 1 Load	T32LOAD1	00h
Timer 1 Current Value	T32VALUE1	04h
Timer 1 Timer Control	T32CONTROL1	08h
Timer 1 Interrupt Clear	T32INTCLR1	0Ch
Timer 1 Raw Interrupt Status	T32RIS1	10h
Timer 1 Interrupt Status	T32MIS1	14h
Timer 1 Background Load	T32BGLOAD1	18h
Timer 2 Load	T32LOAD2	20h
Timer 2 Current Value	T32VALUE2	24h
Timer 2 Timer Control	T32CONTROL2	28h
Timer 2 Interrupt Clear	T32INTCLR2	2Ch
Timer 2 Raw Interrupt Status	T32RIS2	30h
Timer 2 Interrupt Status	T32MIS2	34h
Timer 2 Background Load	T32BGLOAD2	38h

表 6-26. DMA Registers (Base Address: 0x4000_E000)

REGISTER NAME	ACRONYM	OFFSET
Device Configuration Status	DMA_DEVICE_CFG	000h
Software Channel Trigger	DMA_SW_CHTRIG	004h
Channel 0 Source Configuration	DMA_CH0_SRCCFG	010h
Channel 1 Source Configuration	DMA_CH1_SRCCFG	014h
Channel 2 Source Configuration	DMA_CH2_SRCCFG	018h

表 6-26. DMA Registers (Base Address: 0x4000_E000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Channel 3 Source Configuration	DMA_CH3_SRCCFG	01Ch
Channel 4 Source Configuration	DMA_CH4_SRCCFG	020h
Channel 5 Source Configuration	DMA_CH5_SRCCFG	024h
Channel 6 Source Configuration	DMA_CH6_SRCCFG	028h
Channel 7 Source Configuration	DMA_CH7_SRCCFG	02Ch
Interrupt 1 Source Channel Configuration	DMA_INT1_SRCCFG	100h
Interrupt 2 Source Channel Configuration	DMA_INT2_SRCCFG	104h
Interrupt 3 Source Channel Configuration	DMA_INT3_SRCCFG	108h
Interrupt 0 Source Channel Flag	DMA_INT0_SRCFLG	110h
Interrupt 0 Source Channel Clear Flag	DMA_INT0_CLRFLG	114h
Status	DMA_STAT	1000h
Configuration	DMA_CFG	1004h
Channel Control Data Base Pointer	DMA_CTLBASE	1008h
Channel Alternate Control Data Base Pointer	DMA_ALTBASE	100Ch
Channel Wait on Request Status	DMA_WAITSTAT	1010h
Channel Software Request	DMA_SWREQ	1014h
Channel Useburst Set	DMA_USEBURSTSET	1018h
Channel Useburst Clear	DMA_USEBURSTCLR	101Ch
Channel Request Mask Set	DMA_REQMASKSET	1020h
Channel Request Mask Clear	DMA_REQMASKCLR	1024h
Channel Enable Set	DMA_ENASET	1028h
Channel Enable Clear	DMA_ENACLR	102Ch
Channel Primary-Alternate Set	DMA_ALTSET	1030h
Channel Primary-Alternate Clear	DMA_ALTCLR	1034h
Channel Priority Set	DMA_PRIOSET	1038h
Channel Priority Clear	DMA_PRIOCLR	103Ch
Bus Error Clear	DMA_ERRCLR	104Ch

表 6-27. PCM Registers (Base Address: 0x4001_0000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	PCMCTL0	00h
Control 1	PCMCTL1	04h
Interrupt Enable	PCMIE	08h
Interrupt Flag	PCMIFG	0Ch
Clear Interrupt Flag	PCMCLRIFG	10h

表 6-28. CS Registers (Base Address: 0x4001_0400)

REGISTER NAME	ACRONYM	OFFSET
Key	CSKEY	00h
Control 0	CSCTL0	04h
Control 1	CSCTL1	08h
Control 2	CSCTL2	0Ch
Control 3	CSCTL3	10h
Clock Enable	CSCLKEN	30h
Status	CSSTAT	34h
Interrupt Enable	CSIE	40h
Interrupt Flag	CSIFG	48h

表 6-28. CS Registers (Base Address: 0x4001_0400) (continued)

REGISTER NAME	ACRONYM	OFFSET
Clear Interrupt Flag	CSCLRIFG	50h
Set Interrupt Flag	CSSETIFG	58h
DCO External Resistor Calibration 0	CSDCOERCAL0	60h
DCO External Resistor Calibration 1	CSDCOERCAL1	64h

表 6-29. PSS Registers (Base Address: 0x4001_0800)

REGISTER NAME	ACRONYM	OFFSET
Key	PSSKEY	00h
Control 0	PSSCTL0	04h
Interrupt Enable	PSSIE	34h
Interrupt Flag	PSSIFG	38h
Clear Interrupt Flag	PSSCLRIFG	3Ch

表 6-30. FLCTL_A Registers (Base Address: 0x4001_1000)

REGISTER NAME	ACRONYM	OFFSET
Power Status	FLCTL_POWER_STAT	000h
Bank 0 Read Control	FLCTL_BANK0_RDCTL	010h
Bank 1 Read Control	FLCTL_BANK1_RDCTL	014h
Read Burst/Compare Control and Status	FLCTL_RDBRST_CTLSTAT	020h
Read Burst/Compare Start Address	FLCTL_RDBRST_STARTADDR	024h
Read Burst/Compare Length	FLCTL_RDBRST_LEN	028h
Read Burst/Compare Fail Address	FLCTL_RDBRST_FAILADDR	03Ch
Read Burst/Compare Fail Count	FLCTL_RDBRST_FAILCNT	040h
Program Control and Status	FLCTL_PRG_CTLSTAT	050h
Program Burst Control and Status	FLCTL_PRGBRST_CTLSTAT	054h
Program Burst Start Address	FLCTL_PRGBRST_STARTADDR	058h
Program Burst Data0 0	FLCTL_PRGBRST_DATA0_0	060h
Program Burst Data0 1	FLCTL_PRGBRST_DATA0_1	064h
Program Burst Data0 2	FLCTL_PRGBRST_DATA0_2	068h
Program Burst Data0 3	FLCTL_PRGBRST_DATA0_3	06Ch
Program Burst Data1 0	FLCTL_PRGBRST_DATA1_0	070h
Program Burst Data1 1	FLCTL_PRGBRST_DATA1_1	074h
Program Burst Data1 2	FLCTL_PRGBRST_DATA1_2	078h
Program Burst Data1 3	FLCTL_PRGBRST_DATA1_3	07Ch
Program Burst Data2 0	FLCTL_PRGBRST_DATA2_0	080h
Program Burst Data2 1	FLCTL_PRGBRST_DATA2_1	084h
Program Burst Data2 2	FLCTL_PRGBRST_DATA2_2	088h
Program Burst Data2 3	FLCTL_PRGBRST_DATA2_3	08Ch
Program Burst Data3 0	FLCTL_PRGBRST_DATA3_0	090h
Program Burst Data3 1	FLCTL_PRGBRST_DATA3_1	094h
Program Burst Data3 2	FLCTL_PRGBRST_DATA3_2	098h
Program Burst Data3 3	FLCTL_PRGBRST_DATA3_3	09Ch
Erase Control and Status	FLCTL_ERASE_CTLSTAT	0A0h
Erase Sector Address	FLCTL_ERASE_SECTADDR	0A4h
Information Memory Bank 0 Write/Erase Protection	FLCTL_BANK0_INFO_WEPROT	0B0h
Information Memory Bank 1 Write/Erase Protection	FLCTL_BANK1_INFO_WEPROT	0C0h
Benchmark Control and Status	FLCTL_BMRK_CTLSTAT	0D0h

表 6-30. FLCTL_A Registers (Base Address: 0x4001_1000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Benchmark Instruction Fetch Count	FLCTL_BMRK_IFETCH	0D4h
Benchmark Data Read Count	FLCTL_BMRK_DREAD	0D8h
Benchmark Count Compare	FLCTL_BMRK_CMP	0DCh
Interrupt Flag	FLCTL_IFG	0F0h
Interrupt Enable	FLCTL_IE	0F4h
Clear Interrupt Flag	FLCTL_CLRIFG	0F8h
Set Interrupt Flag	FLCTL_SETIFG	0FCh
Read Timing Control	FLCTL_READ_TIMCTL	100h
Read Margin Timing Control	FLCTL_READMARGIN_TIMCTL	104h
Program Verify Timing Control	FLCTL_PRGVER_TIMCTL	108h
Erase Verify Timing Control	FLCTL_ERSVER_TIMCTL	10Ch
Program Timing Control	FLCTL_PROGRAM_TIMCTL	114h
Erase Timing Control	FLCTL_ERASE_TIMCTL	118h
Mass Erase Timing Control	FLCTL_MASSERASE_TIMCTL	11Ch
Burst Program Timing Control	FLCTL_BURSTPRG_TIMCTL	120h
Main Memory Bank 0 Write/Erase Protection 0	FLCTL_BANK0_MAIN_WEPROT0	200h
Main Memory Bank 0 Write/Erase Protection 1	FLCTL_BANK0_MAIN_WEPROT1	204h
Main Memory Bank 0 Write/Erase Protection 2	FLCTL_BANK0_MAIN_WEPROT2	208h
Main Memory Bank 0 Write/Erase Protection 3	FLCTL_BANK0_MAIN_WEPROT3	20Ch
Main Memory Bank 0 Write/Erase Protection 4	FLCTL_BANK0_MAIN_WEPROT4	210h
Main Memory Bank 0 Write/Erase Protection 5	FLCTL_BANK0_MAIN_WEPROT5	214h
Main Memory Bank 0 Write/Erase Protection 6	FLCTL_BANK0_MAIN_WEPROT6	218h
Main Memory Bank 0 Write/Erase Protection 7	FLCTL_BANK0_MAIN_WEPROT7	21Ch
Main Memory Bank 1 Write/Erase Protection 0	FLCTL_BANK1_MAIN_WEPROT0	240h
Main Memory Bank 1 Write/Erase Protection 1	FLCTL_BANK1_MAIN_WEPROT1	244h
Main Memory Bank 1 Write/Erase Protection 2	FLCTL_BANK1_MAIN_WEPROT2	248h
Main Memory Bank 1 Write/Erase Protection 3	FLCTL_BANK1_MAIN_WEPROT3	24Ch
Main Memory Bank 1 Write/Erase Protection 4	FLCTL_BANK1_MAIN_WEPROT4	250h
Main Memory Bank 1 Write/Erase Protection 5	FLCTL_BANK1_MAIN_WEPROT5	254h
Main Memory Bank 1 Write/Erase Protection 6	FLCTL_BANK1_MAIN_WEPROT6	258h
Main Memory Bank 1 Write/Erase Protection 7	FLCTL_BANK1_MAIN_WEPROT7	25Ch

表 6-31. Precision ADC Registers (Base Address: 0x4001_2000)

REGISTER NAME	ACRONYM	OFFSET
Control 0	ADC14CTL0	00h
Control 1	ADC14CTL1	04h
Window Comparator Low Threshold 0	ADC14LO0	08h
Window Comparator High Threshold 0	ADC14HI0	0Ch
Window Comparator Low Threshold 1	ADC14LO1	10h
Window Comparator High Threshold 1	ADC14HI1	14h
Memory Control 0	ADC14MCTL0	18h
Memory Control 1	ADC14MCTL1	1Ch
Memory Control 2	ADC14MCTL2	20h
Memory Control 3	ADC14MCTL3	24h
Memory Control 4	ADC14MCTL4	28h
Memory Control 5	ADC14MCTL5	2Ch
Memory Control 6	ADC14MCTL6	30h

表 6-31. Precision ADC Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory Control 7	ADC14MCTL7	34h
Memory Control 8	ADC14MCTL8	38h
Memory Control 9	ADC14MCTL9	3Ch
Memory Control 10	ADC14MCTL10	40h
Memory Control 11	ADC14MCTL11	44h
Memory Control 12	ADC14MCTL12	48h
Memory Control 13	ADC14MCTL13	4Ch
Memory Control 14	ADC14MCTL14	50h
Memory Control 15	ADC14MCTL15	54h
Memory Control 16	ADC14MCTL16	58h
Memory Control 17	ADC14MCTL17	5Ch
Memory Control 18	ADC14MCTL18	60h
Memory Control 19	ADC14MCTL19	64h
Memory Control 20	ADC14MCTL20	68h
Memory Control 21	ADC14MCTL21	6Ch
Memory Control 22	ADC14MCTL22	70h
Memory Control 23	ADC14MCTL23	74h
Memory Control 24	ADC14MCTL24	78h
Memory Control 25	ADC14MCTL25	7Ch
Memory Control 26	ADC14MCTL26	80h
Memory Control 27	ADC14MCTL27	84h
Memory Control 28	ADC14MCTL28	88h
Memory Control 29	ADC14MCTL29	8Ch
Memory Control 30	ADC14MCTL30	90h
Memory Control 31	ADC14MCTL31	94h
Memory 0	ADC14MEM0	98h
Memory 1	ADC14MEM1	9Ch
Memory 2	ADC14MEM2	A0h
Memory 3	ADC14MEM3	A4h
Memory 4	ADC14MEM4	A8h
Memory 5	ADC14MEM5	ACh
Memory 6	ADC14MEM6	B0h
Memory 7	ADC14MEM7	B4h
Memory 8	ADC14MEM8	B8h
Memory 9	ADC14MEM9	BCh
Memory 10	ADC14MEM10	C0h
Memory 11	ADC14MEM11	C4h
Memory 12	ADC14MEM12	C8h
Memory 13	ADC14MEM13	CCh
Memory 14	ADC14MEM14	D0h
Memory 15	ADC14MEM15	D4h
Memory 16	ADC14MEM16	D8h
Memory 17	ADC14MEM17	DCh
Memory 18	ADC14MEM18	E0h
Memory 19	ADC14MEM19	E4h
Memory 20	ADC14MEM20	E8h
Memory 21	ADC14MEM21	ECh

表 6-31. Precision ADC Registers (Base Address: 0x4001_2000) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory 22	ADC14MEM22	F0h
Memory 23	ADC14MEM23	F4h
Memory 24	ADC14MEM24	F8h
Memory 25	ADC14MEM25	FCh
Memory 26	ADC14MEM26	100
Memory 27	ADC14MEM27	104
Memory 28	ADC14MEM28	108
Memory 29	ADC14MEM29	10C
Memory 30	ADC14MEM30	110h
Memory 31	ADC14MEM31	114h
Interrupt Enable 0	ADC14IER0	13Ch
Interrupt Enable 1	ADC14IER1	140h
Interrupt Flag 0	ADC14IFGR0	144h
Interrupt Flag 1	ADC14IFGR1	148h
Clear Interrupt Flag 0	ADC14CLRIFGR0	14Ch
Clear Interrupt Flag 1	ADC14CLRIFGR1	150h
Interrupt Vector	ADC14IV	154h

表 6-32. LCD_F Registers (Base Address: 0x4001_2400)

REGISTER NAME	ACRONYM	OFFSET
Control	LCDCTL	00h
Blinking and memory control	LCDBMCTL	04h
Voltage control	LCDVCTL	08h
Port control 0	LCDPCTL0	0Ch
Port control 1	LCDPCTL1	10h
COM/SEG select register 0	LCDCSSEL0	14h
COM/SEG select register 1	LCDCSSEL1	18h
Animation Control Register	LCDANMCTL	1Ch
Interrupt enable register	LCDIE	110h
Interrupt flag register	LCDIFG	114h
Set interrupt flag register	LCDSETIFG	118h
Clear interrupt flag register	LCDCLRIFG	11Ch
Memory 0 (L0)	LCDM0	120h
Memory 1 (L1)	LCDM1	121h
Memory 2 (L2)	LCDM2	122h
Memory 3 (L3)	LCDM3	123h
Memory 4 (L4)	LCDM4	124h
Memory 5 (L5)	LCDM5	125h
Memory 6 (L6)	LCDM6	126h
Memory 7 (L7)	LCDM7	127h
Memory 8 (L8)	LCDM8	128h
Memory 9 (L9)	LCDM9	129h
Memory 10 (L10)	LCDM10	12Ah
Memory 11 (L11)	LCDM11	12Bh
Memory 12 (L12)	LCDM12	12Ch
Memory 13 (L13)	LCDM13	12Dh
Memory 14 (L14)	LCDM14	12Eh

表 6-32. LCD_F Registers (Base Address: 0x4001_2400) (continued)

REGISTER NAME	ACRONYM	OFFSET
Memory 15 (L15)	LCDM15	12Fh
Memory 16 (L16)	LCDM16	130h
Memory 17 (L17)	LCDM17	131h
Memory 18 (L18)	LCDM18	132h
Memory 19 (L19)	LCDM19	133h
Memory 20 (L20)	LCDM20	134h
Memory 21 (L21)	LCDM21	135h
Memory 22 (L22)	LCDM22	136h
Memory 23 (L23)	LCDM23	137h
Memory 24 (L24)	LCDM24	138h
Memory 25 (L25)	LCDM25	139h
Memory 26 (L26)	LCDM26	13Ah
Memory 27 (L27)	LCDM27	13Bh
Memory 28 (L28)	LCDM28	13Ch
Memory 29 (L29)	LCDM29	13Dh
Memory 30 (L30)	LCDM30	13Eh
Memory 31 (L31)	LCDM31	13Fh
Memory 32 (L32)	LCDM32	140h
Memory 33 (L33)	LCDM33	141h
Memory 34 (L34)	LCDM34	142h
Memory 35 (L35)	LCDM35	143h
Memory 36 (L36)	LCDM36	144h
Memory 37 (L37)	LCDM37	145h
Memory 38 (L38)	LCDM38	146h
Memory 39 (L39)	LCDM39	147h
Memory 40 (L40)	LCDM40	148h
Memory 41 (L41)	LCDM41	149h
Memory 42 (L42)	LCDM42	14Ah
Memory 43 (L43)	LCDM43	14Bh
Memory 44 (L44)	LCDM44	14Ch
Memory 45 (L45)	LCDM45	14Dh
Memory 46 (L46)	LCDM46	14Eh
Memory 47 (L47)	LCDM47	14Fh
Blinking memory 0 (L0)	LCDBM0	160h
Blinking memory 1 (L1)	LCDBM1	161h
Blinking memory 2 (L2)	LCDBM2	162h
Blinking memory 3 (L3)	LCDBM3	163h
Blinking memory 4 (L4)	LCDBM4	164h
Blinking memory 5 (L5)	LCDBM5	165h
Blinking memory 6 (L6)	LCDBM6	166h
Blinking memory 7 (L7)	LCDBM7	167h
Blinking memory 8 (L8)	LCDBM8	168h
Blinking memory 9 (L9)	LCDBM9	169h
Blinking memory 10 (L10)	LCDBM10	16Ah
Blinking memory 11 (L11)	LCDBM11	16Bh
Blinking memory 12 (L12)	LCDBM12	16Ch
Blinking memory 13 (L13)	LCDBM13	16Dh

表 6-32. LCD_F Registers (Base Address: 0x4001_2400) (continued)

REGISTER NAME	ACRONYM	OFFSET
Blinking memory 14 (L14)	LCDBM14	16Eh
Blinking memory 15 (L15)	LCDBM15	17Fh
Blinking memory 16 (L16)	LCDBM16	170h
Blinking memory 17 (L17)	LCDBM17	171h
Blinking memory 18 (L18)	LCDBM18	172h
Blinking memory 19 (L19)	LCDBM19	173h
Blinking memory 20 (L20)	LCDBM20	174h
Blinking memory 21 (L21)	LCDBM21	175h
Blinking memory 22 (L22)	LCDBM22	176h
Blinking memory 23 (L23)	LCDBM23	177h
Blinking memory 24 (L24)	LCDBM24	178h
Blinking memory 25 (L25)	LCDBM25	179h
Blinking memory 26 (L26)	LCDBM26	17Ah
Blinking memory 27 (L27)	LCDBM27	17Bh
Blinking memory 28 (L28)	LCDBM28	17Ch
Blinking memory 29 (L29)	LCDBM29	17Dh
Blinking memory 30 (L30)	LCDBM30	17Eh
Blinking memory 31 (L31)	LCDBM31	17Fh
Blinking memory 32 (L32)	LCDBM32	180h
Blinking memory 33 (L33)	LCDBM33	181h
Blinking memory 34 (L34)	LCDBM34	182h
Blinking memory 35 (L35)	LCDBM35	183h
Blinking memory 36 (L36)	LCDBM36	184h
Blinking memory 37 (L37)	LCDBM37	185h
Blinking memory 38 (L38)	LCDBM38	186h
Blinking memory 39 (L39)	LCDBM39	187h
Blinking memory 40 (L40)	LCDBM40	188h
Blinking memory 41 (L41)	LCDBM41	189h
Blinking memory 42 (L42)	LCDBM42	18Ah
Blinking memory 43 (L43)	LCDBM43	18Bh
Blinking memory 44 (L44)	LCDBM44	18Ch
Blinking memory 45 (L45)	LCDBM45	18Dh
Blinking memory 46 (L46)	LCDBM46	18Eh
Blinking memory 47 (L47)	LCDBM47	18Fh
Animation memory 0	LCDANM0	1A0h
Animation memory 1	LCDANM1	1A1h
Animation memory 2	LCDANM2	1A2h
Animation memory 3	LCDANM3	1A3h
Animation memory 4	LCDANM4	1A4h
Animation memory 5	LCDANM5	1A5h
Animation memory 6	LCDANM6	1A6h
Animation memory 7	LCDANM7	1A7h

6.3.3.2 Peripheral Bit Band Alias Region

The 32-MB region from 0x4200_0000 to 0x43FF_FFFF forms the bit-band alias region for the 1MB Peripheral region. Bit-banding is a feature of the Cortex-M4 processor and allows the application to set or clear individual bits throughout the peripheral memory space without using the pipeline bandwidth of the processor to carry out an exclusive read-modify-write sequence.

注

The restriction of accessing 16-bit peripherals only through byte or half-word accesses also applies to the corresponding bit-band region of these peripherals. In other words, writes to the bit-band alias region for these peripherals must be in the form of byte or half-word accesses only.

6.3.4 Debug and Trace Peripheral Zone

This zone maps the internal and external PPB regions of the Cortex-M4. The following peripherals are mapped to this zone:

- Core and System debug control registers (internal PPB)
- NVIC and other registers in the System Control space of the Cortex-M4 (internal PPB)
- FPB, DWT, ITM (internal PPB)
- TPIU, Debug ROM table (external PPB)
- Reset Controller (external PPB)
- System Controller (external PPB)

注

For the address maps of the Arm modules listed in 表 6-33, see Cortex-M4 technical reference manual at www.arm.com.

表 6-33. Debug Zone Memory Map

ADDRESS RANGE	MODULE OR PERIPHERAL	REMARKS
0xE000_0000 to 0xE000_0FFF	ITM	Internal PPB
0xE000_1000 to 0xE000_1FFF	DWT	Internal PPB
0xE000_2000 to 0xE000_2FFF	FPB	Internal PPB
0xE000_3000 to 0xE000_DFFF	Reserved	Internal PPB
0xE000_E000 to 0xE000_EFFF	Cortex-M4 System Control Space	Internal PPB
0xE000_F000 to 0xE003_FFFF	Reserved	Internal PPB
0xE004_0000 to 0xE004_0FFF	TPIU	External PPB
0xE004_1000 to 0xE004_1FFF	Reserved	External PPB
0xE004_2000 to 0xE004_23FF	Reset Controller (see 表 6-34)	External PPB
0xE004_2400 to 0xE004_2FFF	Reserved	External PPB
0xE004_3000 to 0xE004_33FF	System Controller	External PPB
0xE004_3400 to 0xE004_3FFF	Reserved	External PPB
0xE004_4000 to 0xE004_43FF	System Controller	External PPB
0xE004_4400 to 0xE00F_EFFF	Reserved	External PPB
0xE00F_F000 to 0xE00F_FFFF	ROM Table (External PPB)	External PPB
0xE010_0000 to 0xFFFF_FFFF	Reserved	Vendor Space

表 6-34. RSTCTL Registers

REGISTER NAME	ACRONYM	OFFSET
Reset Request	RSTCTL_RESET_REQ	000h
Hard Reset Status	RSTCTL_HARDRESET_STAT	004h
Hard Reset Status Clear	RSTCTL_HARDRESET_CLR	008h
Hard Reset Status Set	RSTCTL_HARDRESET_SET	00Ch
Soft Reset Status	RSTCTL_SOFTRESET_STAT	010h
Soft Reset Status Clear	RSTCTL_SOFTRESET_CLR	014h
Soft Reset Status Set	RSTCTL_SOFTRESET_SET	018h
PSS Reset Status	RSTCTL_PSSRESET_STAT	100h
PSS Reset Status Clear	RSTCTL_PSSRESET_CLR	104h
PCM Reset Status	RSTCTL_PCMRESET_STAT	108h
PCM Reset Status Clear	RSTCTL_PCMRESET_CLR	10Ch
Pin Reset Status	RSTCTL_PINRESET_STAT	110h
Pin Reset Status Clear	RSTCTL_PINRESET_CLR	114h
Reboot Reset Status	RSTCTL_REBOOTRESET_STAT	118h
Reboot Reset Status Clear	RSTCTL_REBOOTRESET_CLR	11Ch
CS Reset Status	RSTCTL_CSRESET_STAT	120h
CS Reset Status Clear	RSTCTL_CSRESET_CLR	124h

表 6-35. SYSCTL_A Registers

REGISTER NAME	ACRONYM	OFFSET
Reboot Control	SYS_REBOOT_CTL	0000h
NMI Control and Status	SYS_NMI_CTLSTAT	0004h
Watchdog Reset Control	SYS_WDTRESET_CTL	0008h
Peripheral Halt Control	SYS_PERIHALT_CTL	000Ch
SRAM Size	SYS_SRAM_SIZE	0010h
SRAM Number of Banks	SYS_SRAM_NUMBANKS	0014h
SRAM Number of Blocks	SYS_SRAM_NUMBLOCKS	0018h
Flash Main Memory Size	SYS_MAINFLASH_SIZE	0020h
Flash Information Memory Size	SYS_INFOFLASH_SIZE	0024h
Digital I/O Glitch Filter Control	SYS_DIO_GLTFLT_CTL	0030h
IP Protected Secure Zone Data Access Unlock	SYS_SECDATA_UNLOCK	0040h
SRAM Bank Enable Control 0	SYS_SRAM_BANKEN_CTL0	0050h
SRAM Block Retention Control 0	SYS_SRAM_BLKRET_CTL0	0070h
SRAM Status	SYS_SRAM_STAT	0090h
Master Unlock	SYS_MASTER_UNLOCK	1000h
Boot Override Request 0	SYS_BOOTOVER_REQ0	1004h
Boot Override Request 1	SYS_BOOTOVER_REQ1	1008h
Boot Override Acknowledge	SYS_BOOTOVER_ACK	100Ch
Reset Request	SYS_RESET_REQ	1010h
Reset Status and Override	SYS_RESET_STATOVER	1014h
System Status	SYS_SYSTEM_STAT	1020h

6.4 Memories on MSP432P4x1xT

MSP432P4x1xT devices include flash memory and SRAM for general-application purposes. In addition, the devices include a backup memory (a portion of total available SRAM) that is retained in low-power modes.

6.4.1 Flash Memory

MSP432P4x1xT devices include a high-endurance low-power flash memory that supports up to a minimum of 20000 write or erase cycles. The flash memory is 128 bits wide, thereby enabling high code execution performance by virtue of each fetch returning up to four 32-bit instructions (or up to eight 16-bit instructions). The flash is further divided into two types of subregions: Main Memory and Information Memory.

From a physical perspective, the flash memory comprises two banks, with the main and information memory regions divided equally between the two banks. This permits an application to carry out a simultaneous read or execute operation from one bank while the other bank can be undergoing a program or erase operation.

图 6-5 shows the memory map of flash on MSP432P4x1xT devices.

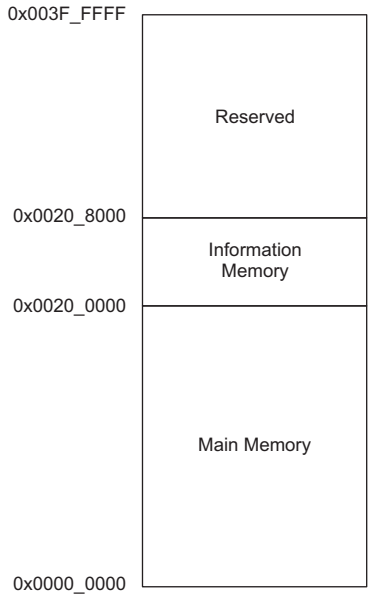


图 6-5. Flash Memory Map

6.4.1.1 Flash Main Memory (0x0000_0000 to 0x001F_FFFF)

The flash main memory on MSP432P4x1xT devices can be up to 2MB. Flash main memory consists of up to 512 sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The main memory can be viewed as two independent identical banks of up to 1MB each, allowing simultaneous read or execute from one bank while the other bank is undergoing a program or erase operation.

6.4.1.2 Flash Information Memory (0x0020_0000 to 0x0020_7FFF)

The flash information memory region is 32KB. Flash information memory consists of eight sectors of 4KB each, with a minimum erase granularity of 4KB (1 sector). The information memory can be viewed as two independent blocks of 16KB each, which allows read or execute from one block while the other block is undergoing a program or erase operation. 表 6-36 describes different regions of flash information memory and the contents of each of the regions. The flash information memory region that contains the device descriptor (TLV) is factory configured for protection against write or erase operations. Flash information memory sectors that are empty are available for user application

表 6-36. Flash Information Memory Regions

REGION	ADDRESS RANGE	CONTENTS	WRITE AND ERASE PROTECTED?
Bank 0, Sector 0	0x0020_0000 to 0x0020_0FFF	Flash Boot-override Mailbox	No
Bank 0, Sector 1	0x0020_1000 to 0x0020_1FFF	Device Descriptor (TLV)	Yes
Bank 0, Sector 2	0x0020_2000 to 0x0020_2FFF	TI BSL	No
Bank 0, Sector 3	0x0020_3000 to 0x0020_3FFF	TI BSL	No
Bank 1, Sector 0	0x0020_4000 to 0x0020_4FFF	Empty	No
Bank 1, Sector 1	0x0020_5000 to 0x0020_5FFF	Empty	No
Bank 1, Sector 2	0x0020_6000 to 0x0020_6FFF	Empty	No
Bank 1, Sector 3	0x0020_7000 to 0x0020_7FFF	Empty	No

6.4.1.3 Flash Operation

The flash memory provides multiple read and program modes of operation that the application can deploy. Up to 128 bits (memory word width) can be programmed (set from 1 to 0) in a single program operation. Although the CPU data buses are 32 bits wide, the flash can buffer 128-bit write data before initiating flash programming, thereby making it more seamless and power efficient for software to program large blocks of data at a time. In addition, the flash memory also supports a burst write mode that takes less time when compared to programming words individually. See for information on timing parameters.

The flash main and information memory regions offer write/erase protection control at a sector granularity to enable software to optimize operations like mass erase while protecting certain regions of the flash. In low-power modes of operation, the flash memory is disabled and put in a power-down state to minimize leakage.

For details on the flash memory and its various modes of operation and configuration, see the *Flash Controller A (FLCTL_A)* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*.

注

Depending on the CPU (MCLK) frequency and the active mode in use, the flash may need to be accessed with single/multiple wait states. Whenever there is a change required in the operating frequency, the application must ensure that the flash access wait states are configured correctly before making the frequency change. See the electrical specification for details on flash wait state requirements.

6.4.2 SRAM

MSP432P4x1xT devices support up to 256KB of SRAM, with the rest of the 1-MB SRAM region reserved. The SRAM is aliased in both Code and SRAM zones. This enables fast single-cycle execution of code from the SRAM, as the Cortex-M4 processor pipelines instruction fetches to memory zones other than the Code space. As with the flash memory, the SRAM can be powered down or placed in a low-leakage retention state in low-power modes of operation.

图 6-6 shows the memory map of SRAM on MSP432P4x1xT devices.

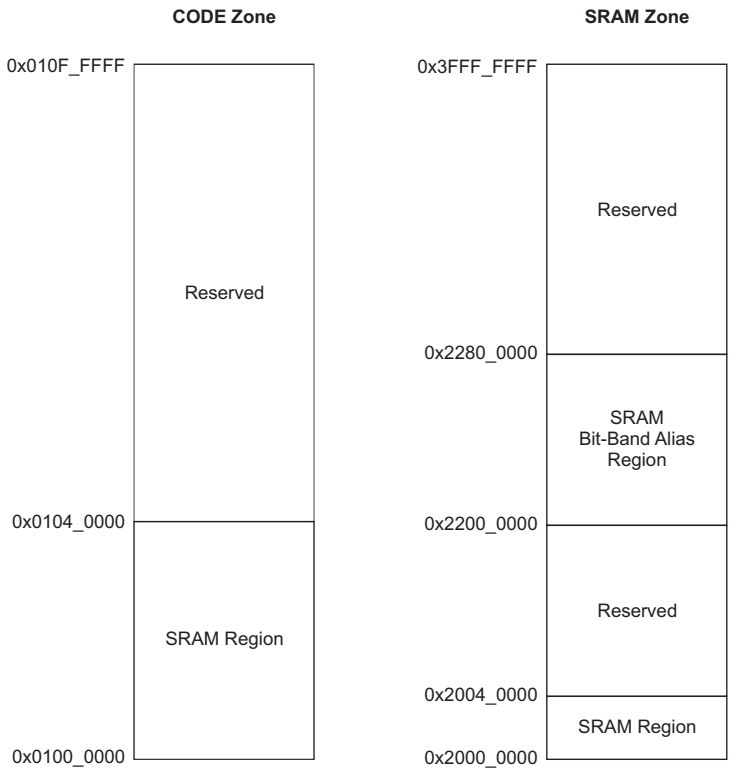


图 6-6. SRAM Map

6.4.2.1 SRAM Bank Enable Configuration

The application can optimize the power consumption of the SRAM. To enable this, the SRAM is divided into 64-KB banks that can be individually powered down. Banks that are powered down remain powered down in both active and low-power modes of operation, thereby limiting any unnecessary inrush current when the device transitions between active and retention-based low-power modes. The application can also disable one (or more) banks for a certain stage in the processing and enable it for another stage.

When a particular bank is disabled, reads to its address space return 0h, and writes are discarded. To prevent holes in the memory map, if a particular bank is enabled, all the lower banks are also forced to enabled state. This ensures a contiguous memory map through the set of enabled banks, instead of a allowing a disabled bank to appear between enabled banks. For example:

- If there are four banks in the device, the valid combinations of the BNKxx_EN fields in SYS_SRAM_BANKEN_CTL0 register are 0001, 0011, 0111, and 1111.
- Other combination of BNKxx_EN fields like 1011 are not valid, and the resultant bank configuration is automatically set to 1111.

图 6-7 shows valid and invalid combinations of bank enable settings.

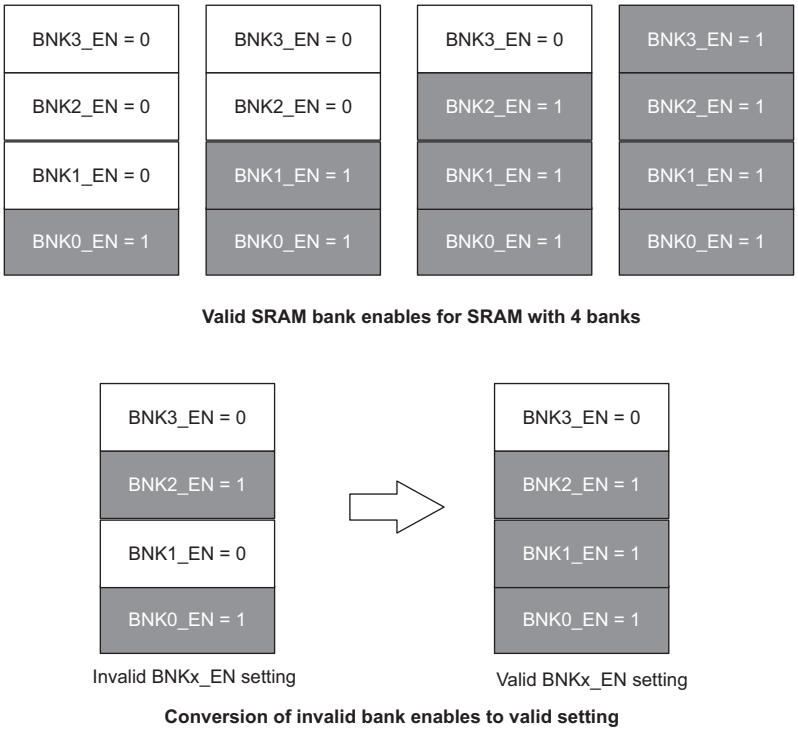


图 6-7. Configuring SRAM Bank Enables

Bank 0 of SRAM is always enabled and cannot be disabled. For all other banks, any enable or disable change results in the BNKEN_RDY bit of the SYS_SRAM_STAT register being set to 0 until the configuration change is effective. Accesses to the SRAM is stalled during this time and resumes only after the SRAM banks are ready for read or write operations. This is handled transparently and does not require any code intervention. See Table 5-51 for the SRAM bank enable or disable latency.

6.4.2.2 SRAM Block Retention Configuration and Backup Memory

The application can optimize the leakage power consumption of the SRAM in LPM3 and LPM4 modes of operation. To enable this, each SRAM bank is further divided into 8-KB blocks that can be individually configured for retention. Blocks that are enabled for retention retain their data through the LPM3 and LPM4 modes. The application can also retain a subset of the blocks in the enabled banks.

For example, the application may need 128KB of SRAM for its processing needs (two banks are kept enabled). However, of these two banks, only one 8-KB block may contain critical data that must be retained in LPM3 or LPM4, while the rest are powered off completely to minimize power consumption.

Block 0 of SRAM Bank 0 is always retained and cannot be powered down. Therefore, it also operates as a possible backup memory in the LPM3, LPM4, and LPM3.5 modes of operation.

6.4.2.3 Utility SRAM

MSP432P4x1xT devices support an additional 2KB of Utility SRAM space in the peripheral memory map region. This space can be used by the application for storing any application related data (for example, DMA descriptors).

6.4.3 ROM

MSP432P4x1xT devices support 32KB of ROM, with the rest of the 1-MB region reserved (for future upgrades). The lower 2KB of the ROM is reserved for TI internal purposes and accesses to this space return an error response. The rest of the ROM is used for driver libraries.

注

The entire ROM region returns an error response for write accesses. The lower 2KB of the ROM always returns an error response for any access.

6.5 DMA

MSP432P4x1xT devices implement an 8-channel Arm µDMA. This allows eight simultaneously active channels for data transfer between memory and peripherals without needing to use the bandwidth of the CPU (thereby reducing power by idling the CPU when there is no data processing required). In addition, the DMA remains active in multiple low-power modes of operation, allowing for a very low power state in which data can be transferred at low rates.

For maximum flexibility, up to eight DMA event sources can map to any of the eight channels. This is controlled through configuration registers in the DMA. In addition, the DMA can generate up to four interrupt requests (described in 节 6.5.2). For details regarding configuration of the DMA, see the DMA chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*.

6.5.1 DMA Source Mapping

Each of the eight available channels has a control register that can select any of the device-level DMA sources as the final source for that channel. 表 6-37 lists the sources available for mapping to each channel, based on the value of the Source Configuration (SRCCFG) register. Any source marked as Reserved is unused. It may be used for software-controlled DMA tasks, but typically it is reserved for enhancement purposes on future devices.

表 6-37. DMA Sources

CHANNEL	SRCCFG							
	0	1	2	3	4	5	6	7
0	Reserved	eUSCI_A0 TX	eUSCI_B0 TX0	eUSCI_B3 TX1	eUSCI_B2 TX2	eUSCI_B1 TX3	TA0CCR0	AES256_Trigger0
1	Reserved	eUSCI_A0 RX	eUSCI_B0 RX0	eUSCI_B3 RX1	eUSCI_B2 RX2	eUSCI_B1 RX3	TA0CCR2	AES256_Trigger1
2	Reserved	eUSCI_A1 TX	eUSCI_B1 TX0	eUSCI_B0 TX1	eUSCI_B3 TX2	eUSCI_B2 TX3	TA1CCR0	AES256_Trigger2
3	Reserved	eUSCI_A1 RX	eUSCI_B1 RX0	eUSCI_B0 RX1	eUSCI_B3 RX2	eUSCI_B2 RX3	TA1CCR2	Reserved
4	Reserved	eUSCI_A2 TX	eUSCI_B2 TX0	eUSCI_B1 TX1	eUSCI_B0 TX2	eUSCI_B3 TX3	TA2CCR0	Reserved
5	Reserved	eUSCI_A2 RX	eUSCI_B2 RX0	eUSCI_B1 RX1	eUSCI_B0 RX2	eUSCI_B3 RX3	TA2CCR2	Reserved
6	Reserved	eUSCI_A3 TX	eUSCI_B3 TX0	eUSCI_B2 TX1	eUSCI_B1 TX2	eUSCI_B0 TX3	TA3CCR0	DMAE0 (External Pin)
7	Reserved	eUSCI_A3 RX	eUSCI_B3 RX0	eUSCI_B2 RX1	eUSCI_B1 RX2	eUSCI_B0 RX3	TA3CCR2	Precision ADC

6.5.2 DMA Completion Interrupts

In the case of the Arm µDMA controller, it is usually the responsibility of software to maintain a list of channels that have completed their operation. To provide more flexibility, MSP432P4x1xT DMA supports four DMA completion interrupts, which are mapped as follows:

- DMA_INT0: Logical OR of all completion events except those that are already mapped to DMA_INT1, DMA_INT2, or DMA_INT3.
- DMA_INT1, DMA_INT2, DMA_INT3: Can be mapped to the DMA completion event of any channel.

注

Software must ensure that DMA_INT1, DMA_INT2, and DMA_INT3 are mapped to different channels, so that the same channel does not result in multiple interrupts.

6.5.3 DMA Access Privileges

The DMA has access to all of the memories and peripheral configuration interfaces of the device. If the device is configured for IP protection, DMA access to the flash is restricted to only bank 1 of the flash main and information memory regions. This restriction prevents the DMA from being used as an unauthorized access source into bank 0 of the flash, where secure data regions are housed.

6.6 Memory Map Access Details

The bus system on MSP432P4x1xT devices incorporates four masters, which can initiate various types of transactions:

- ICODE: Cortex-M4 instruction fetch bus. Accesses the Code zone only
- DCODE: Cortex-M4 data and literal load/store bus. Accesses the Code zone only. Debugger accesses to Code zone also appear on this bus.
- SBUS: Cortex-M4 data read and write bus. Accesses to all zones except Code zones and PPB memory space only. Debugger accesses to this space also appear on this bus.
- DMA: Access to all zones except the PPB memory space

注

The PPB space is dedicated only to the Cortex-M4 Private Peripheral Bus.

6.6.1 Master and Slave Access Priority Settings

表 6-38 lists all the available masters (rows) and their access permissions to slaves (columns). If multiple masters can access one slave, the table lists access priorities if arbitration is required. A lower number in the table indicates a higher arbitration priority (the priority is always fixed).

表 6-38. Master and Slave Access Priority

	FLASH MEMORY	ROM	SRAM	PERIPHERALS
ICODE	3	2	4	N/A
DCODE	2 (1)	1	2	N/A
SBUS	N/A	N/A	3	2
DMA	1 (2)	N/A	1 (3)	1

(1) Access from the DCODE to flash memory may be restricted if the device is operating in a secure mode
(2) Access from DMA to flash memory is restricted to Bank 1 if the device is operating in a secure mode with IP protection enabled. In such cases, access to Bank 0 returns an error response
(3) Although the SRAM is mapped to both Code and System spaces, accesses from DMA to SRAM must use the System space addressing ONLY.

6.6.2 Memory Map Access Response

表 6-39 summarizes the access responses to the entire memory map of MSP432P4x1xT devices.

表 6-39. Memory Map Access Response

ADDRESS RANGE	DESCRIPTION	READ (1)	WRITE (1)	INSTRUCTION FETCH (1)
0x0000_0000 to 0x001F_FFFF	Flash Main Memory	OK	OK (2), (3)	OK
0x0020_0000 to 0x0020_7FFF	Flash Information Memory	OK	OK (3)	OK
0x0020_8000 to 0x00FF_FFFF	Reserved	Error	Error	Error
0x0100_0000 to 0x0103_FFFF	SRAM	OK	OK	OK
0x0104_0000 to 0x01FF_FFFF	Reserved	Error	Error	Error
0x0200_0000 to 0x0200_07FF	ROM (Reserved)	Error	Error	Error
0x0200_0800 to 0x0200_7FFF	ROM	OK	Error	OK
0x0200_8000 to 0x1FFF_FFFF	Reserved	Error	Error	Error
0x2000_0000 to 0x2003_FFFF	SRAM	OK	OK	OK
0x2004_0000 to 0x21FF_FFFF	Reserved	Error	Error	Error
0x2200_0000 to 0x23FF_FFFF	SRAM bit-band alias	OK (4)	OK	Error
0x2400_0000 to 0x3FFF_FFFF	Reserved	Error	Error	Error
0x4000_0000 to 0x4001_FFFF	Peripheral	OK	OK	Error
0x4002_0000 to 0x41FF_FFFF	Reserved	Error	Error	Error
0x4200_0000 to 0x43FF_FFFF	Peripheral bit-band alias	OK (4)	OK	Error
0x4400_0000 to 0xDFFF_FFFF	Reserved	Error	Error	Error
0xE000_0000 to 0xE003_FFFF	Internal PPB (5)	OK	OK	Error
0xE004_0000 to 0xE004_0FFF	TPIU (External PPB)	OK	OK	Error
0xE004_1000 to 0xE004_1FFF	Reserved	Reserved	Reserved	Error
0xE004_2000 to 0xE004_23FF	Reset Controller (External PPB)	OK	OK	Error
0xE004_2400 to 0xE004_2FFF	Reserved	Reserved	Reserved	Error
0xE004_3000 to 0xE004_33FF	SYSCTL_A (External PPB)	OK	OK	Error
0xE004_3400 to 0xE004_3FFF	Reserved	Reserved	Reserved	Error
0xE004_4000 to 0xE004_43FF	SYSCTL_A (External PPB)	OK	OK	Error
0xE004_4400 to 0xE00F_EFFF	Reserved	Reserved	Reserved	Error
0xE00F_F000 to 0xE00F_FFFF	ROM Table (External PPB)	OK	OK	Error
0xE010_0000 to 0xFFFF_FFFF	Reserved	Error	Error	Error

(1) A reserved memory region returns 0h on reads and instruction fetches. Writes to this region are ignored.
(2) If the user memory address is part of a secure region, this access returns an error if it is initiated by an unauthorized source. For more details, see the device security application note.
(3) Writes to this address are ignored if the sector has write protection enabled.
(4) Reads from the bit-band region return 00h if the bit is clear and 01h if the bit is set.
(5) See the Cortex-M4 technical reference manual at www.arm.com for details of the memory map of the internal PPB.

6.7 Interrupts

The Cortex-M4 processor on MSP432P4x1xT devices implements an NVIC with 64 external interrupt lines and 8 levels of priority. From an application perspective, the interrupt sources at the device level are divided into two classes, the NMI and the User Interrupts. Internally, the CPU exception model handles the various exceptions (internal and external events including CPU instruction, memory, and bus fault conditions) in a fixed and configurable order of priority. For details on the handling of various exception priorities (including CPU reset and fault models), see the Arm-V7M architecture reference manual at www.arm.com.

6.7.1 NMI

The NMI input of the NVIC has the following possible sources:

- External NMI pin (if configured in NMI mode)
- Oscillator fault condition
- Power Supply System (PSS) generated interrupts
- Power Control Manager (PCM) generated interrupts

6.7.2 Device-Level User Interrupts

表 6-40 lists the various interrupt sources and their connection to the NVIC inputs.

注

Some sources have multiple interrupt conditions. In this case, the appropriate interrupt status or flag register of the source must be examined to differentiate between the generating conditions.

表 6-40. NVIC Interrupts

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[0]	PSS (1)	
INTISR[1]	CS (1)	
INTISR[2]	PCM (1)	
INTISR[3]	WDT_A	
INTISR[4]	FPU_INT (2)	Combined interrupt from flags in the FPSCR (part of Cortex-M4 FPU)
INTISR[5]	FLCTL_A	FLCTL_A interrupt flags
INTISR[6]	COMP_E0	Comparator_E0 interrupt flags
INTISR[7]	COMP_E1	Comparator_E1 interrupt flags
INTISR[8]	Timer_A0	TA0CCTL0.CCIFG
INTISR[9]	Timer_A0	TA0CCTLx.CCIFG (x = 1 to 4), TA0CTL.TAIFG
INTISR[10]	Timer_A1	TA1CCTL0.CCIFG
INTISR[11]	Timer_A1	TA1CCTLx.CCIFG (x = 1 to 4), TA1CTL.TAIFG
INTISR[12]	Timer_A2	TA2CCTL0.CCIFG
INTISR[13]	Timer_A2	TA2CCTLx.CCIFG (x = 1 to 4), TA2CTL.TAIFG
INTISR[14]	Timer_A3	TA3CCTL0.CCIFG
INTISR[15]	Timer_A3	TA3CCTLx.CCIFG (x = 1 to 4), TA3CTL.TAIFG
INTISR[16]	eUSCI_A0	UART or SPI mode TX, RX, and status flags
INTISR[17]	eUSCI_A1	UART or SPI mode TX, RX, and status flags
INTISR[18]	eUSCI_A2	UART or SPI mode TX, RX, and status flags
INTISR[19]	eUSCI_A3	UART or SPI mode TX, RX, and status flags
INTISR[20]	eUSCI_B0	SPI or I^2C mode TX, RX, and status flags (I^2C in multiple-slave mode)
INTISR[21]	eUSCI_B1	SPI or I^2C mode TX, RX, and status flags (I^2C in multiple-slave mode)
INTISR[22]	eUSCI_B2	SPI or I^2C mode TX, RX, and status flags (I^2C in multiple-slave mode)
INTISR[23]	eUSCI_B3	SPI or I^2C mode TX, RX, and status flags (I^2C in multiple-slave mode)
INTISR[24]	Precision ADC	IFG[0-31], LOIFG, ININFG, HIIFG, RDYIFG, OVIFG, TOVIFG
INTISR[25]	Timer32_INT1	Timer32 interrupt for Timer 1
INTISR[26]	Timer32_INT2	Timer32 interrupt for Timer 2
INTISR[27]	Timer32_INTC	Timer32 combined interrupt
INTISR[28]	AES256	AESRDYIFG
INTISR[29]	RTC_C	OFIFG, RDYIFG, TEVIFG, AIFG, RT0PSIFG, RT1PSIFG
INTISR[30]	DMA_ERR	DMA error interrupt

(1) This source can also be mapped to the system NMI. See the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual* for more details.
(2) The FPU of the Cortex-M4 can generate interrupts due to multiple floating-point exceptions. The software must process and clear the interrupt flags in the FPSCR.

表 6-40. NVIC Interrupts (continued)

NVIC INTERRUPT INPUT	SOURCE	FLAGS IN SOURCE
INTISR[31]	DMA_INT3	DMA completion interrupt 3
INTISR[32]	DMA_INT2	DMA completion interrupt 2
INTISR[33]	DMA_INT1	DMA completion interrupt 1
INTISR[34]	DMA_INT0(3)	DMA completion interrupt0
INTISR[35]	I/O Port P1	P1IFG.x (x = 0 to 7)
INTISR[36]	I/O Port P2	P2IFG.x (x = 0 to 7)
INTISR[37]	I/O Port P3	P3IFG.x (x = 0 to 7)
INTISR[38]	I/O Port P4	P4IFG.x (x = 0 to 7)
INTISR[39]	I/O Port P5	P5IFG.x (x = 0 to 7)
INTISR[40]	I/O Port P6	P6IFG.x (x = 0 to 7)
INTISR[41]	LCD_F	LCD interrupt flags
INTISR[42]	Reserved	
INTISR[43]	Reserved	
INTISR[44]	Reserved	
INTISR[45]	Reserved	
INTISR[46]	Reserved	
INTISR[47]	Reserved	
INTISR[48]	Reserved	
INTISR[49]	Reserved	
INTISR[50]	Reserved	
INTISR[51]	Reserved	
INTISR[52]	Reserved	
INTISR[53]	Reserved	
INTISR[54]	Reserved	
INTISR[55]	Reserved	
INTISR[56]	Reserved	
INTISR[57]	Reserved	
INTISR[58]	Reserved	
INTISR[59]	Reserved	
INTISR[60]	Reserved	
INTISR[61]	Reserved	
INTISR[62]	Reserved	
INTISR[63]	Reserved	

(3) DMA_INT0 has a different functionality from DMA_INT1, DMA_INT2, or DMA_INT3. See 节 6.5.2 for more details.

注

The Interrupt Service Routine (ISR) must ensure that the relevant interrupt flag in the source peripheral is cleared before returning from the ISR. If the flag is not cleared, the same interrupt may be incorrectly triggered again as a new event, even though the event has already been processed by the ISR. As there may be a few cycles of delay between the execution of the write command and the actual write reflecting in the interrupt flag register of the peripheral, TI recommends that the application carry out the write and wait for a few cycles before exiting the ISR. Alternatively, the application can read the flag to ensure that it is cleared before exiting the ISR.

6.8 System Control

System Control comprises the modules that govern the overall behavior of the device, including power management, operating modes, clocks, reset handling, and user configuration settings.

6.8.1 Device Resets

MSP432P4x1xT devices support multiple classes of reset. Each class results in a different level of initiation of device logic, thus allowing the application developer to initiate different resets based reset requirements during code development and debug. The following sections cover the classes of reset in the device

6.8.1.1 Power On/Off Reset (POR)

The POR initiates a complete initialization of the application settings and device configuration information. This class of reset may be initiated either by the PSS, the PCM, the RSTn pin, the Clock System upon DCO external resistor short-circuit fault, or the device emulation logic (through the debugger). From an application perspective, all sources of POR return the device to the same state of initialization.

注

Depending on the source of the reset, the device may exhibit different wake-up latencies from the POR. This implementation enables optimization of the reset recovery time.

6.8.1.2 Reboot Reset

A reboot reset is identical to the POR and allows the application to emulate a POR class reset without needing to cycle power to the device or activate the RSTn pin. A reboot reset can be initiated through the debugger and, hence, does not affect the debug connection to the device, while a POR results in a debug disconnect.

6.8.1.3 Hard Reset

A hard reset initializes all modules that are set up or modified by the application. This includes all peripherals and the nondebug logic of the Cortex-M4. MSP432P4x1xT devices support up to 16 sources of hard reset. 表 6-41 lists the reset source allocation. The Reset Controller registers can be used to identify the source of the reset in the device. For more details, see the *Reset Controller* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*.

表 6-41. Hard Reset Sources

RESET SOURCE NUMBER	SOURCE
0	SYSRESETREQ (system reset output of Cortex-M4)
1	WDT_A time-out (1)
2	WDT_A password violation (1)
3	FLCTL_A (2)
4	Reserved (3)
5	Reserved (3)
6	Reserved (3)
7	Reserved (3)
8	Reserved (3)
9	Reserved (3)
10	Reserved (3)
11	Reserved (3)
12	Reserved (3)
13	Reserved (3)

(1) The WDT_A generated resets can be mapped as either a hard reset or a soft reset.
(2) The FLCTL_A can generate a reset if a voltage anomaly is detected that can corrupt only flash reads and not the rest of the system.
(3) Reserved indicates that this source of Hard Reset is currently unused and left for future expansion.

表 6-41. Hard Reset Sources (continued)

RESET SOURCE NUMBER	SOURCE
14	CS (4)
15	PCM (5)

(4) The CS cannot initiate a hard reset, but if a hard reset occurs during clock source or frequency changes, the CS can extend the reset to allow the clocks to settle before releasing the system. This reduces the chance of nondeterministic behavior.
(5) The PCM cannot initiate a hard reset, but if a hard reset causes power mode changes, the PCM can extend the reset to allow the system to settle before releasing the reset. This reduces the chance of nondeterministic behavior.

6.8.1.4 Soft Reset

A soft reset affects only the execution component of the system, which is the nondebug logic in the Cortex-M4 and the WDT_A. This reset remains nonintrusive to all other peripherals and system components. MSP432P4x1xT devices support up to 16 sources of soft reset. 表 6-42 lists the reset source allocation. The Reset Controller registers can be used to identify the source of reset in the design. For more details, see the *Reset Controller* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*.

表 6-42. Soft Reset Sources

RESET SOURCE NUMBER	SOURCE
0	CPU LOCKUP condition (LOCKUP output of Cortex-M4)
1	WDT_A time-out (1)
2	WDT_A password violation (1)
3	Reserved (2)
4	Reserved (2)
5	Reserved (2)
6	Reserved (2)
7	Reserved (2)
8	Reserved (2)
9	Reserved (2)
10	Reserved (2)
11	Reserved (2)
12	Reserved (2)
13	Reserved (2)
14	Reserved (2)
15	Reserved (2)

(1) The WDT_A generated resets can be mapped as either a hard reset or a soft reset.
(2) Reserved indicates that this source of Soft Reset is currently unused and left for future expansion.

注

To support and enhance debug of reset conditions, the Reset Controller is on the PPB of the device. This allows the Reset Controller to remain accessible even if the device is stuck in a hard or soft reset state. The Reset Controller permits overrides for hard and soft resets, thereby allowing an application to regain control of the device and isolate the cause of a stuck reset.

6.8.2 Power Supply System (PSS)

The PSS controls all the power supply related functionality of the device. The PSS consists of the following components.

6.8.2.1 VCCDET

The VCCDET monitors the input voltage applied at the DVCC and AVCC pins of the device. When the V_{CC} is found to be below the operating range of the VCCDET trip points, it generates a brownout condition, thereby initiating a device reset (POR class reset).

6.8.2.2 Supply Supervisor and Monitor for High Side (SVSMH)

The SVSMH supervises and monitors the V_{CC}. SVSMH has a programmable threshold setting and can be used by the application to generate a reset or an interrupt if the V_{CC} dips below the desired threshold. In supervisor mode, the SVSMH generates a device reset (POR class reset). In monitor mode, the SVSMH generates an interrupt. The SVSMH can also be disabled if monitoring and supervision of the supply voltage are not required (offers more power savings).

6.8.2.3 Core Voltage Regulator

MSP432P4x1xT devices can be programmed to operate with either an LDO or a DC/DC as the voltage regulator for the digital logic in the core domain of the device. The DC/DC offers significant boost in power efficiency for high-current high-performance applications. The LDO is a highly efficient regulator that offers power advantages at lower V_{CC} ranges and in the ultra-low-power modes of operation.

The core operating voltage (output of the LDO or DC/DC) is automatically set by the device depending on the selected operating mode of the device (see 表 6-43 for more details). The device offers seamless switching between LDO and DC/DC operating modes and also implements a seamless DC/DC fail-safe mechanism.

6.8.3 Power Control Manager (PCM)

The PCM controls the operating modes of the device and the switching between the modes. Mode selection is controlled by the application, which can choose modes to meet its power and performance requirements. 表 6-43 lists the operating modes of the device.

表 6-43. Operating Modes

OPERATING MODE	DESCRIPTION
AM_LDO_VCORE0	LDO-based active mode, medium performance, core voltage level 0
LPM0_LDO_VCORE0	Same as AM_LDO_VCORE0, except that CPU is off (no code execution)
AM_DCDC_VCORE0	DC/DC-based active mode, medium performance, core voltage level 0
LPM0_DCDC_VCORE0	Same as AM_DCDC_VCORE0, except that CPU is off (no code execution)
AM_LF_VCORE0	LDO-based low-frequency active mode, core voltage level 0
LPM0_LF_VCORE0	Same as AM_LF_VCORE0, except that CPU is off (no code execution)
LPM3_VCORE0	LDO-based low-power mode with full state retention, core voltage level 0. In addition to RTC_C and WDT_A, other peripherals can be operational with an external or internal low-frequency clocks up to 128 kHz. 表 6-44 lists the peripherals that are available in this mode.
LPM4_VCORE0	LDO-based low-power mode with full state retention, core voltage level 0. Peripherals can be operational out of external clocks up to 128 kHz. 表 6-44 lists the peripherals that are available in this mode.
LPM3.5	LDO-based low-power mode, core voltage level 0, no retention of peripheral registers, RTC_C and WDT_A can be active.
LPM4.5	Core voltage turned off, wake up only through the reset pin or wake-up capable I/Os

6.8.3.1 Peripherals in LPM3 and LPM4

Most peripherals in MSP432P4x1xT devices can be activated in LPM3 out of low-frequency internal or external clocks. LPM4 mode is LPM3 with peripherals not clocked from internal clock sources. Some analog modules can be operational in LPM4, because they do not require a clock to operate (for example, the comparator). Activating a peripheral in LPM3 or LPM4 increases the current consumption due to its active supply current contribution but also due to an additional idle current. To limit the idle current adder, certain peripherals are combined into power islands within the device. To achieve optimal current consumption, use modules within one group and limit the number of groups with active modules. 表 6-44 lists the grouping. Modules not listed in this table are either already included in the standard LPM3 current consumption or cannot be used in LPM3 or LPM4. The idle current adder is very small at room temperature (25°C) but increases at high temperatures (125°C); see the IDLE current parameters in the electrical characteristics section for details.

表 6-44. Peripheral Groups (PG)

PG1	PG2	PG3
Timer_A0, eUSCI_A0, eUSCI_B0, Clock output on pins	Timer_A1, Timer_A2, eUSCI_A1, eUSCI_A2, eUSCI_A3, eUSCI_B1, eUSCI_B2, eUSCI_B3	Timer_A3, Precision ADC, Comp_E0, Comp_E1, REF_A, LCD_F

6.8.4 Clock System (CS)

The CS contains the sources of the various clocks in the device and also controls the mapping between sources and the clock domains in the device.

6.8.4.1 LFXT

The LFXT supports 32.768-kHz low-frequency crystals.

6.8.4.2 HFXT

The HFXT supports high-frequency crystals up to 24 MHz.

6.8.4.3 DCO

The DCO is a power-efficient tunable internal oscillator that generates up to 24 MHz.

6.8.4.4 Very-Low-Power Low-Frequency Oscillator (VLO)

The VLO is an ultra-low-power internal oscillator that generates a low-accuracy clock at typical frequency of 9.4 kHz.

6.8.4.5 Low-Frequency Reference Oscillator (REFO)

The REFO can be used as an alternate low-power lower-accuracy source of a 32.768-kHz clock instead of the LFXT. REFO can also be programmed to generate a 128-kHz clock.

6.8.4.6 Module Oscillator (MODOSC)

The MODOSC is an internal clock source that has a very-low-latency wake-up time. MODOSC is factory-calibrated to a frequency of 25 MHz. The MODOSC is typically used to supply a clock on request to modules like the ADC (when in 500-ksps conversion mode). When used as an ADC clock for the 500-ksps mode, the internal clock dividers should be enabled in the ADC to obtain a 12.5-MHz clock.

6.8.4.7 System Oscillator (SYSOSC)

The SYSOSC is a low-frequency internal clock source that has a very-low-latency wake-up time. SYSOSC is factory-calibrated to a frequency of 5 MHz. The SYSOSC drives the ADC sampling clock in the 200-ksps conversion mode. In addition, it is also used for timing of various system-level control and management operations.

6.8.4.8 Fail-Safe Mechanisms

All clock sources that operate with external components have a built-in fail-safe mechanism that automatically switches to the relevant backup source, thereby ensuring that spurious or unstable clocks never affect the device behavior. 表 6-45 lists the different types of clock source faults and the corresponding fail-safe clocks.

表 6-45. Fail-Safe Clocks

Fault Type	Fail-Safe Clock
LFXT oscillator fault	REFO clock
HFXT oscillator fault	SYSOSC clock
DCO external resistor open circuit fault	DCO clock in internal resistor mode

6.8.5 System Controller (SYSCTL_A)

The SYSCTL_A is a set of various miscellaneous features of the device, including device memory configuration, RSTn or NMI function selection, clock run or stop control, watchdog configuration for selecting reset classes, and device NMI source configuration and status. In addition, the SYSCTL_A enables device security features like JTAG and SWD lock and IP protection, which can be used to protect unauthorized accesses either to the entire device memory map or to certain selected regions of the flash.

注

Like the Cortex-M4 system control registers (in the internal PPB space), the System Controller module registers are mapped to the Cortex-M4 external PPB. This keeps the System Controller module accessible even when hard or soft resets are active.

6.9 Peripherals

6.9.1 Digital I/O

Up to 10 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt capability is available on ports P1 to P6.
- Wake-up capability from LPM3, LPM4, LPM3.5, and LPM4.5 modes over ports P1 to P6.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or in pairs (16-bit widths).
- Capacitive Touch functionality is supported on all pins of ports P1 to P10 and PJ.
- Four 20-mA high-drive I/Os over pins P2.0 to P2.3
- Glitch filtering capability on selected digital I/Os

6.9.1.1 Glitch Filtering on Digital I/Os

Some of the interrupt and wake-up capable digital I/Os can suppress glitches through the use of analog glitch filter to prevent unintentional interrupt or wake-up during device operation. The analog filter suppresses a minimum of 250-ns wide glitches. The glitch filter on these selected digital I/Os is enabled by default. If the glitch filtering capability is not required in the application, it can be bypassed using the SYS_DIO_GLTFLT_CTL register. When GLTFLT_EN bit in this register is cleared, the glitch filters on all the digital I/Os are bypassed. The glitch filter is automatically bypassed on a digital I/O when it is configured for peripheral or analog functionality by programming the respective PySEL0.x and PySEL1.x registers.

注

The glitch filter is implemented on the following digital I/Os on MSP432P4x1xT devices: P1.0, P1.4, P1.5, P3.0, P3.4, P3.5, P6.6, and P6.7.

6.9.2 Port Mapping Controller (PMAPCTL)

The port mapping controller allows flexible and reconfigurable mapping of digital functions.

6.9.2.1 Port Mapping Definitions

The port mapping controller on MSP432P4x1xT devices allows reconfigurable mapping of digital functions on ports P2, P3, and P7.

表 6-46. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_UCA0CLK	eUSCI_A0 clock input/output (direction controlled by eUSCI)	
2	PM_UCA0RXD	eUSCI_A0 UART RXD (direction controlled by eUSCI – input)	
	PM_UCA0SOMI	eUSCI_A0 SPI slave out master in (direction controlled by eUSCI)	
3	PM_UCA0TXD	eUSCI_A0 UART TXD (direction controlled by eUSCI – output)	
	PM_UCA0SIMO	eUSCI_A0 SPI slave in master out (direction controlled by eUSCI)	
4	PM_UCB0CLK	eUSCI_B0 clock input/output (direction controlled by eUSCI)	
5	PM_UCB0SDA	eUSCI_B0 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB0SIMO	eUSCI_B0 SPI slave in master out (direction controlled by eUSCI)	
6	PM_UCB0SCL	eUSCI_B0 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB0SOMI	eUSCI_B0 SPI slave out master in (direction controlled by eUSCI)	
7	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
8	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
9	PM_UCA1RXD	eUSCI_A1 UART RXD (direction controlled by eUSCI – input)	
	PM_UCA1SOMI	eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
10	PM_UCA1TXD	eUSCI_A1 UART TXD (direction controlled by eUSCI – output)	
	PM_UCA1SIMO	eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
11	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
12	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
13	PM_UCA2RXD	eUSCI_A2 UART RXD (direction controlled by eUSCI – input)	
	PM_UCA2SOMI	eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
14	PM_UCA2TXD	eUSCI_A2 UART TXD (direction controlled by eUSCI – output)	
	PM_ UCA2SIMO	eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
15	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
16	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
17	PM_UCB2SDA	eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
	PM_UCB2SIMO	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)	
18	PM_UCB2SCL	eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
	PM_UCB2SOMI	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)	
19	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
20	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
21	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
22	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
23	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
24	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
25	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
26	PM_TA1CCR3A	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
27	PM_TA1CCR4A	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4
28	PM_TA0CLK	Timer_A0 external clock input	None
	PM_C0OUT	None	Comparator-E0 output

表 6-46. Port Mapping Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
29	PM_TA1CLK	Timer_A1 external clock input	None
	PM_C1OUT	None	Comparator-E1 output
30	PM_DMAE0	DMAE0 input	None
	PM_SMCLK	None	SMCLK
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is 31. The port mapping registers are 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

表 6-47. Default Mapping

PIN NAME	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/PM_UCA1STE/L11	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
P2.1/PM_UCA1CLK/L10	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
P2.2/PM_UCA1RXD/ PM_UCA1SOMI/L9	PM_UCA1RXD/ PM_UCA1SOMI	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
P2.3/PM_UCA1TXD/ PM_UCA1SIMO/L8	PM_UCA1TXD/ PM_UCA1SIMO	eUSCI_A1 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
P2.4/PM_TA0.1/L23(1)	PM_TA0CCR1A	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
P2.5/PM_TA0.2/L22(1)	PM_TA0CCR2A	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
P2.6/PM_TA0.3/L21(1)	PM_TA0CCR3A	TA0 CCR3 capture input CCI3A	TA0 CCR3 compare output Out3
P2.7/PM_TA0.4/L20(1)	PM_TA0CCR4A	TA0 CCR4 capture input CCI4A	TA0 CCR4 compare output Out4
P3.0/PM_UCA2STE/L7	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.1/PM_UCA2CLK/L6	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
P3.2/PM_UCA2RXD/ PM_UCA2SOMI/L5	PM_UCA2RXD/ PM_UCA2SOMI	eUSCI_A2 UART RXD (direction controlled by eUSCI – input)/ eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
P3.3/PM_UCA2TXD/ PM_UCA2SIMO/L4	PM_UCA2TXD/ PM_UCA2SIMO	eUSCI_A2 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
P3.4/PM_UCB2STE/L3	PM_UCB2STE	eUSCI_B2 SPI slave transmit enable (direction controlled by eUSCI)	
P3.5/PM_UCB2CLK/L2	PM_UCB2CLK	eUSCI_B2 clock input/output (direction controlled by eUSCI)	
P3.6/PM_UCB2SIMO/ PM_UCB2SDA/L1	PM_UCB2SIMO/ PM_UCB2SDA	eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)/ eUSCI_B2 I^2C data (open drain and direction controlled by eUSCI)	
P3.7/PM_UCB2SOMI/ PM_UCB2SCL/L0	PM_UCB2SOMI/ PM_UCB2SCL	eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)/ eUSCI_B2 I^2C clock (open drain and direction controlled by eUSCI)	
P7.0/PM_SMCLK/ PM_DMAE0/R03	PM_SMCLK/ PM_DMAE0	DMAE0 input	SMCLK
P7.1/PM_C0OUT/ PM_TA0CLK/R13/LCDREF	PM_C0OUT/ PM_TA0CLK	Timer_A0 external clock input	Comparator-E0 output
P7.2/PM_C1OUT/ PM_TA1CLK/R23	PM_C1OUT/ PM_TA1CLK	Timer_A1 external clock input	Comparator-E1 output
P7.3/PM_TA0.0/R33/LCDCAP	PM_TA0CCR0A	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
P7.4/PM_TA1.4/C0.5/L31(1)	PM_TA1CCR4A	TA1 CCR4 capture input CCI4A	TA1 CCR4 compare output Out4
P7.5/PM_TA1.3/C0.4/L30(1)	PM_TA1CCR3A	TA1 CCR3 capture input CCI3A	TA1 CCR3 compare output Out3
P7.6/PM_TA1.2/C0.3/L29(1)	PM_TA1CCR2A	TA1 CCR2 capture input CCI2A	TA1 CCR2 compare output Out2
P7.7/PM_TA1.1/C0.2/L28(1)	PM_TA1CCR1A	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1

(1) Not available on the 64-pin RGC package.

6.9.3 Timer_A

Timers TA0, TA1, TA2, and TA3 are 16-bit timers and counters (Timer_A type) with five capture/compare registers each. Each timer supports multiple captures or compares, PWM outputs, and interval timing. Each timer has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each capture/compare register.

6.9.3.1 Timer_A Signal Connection Tables

表 6-48 to 表 6-51 list the interface signals of the Timer_A modules on the device and connections of the interface signals to the corresponding pins or internal signals. The following rules apply to the naming conventions used.

- The first column lists the device level pin or internal signal that sources the clocks and/or triggers into the Timer. The default assumption is that these are pins, unless specifically marked as (internal). Nomenclature used for internal signals is as follows:
  - CxOUT: output from Comparator 'x'.
  - TAx_Cy: Output from Timer 'x', Capture/Compare module 'y'.
- The second column lists the input signals of the Timer module.
- The third column lists the submodule of the Timer and also implies the functionality (Timer, Capture (Inputs or Triggers), or Compare (Outputs or PWM)).
- The fourth column lists the output signals of the Timer module.
- The fifth column lists the device-level pin or internal signal that is driven by the outputs of the Timer. The default assumption is that these are pins, unless specifically marked as (internal).

注

The pin names listed in the tables are the complete names. It is the responsibility of the software to ensure that the pin is used in the intended mode for the targeted Timer functionality.

注

Internal signals that are sourced by the Timer outputs may connect to other modules (for example, other timers or the ADC) in the device (as trigger sources).

表 6-48. TA0 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.1/PM_C0OUT/PM_TA0CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C0OUT (internal)	INCLK			
P7.3/PM_TA0.0	CCI0A	CCR0	TA0	P7.3/PM_TA0.0 TA0_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.4/PM_TA0.1	CCI1A	CCR1	TA1	P2.4/PM_TA0.1 TA0_C1 (internal) Precision ADC (internal) ADC14SHSx = {1}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.5/PM_TA0.2	CCI2A	CCR2	TA2	P2.5/PM_TA0.2 TA0_C2 (internal) Precision ADC (internal) ADC14SHSx = {2}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.6/PM_TA0.3	CCI3A	CCR3	TA3	P2.6/PM_TA0.3 TA0_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P2.7/PM_TA0.4	CCI4A	CCR4	TA4	P2.7/PM_TA0.4 TA0_C4 (internal)
TA1_C4 (Internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

表 6-49. TA1 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P7.2/PM_C1OUT/PM_TA1CLK	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
C1OUT (internal)	INCLK			
P8.0/UCB3STE/TA1.0/C0.1	CCI0A	CCR0	TA0	P8.0/UCB3STE/TA1.0/C0.1 TA1_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.7/PM_TA1.1/C0.2	CCI1A	CCR1	TA1	P7.7/PM_TA1.1/C0.2 TA1_C1 (internal) Precision ADC (internal) ADC14SHSx = {3}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.6/PM_TA1.2/C0.3	CCI2A	CCR2	TA2	P7.6/PM_TA1.2/C0.3 TA1_C2 (internal) Precision ADC (internal) ADC14SHSx = {4}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.5/PM_TA1.3/C0.4	CCI3A	CCR3	TA3	P7.5/PM_TA1.3/C0.4 TA1_C3 (internal)
C1OUT (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P7.4/PM_TA1.4/C0.5	CCI4A	CCR4	TA4	P7.4/PM_TA1.4/C0.5 TA1_C4 (internal)
TA0_C4 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

表 6-50. TA2 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P4.2/ACLK/TA2CLK/A11	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 0 (internal)	INCLK			
P8.1/UCB3CLK/TA2.0/C0.0	CCI0A	CCR0	TA0	P8.1/UCB3CLK/TA2.0/C0.0 TA2_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.6/TA2.1/VREF+/VeREF+/C1.7	CCI1A	CCR1	TA1	P5.6/TA2.1/VREF+/VeREF+/C1.7 TA2_C1 (internal) Precision ADC (internal) ADC14SHSx = {5}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P5.7/TA2.2/VREF-/VeREF-/C1.6	CCI2A	CCR2	TA2	P5.7/TA2.2/VREF-/VeREF-/C1.6 TA2_C2 (internal) Precision ADC (internal) ADC14SHSx = {6}
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	CCI3A	CCR3	TA3	P6.6/TA2.3/UCB3SIMO/ UCB3SDA/C1.1 TA2_C3 (internal)
TA3_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	CCI4A	CCR4	TA4	P6.7/TA2.4/UCB3SOMI/ UCB3SCL/C1.0 TA2_C4 (internal)
From Capacitive Touch I/O 0 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

表 6-51. TA3 Signal Connections

DEVICE INPUT PIN OR INTERNAL SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT PIN OR INTERNAL SIGNAL
P8.3/TA3CLK/A22	TACLK	Timer	N/A	N/A
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
From Capacitive Touch I/O 1 (internal)	INCLK			
P10.4/TA3.0/C0.7	CCI0A	CCR0	TA0	P10.4/TA3.0/C0.7 TA3_C0 (internal)
DV_{SS}	CCI0B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P10.5/TA3.1/C0.6	CCI1A	CCR1	TA1	P10.5/TA3.1/C0.6 TA3_C1 (internal) Precision ADC (internal) ADC14SHSx = {7}
ACLK (internal)	CCI1B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P8.2/TA3.2/A23	CCI2A	CCR2	TA2	P8.2/TA3.2/A23 TA3_C2 (internal)
C0OUT (internal)	CCI2B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.2/TA3.3	CCI3A	CCR3	TA3	P9.2/TA3.3 TA3_C3 (internal)
TA2_C3 (internal)	CCI3B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			
P9.3/TA3.4	CCI4A	CCR4	TA4	P9.3/TA3.4 TA3_C4 (internal)
From Capacitive Touch I/O 1 (internal)	CCI4B			
DV_{SS}	GND			
DV_{CC}	V_{CC}			

6.9.4 Timer32

Timer32 is an Arm dual 32-bit timer module. It contains two 32-bit timers, each of which can be configured as two independent 16-bit timers. The two timers can generate independent events or a combined event, which can be processed according to application requirements.

6.9.5 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI modules are used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3-pin or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module provides support for SPI (3-pin or 4-pin), UART, enhanced UART, and IrDA.

The eUSCI_Bn module provides support for SPI (3-pin or 4-pin) and I^2C.

MSP432P4x1xT devices offer up to four eUSCI_A and four eUSCI_B modules.

6.9.6 Real-Time Clock (RTC_C)

The RTC_C module contains an integrated real-time clock. It integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C operation is available in LPM3 and LPM3.5 modes to minimize power consumption.

6.9.7 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart if a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

The watchdog can generate a reset on either a time-out or a password violation. This reset can be configured to generate either a Hard Reset or a Soft Reset into the system. See the *WDT_A* chapter in *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual* for more details.

表 6-52. WDT_A Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	BCLK

CAUTION

The WDT must be set to interval mode before transitioning into the LPM3 or LPM3.5 modes of operation. This allows the WDT event to wake the device and return it to active modes of operation. Using the WDT in watchdog mode may result in nondeterministic behavior due to the generated reset.

6.9.8 Precision ADC

The Precision ADC module can achieve up to 16-bit precision with software oversampling, up to 500-ksps sampling rate with differential and single-ended inputs. The module implements a native 14-bit SAR core, sample-and-hold circuit, reference generator, and a conversion result buffer. The window comparators with lower and upper limits allow CPU-independent result monitoring through window comparator interrupt flags.

表 6-53 summarizes the available Precision ADC external trigger sources.

表 6-53. Precision ADC Trigger Signal Connections

ADC14SHSx		CONNECTED TRIGGER SOURCE
BINARY	DECIMAL	
000	0	Software (ADC14SC)
001	1	TA0_C1
010	2	TA0_C2
011	3	TA1_C1
100	4	TA1_C2
101	5	TA2_C1
110	6	TA2_C2
111	7	TA3_C1

表 6-54 and 表 6-55 list the available multiplexing between internal and external analog inputs of the Precision ADC.

表 6-54. Precision ADC Channel Mapping on 100-Pin PZ Devices

Precision ADC CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 23	A23	Battery Monitor	ADC14BATMAP
Channel 22	A22	Temperature Sensor	ADC14TCMAP
Channel 21	A21	N/A (Reserved)	ADC14CH0MAP
Channel 20	A20	N/A (Reserved)	ADC14CH1MAP
Channel 19	A19	N/A (Reserved)	ADC14CH2MAP
Channel 18	A18	N/A (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as N/A or Reserved, it indicates that only the external source is available for that channel.
(2) See the Precision ADC chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

表 6-55. Precision ADC Channel Mapping on 64-Pin RGC Devices

Precision ADC CHANNEL	EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0)	INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1)	CONTROL BIT(2)
Channel 23	N/A	Battery Monitor	ADC14BATMAP
Channel 22	N/A	Temperature Sensor	ADC14TCMAP
Channel 11	A11	Battery Monitor	ADC14BATMAP
Channel 10	A10	Temperature Sensor	ADC14TCMAP
Channel 9	A9	N/A (Reserved)	ADC14CH0MAP
Channel 8	A8	N/A (Reserved)	ADC14CH1MAP
Channel 7	A7	N/A (Reserved)	ADC14CH2MAP
Channel 6	A6	N/A (Reserved)	ADC14CH3MAP

(1) If an internal source is marked as N/A or Reserved, only the external source is available for that channel.
(2) See the *Precision ADC* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual* for details on the registers that contain the control bits listed in the table.

6.9.9 Comparator_E (COMP_E)

The primary function of the COMP_E module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

Two COMP_E modules are available on MSP432P4x1xT devices.

6.9.10 Shared Reference (REF_A)

The REF_A generates all critical reference voltages that can be used by the various analog peripherals in the device. The reference voltage from REF_A can also be output on a device pin for external use.

6.9.11 LCD Controller (LCD_F)

The LCD_F driver generates the segment and common signals that are required to drive a liquid crystal display (LCD). The LCD_F controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, and 8-mux LCDs are supported. The module also provides an automatic blinking capability for individual segments. The module provides for automatic animation capability over eight of the segment lines.

6.9.12 CRC32

The CRC32 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. It supports both a CRC32 and a CRC16 computation.

- The CRC16 computation signature is based on the CRC16-CCITT standard.
- The CRC32 computation signature is based on the CRC32-ISO 3309 standard.

6.9.13 AES256 Accelerator

The AES accelerator module performs encryption and decryption of 128-bit data with 128-, 192-, or 256-bit keys according to the Advanced Encryption Standard (AES) (FIPS PUB 197) in hardware.

6.9.14 True Random Seed

The Device Descriptor Information (TLV) section contains a 128-bit true random seed that can be used to implement a deterministic random number generator.

6.10 Code Development and Debug

MSP432P4x1xT devices support various methods through which the user can carry out code development and debug on the device.

6.10.1 JTAG and Serial Wire Debug (SWD) Based Development, Debug, and Trace

The device supports both 4-pin JTAG and the 2-pin SWD modes of operation. The device is compatible with all standard Cortex-M4 debuggers available in the market today. The debug logic in the device has been designed to remain minimally intrusive to the application state. In low-power modes, the user can enable the debugger to override the state of the PSS, thereby gaining access to debug and trace features.

In 2-pin SWD mode, the TDO pin can be used to export serial wire trace output (SWO) data. In addition, the TDI and TDO pins of the device can be reassigned as user I/Os. See 节 6.12.24 and 节 6.12.25 for more details.

注

If the device has activated debug security, debugger accesses into the device is disabled. The debugger, however, can still detect the run or halt state of the CPU. More control of and visibility into the device is possible only after initiating a mass erase of the device flash contents.

6.10.2 Peripheral Halt Control

The Peripheral Halt Control register in the System Controller module gives the user independent control over the functionality of device peripherals during code development and debug. When the CPU is halted, the bits in this register can control whether the corresponding peripheral freezes its operation (such as incrementing, transmit, and receive) or continues its operation (debug remains nonintrusive). The registers of the peripheral remain accessible without regard to the values in the Peripheral Halt Control Register.

6.10.3 Bootloader (BSL)

The BSL users program flash or SRAM on the device using a UART, I^2C, or SPI. Access to the device memory through the BSL is protected by a user-defined password. 表 6-56 lists the pins required for the BSL.

表 6-56. BSL Pins and Functions

DEVICE PIN	BSL FUNCTION
P1.2	UART BSLRXD

表 6-56. BSL Pins and Functions (continued)

DEVICE PIN	BSL FUNCTION
P1.3	UART BSLTXD
P1.4	SPI BSLSTE
P1.5	SPI BSLCLK
P1.6	SPI BSLSIMO
P1.7	SPI BSLSOMI
P3.6	I^2C BSLSDA
P3.7	I^2C BSLSCL

The BSL is invoked under any of the following conditions.

- Erasure of flash main memory
- Hardware invocation of BSL
- Software-based API calls to BSL functions

The user can perform hardware invocation of BSL using any pin of ports P1, P2, or P3. The pin selected for this purpose should not be same as the ones used for BSL. The user can configure the device pin and its polarity through the flash boot-override mailbox. The BSL can then be invoked upon a power cycle or POR reset event with the configured pin.

For the complete description of the BSL features and its implementation, see the *MSP432P4xx SimpleLink™ Microcontrollers Bootloader (BSL) User's Guide*.

6.10.4 Device Security

The MSP432P4x1xT MCUs offer the following two types of device security for the user application code programmed on to the device.

- JTAG and SWD lock
- IP protection

JTAG and SWD lock as the name indicates locks the JTAG and SWD interface of the device. IP protection is useful for protection of customer software IP, for example, in multiple-vendor development scenarios. It is possible to have up to four IP protected zones with configurable start address and size. The security configurations of the device are set using the flash boot-override mailbox.

The SYSCTL_A module provides infrastructure for encrypted in-field updates to the application code on devices that are JTAG and SWD locked or have defined IP protection zones. For complete details of the device security features, see the *SYSCTL_A* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*.

6.11 Performance Benchmarks

The MSP432P4x1xT MCUs achieve the performance benchmarks in the following section under the software configurations and profile configurations given for each benchmark. These performance benchmarks are done with system supply voltage of 2.97 V at ambient temperature of 25°C.

6.11.1 CoreMark/MHz Performance: 3.41

表 6-57 lists the software configuration for the CoreMark test.

表 6-57. Software Configuration

Items	Details
Compiler Name and Version	IAR EWARM v6.70.3
Compiler Flags	--no_size_constraints --debug --endian=little --cpu=Cortex-M4F -e --fpu=None --dlib_config C:\Program Files (x86)\IAR Systems\Embedded Workbench 6.\arm\INC\c\DLib_Config_Normal.h -Ohs
CoreMark Profile and Version	v1.0

表 6-58 lists the profile configuration for the CoreMark test.

表 6-58. Profile Configuration

Configuration	Details
Active Power Mode Name	Active mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.62 V

6.11.2 DMIPS/MHz (Dhrystone 2.1) Performance: 1.196

表 6-59 lists the software configuration for the Dhrystone test.

表 6-59. Software Configuration

Items	Details
Compiler Name and Version	Keil uVision Arm Compiler v5.06(build 20)
Compiler Flags	-c --cpu Cortex-M4.fp -g -O3 -Otime --apcs=interwork --asm --interleave --asm_dir
Dhrystone Profile and Version	v2.1

表 6-60 lists the profile configuration for the Dhrystone test.

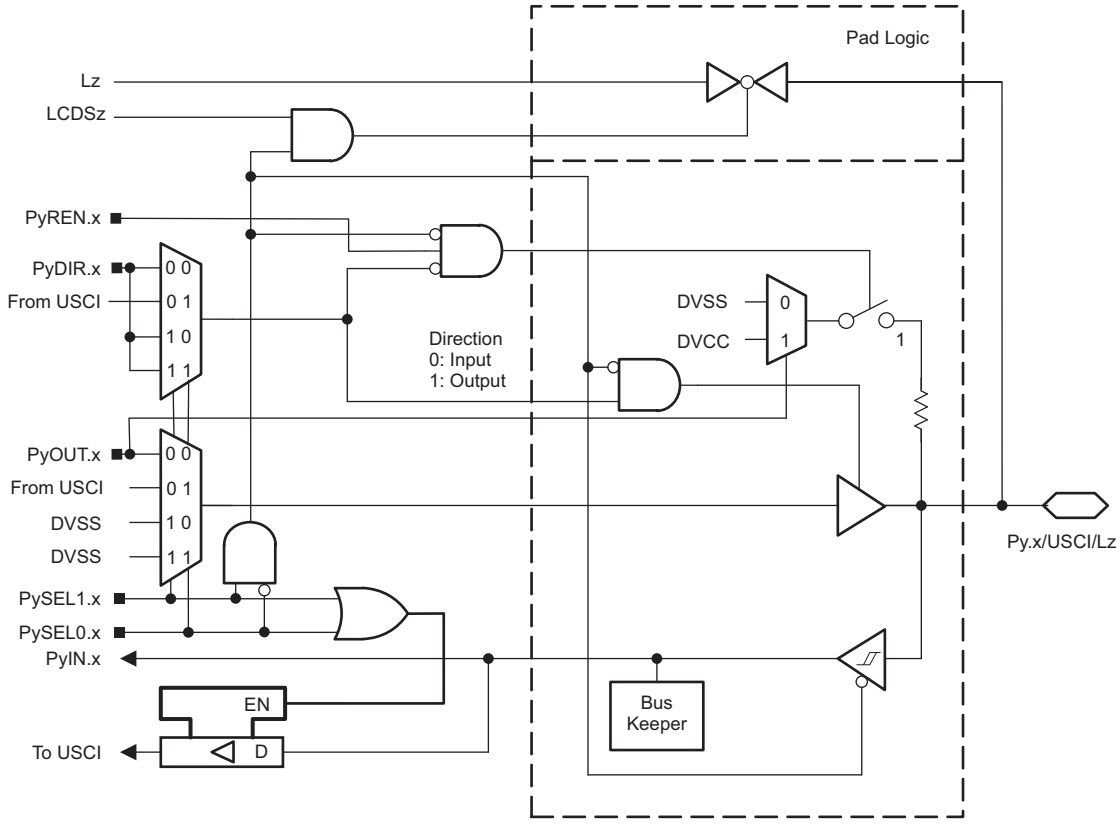
表 6-60. Profile Configuration

Configuration	Details
Active Power Mode Name	Active mode
Active Mode Clock Configuration	CPU: 3 MHz
Active Mode Voltage Integrity	1.62 V

6.12 Input/Output Schematics

6.12.1 Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

图 6-8 shows the port schematic. 表 6-61 lists the settings to select the pin function.



Functional representation only.

图 6-8. Py.x/USCI/Lz Pin Schematic

表 6-61. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA0STE/L19	0	P1.0 (I/O)	I: 0; O: 1	0	0
		UCA0STE	X(2)	0	1
		L19(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.1/UCA0CLK/L18	1	P1.1 (I/O)	I: 0; O: 1	0	0
		UCA0CLK	X(2)	0	1
		L18(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.2/UCA0RXD/UCA0SOMI/L17	2	P1.2 (I/O)	I: 0; O: 1	0	0
		UCA0RXD/UCA0SOMI	X(2)	0	1
		L17(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.3/UCA0TXD/UCA0SIMO/L16	3	P1.3 (I/O)	I: 0; O: 1	0	0
		UCA0TXD/UCA0SIMO	X(2)	0	1
		L16(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.4/UCB0STE/L15	4	P1.4 (I/O)	I: 0; O: 1	0	0
		UCB0STE	X(4)	0	1
		L15(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.5/UCB0CLK/L14	5	P1.5 (I/O)	I: 0; O: 1	0	0
		UCB0CLK	X(4)	0	1
		L14(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.6/UCB0SIMO/UCB0SDA/L13	6	P1.6 (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA	X(4)	0	1
		L13(3)	X	1	0
		N/A	0	1	1
		DVSS	1		
P1.7/UCB0SOMI/UCB0SCL/L12	7	P1.7 (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL	X(4)	0	1
		L12(3)	X	1	0
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Direction controlled by eUSCI_A0 module.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Direction controlled by eUSCI_B0 module.

6.12.2 Port P2, P2.0 to P2.3, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-8

表 6-62 lists the settings to select the pin function.

表 6-62. Port P2 (P2.0 to P2.3) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.0/PM_UCA1STE/L11	0	P2.0 (I/O)	I: 0; O: 1	0	0	X
		UCA1STE	X(2)	0	1	default
		L11(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.1/PM_UCA1CLK/L10	1	P2.1 (I/O)	I: 0; O: 1	0	0	X
		UCA1CLK	X(2)	0	1	default
		L10(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.2/PM_UCA1RXD/PM_UCA1SOMI/L9	2	P2.2 (I/O)	I: 0; O: 1	0	0	X
		UCA1RXD/UCA1SOMI	X(2)	0	1	default
		L9(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.3/PM_UCA1TXD/PM_UCA1SIMO/L8	3	P2.3 (I/O)	I: 0; O: 1	0	0	X
		UCA1TXD/UCA1SIMO	X(2)	0	1	default
		L8(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Direction controlled by eUSCI_A1 module.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12.3 Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-8

表 6-63 lists the settings to select the pin function.

表 6-63. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.0/PM_UCA2STE/L7	0	P3.0 (I/O)	I: 0; O: 1	0	0	X
		UCA2STE	X(2)	0	1	default
		L7(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.1/PM_UCA2CLK/L6	1	P3.1 (I/O)	I: 0; O: 1	0	0	X
		UCA2CLK	X(2)	0	1	default
		L6(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.2/PM_UCA2RXD/PM_UCA2SOMI/L5	2	P3.2 (I/O)	I: 0; O: 1	0	0	X
		UCA2RXD/UCA2SOMI	X(2)	0	1	default
		L5(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.3/PM_UCA2TXD/PM_UCA2SIMO/L4	3	P3.3 (I/O)	I: 0; O: 1	0	0	X
		UCA2TXD/UCA2SIMO	X(2)	0	1	default
		L4(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.4/PM_UCB2STE/L3	4	P3.4 (I/O)	I: 0; O: 1	0	0	X
		UCB2STE	X(4)	0	1	default
		L3(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.5/PM_UCB2CLK/L2	5	P3.5 (I/O)	I: 0; O: 1	0	0	X
		UCB2CLK	X(4)	0	1	default
		L2(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P3.6/PM_UCB2SIMO/PM_UCB2SDA/L1	6	P3.6 (I/O)	I: 0; O: 1	0	0	X
		UCB2SIMO/UCB2SDA	X(4)	0	1	default
		L1(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Direction controlled by eUSCI_A2 module.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Direction controlled by eUSCI_B2 module.

表 6-63. Port P3 (P3.0 to P3.7) Pin Functions (continued)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P3DIR.x	P3SEL1.x	P3SEL0.x	P3MAPx
P3.7/PM_UCB2SOMI/PM_UCB2SCL/L0	7	P3.7 (I/O)	I: 0; O: 1	0	0	X
		UCB2SOMI/UCB2SCL	X(4)	0	1	default
		L0(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

6.12.4 Port P9, P9.4 to P9.7, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-8

表 6-64 lists the settings to select the pin function.

表 6-64. Port P9 (P9.4 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.4/UCA3STE/L43(2)	4	P9.4 (I/O)	I: 0; O: 1	0	0
		UCA3STE	X(3)	0	1
		L43(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P9.5/UCA3CLK/L42(2)	5	P9.5 (I/O)	I: 0; O: 1	0	0
		UCA3CLK	X(3)	0	1
		L42(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P9.6/UCA3RXD/UCA3SOMI/L41(2)	6	P9.6 (I/O)	I: 0; O: 1	0	0
		UCA3RXD/UCA3SOMI	X(3)	0	1
		L41(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P9.7/UCA3TXD/UCA3SIMO/L40(2)	7	P9.7 (I/O)	I: 0; O: 1	0	0
		UCA3TXD/UCA3SIMO	X(3)	0	1
		L40(4)	X	1	0
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Not available on 64-pin RGC package.
(3) Direction controlled by eUSCI_A3 module.
(4) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12.5 Port P10, P10.0 to P10.3, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-8

表 6-65 lists the settings to select the pin function.

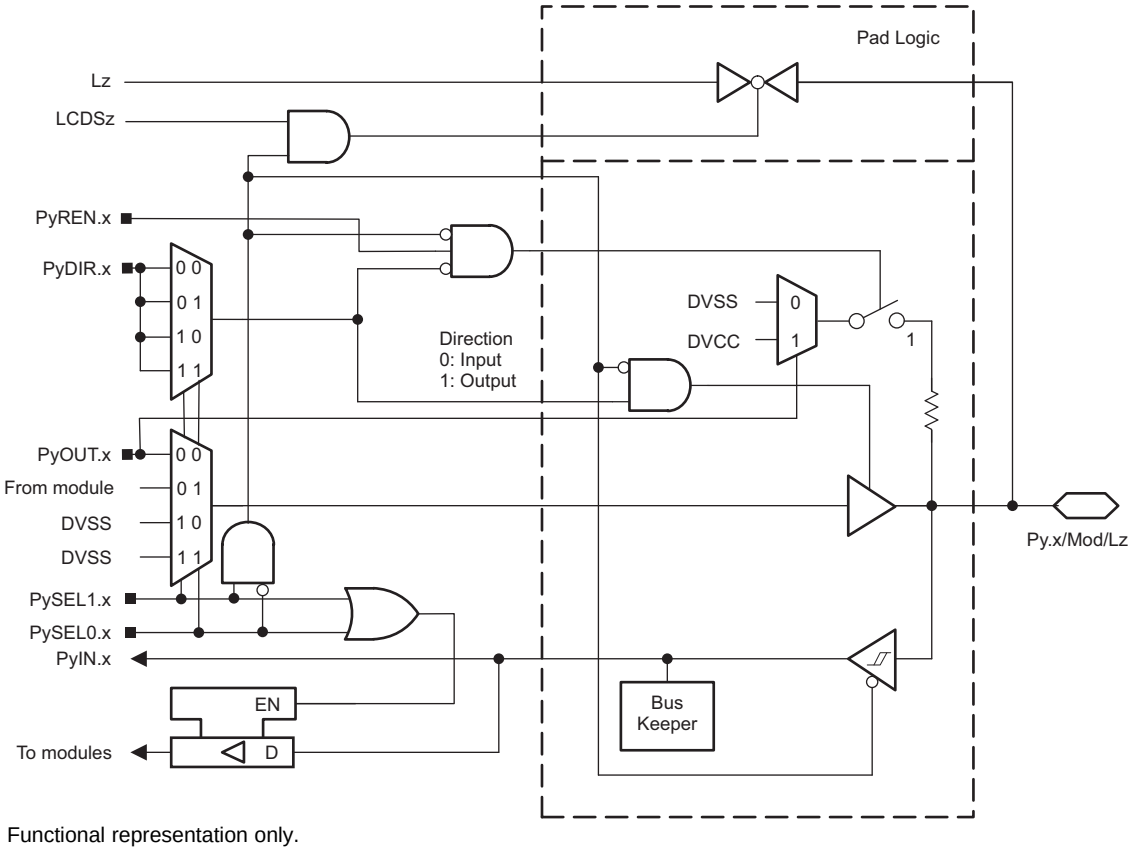
表 6-65. Port P10 (P10.0 to P10.3) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.0/UCB3STE/L39(2)	0	P10.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(3)	0	1
		L39(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P10.1/UCB3CLK/L38(2)	1	P10.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(3)	0	1
		L38(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P10.2/UCB3SIMO/UCB3SDA/L37(2)	2	P10.2 (I/O)	I: 0; O: 1	0	0
		UCB3SIMO/UCB3SDA	X(3)	0	1
		L37(4)	X	1	0
		N/A	0	1	1
		DVSS	1		
P10.3/UCB3SOMI/UCB3SCL/L36(2)	3	P10.3 (I/O)	I: 0; O: 1	0	0
		UCB3SOMI/UCB3SCL	X(3)	0	1
		L36(4)	X	1	0
		N/A	0	1	1
		DVSS	1		

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Direction controlled by eUSCI_B3 module.
(4) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12.6 Port P2, P2.4 to P2.7, Input/Output With Schmitt Trigger

图 6-9 shows the port schematic. 表 6-66 lists the settings to select the pin function.



Functional representation only.

图 6-9. Py.x/Mod/Lz Pin Schematic

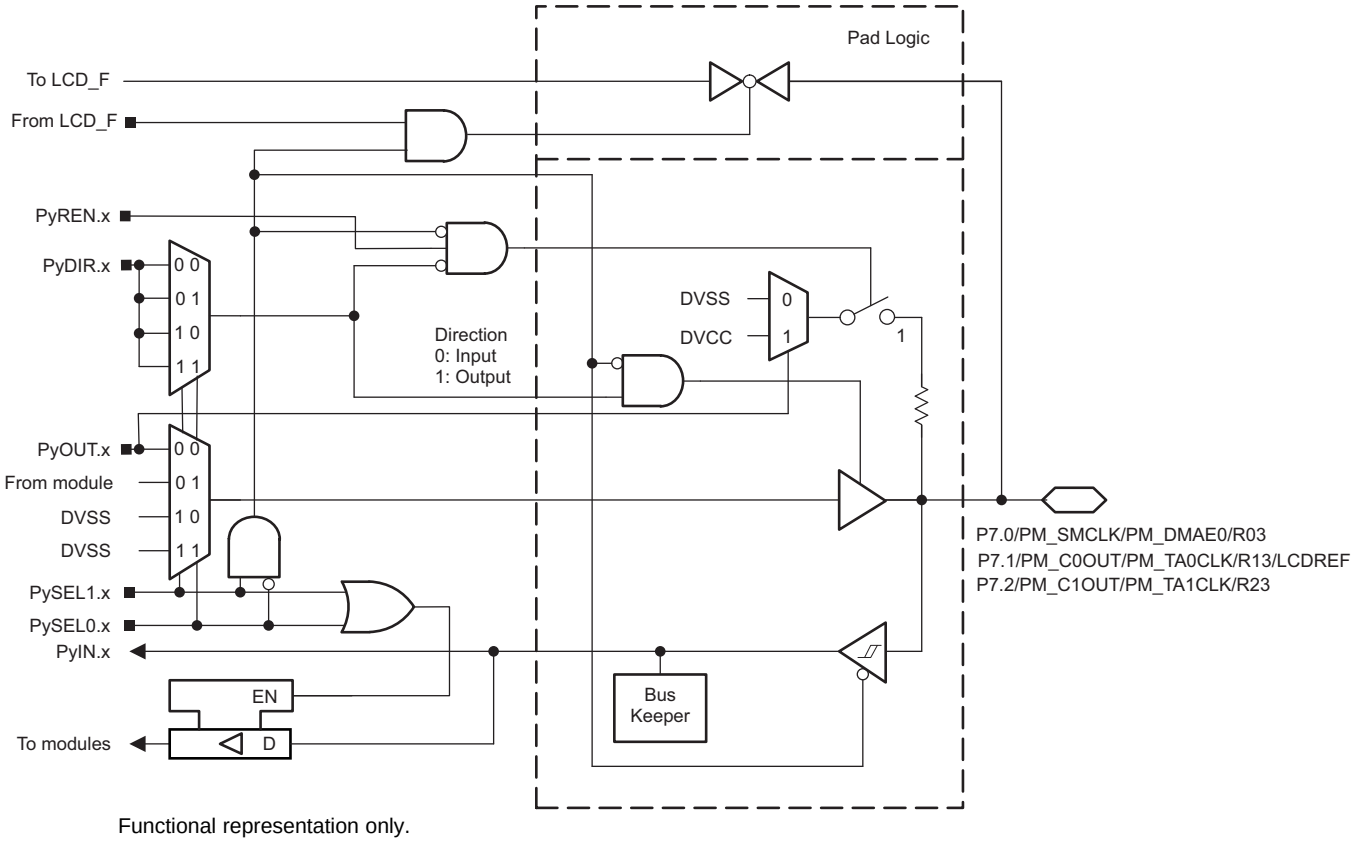
表 6-66. Port P2 (P2.4 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P2DIR.x	P2SEL1.x	P2SEL0.x	P2MAPx
P2.4/PM_TA0.1/L23(2)	4	P2.4 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI1A	0	0	1	default
		TA0.1	1			
		L23(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.5/PM_TA0.2/L22(2)	5	P2.5 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI2A	0	0	1	default
		TA0.2	1			
		L22(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.6/PM_TA0.3/L21(2)	6	P2.6 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI3A	0	0	1	default
		TA0.3	1			
		L21(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P2.7/PM_TA0.4/L20(2)	7	P2.7 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI4A	0	0	1	default
		TA0.4	1			
		L20(3)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12.7 Port P7, P7.0 to P7.2, Input/Output With Schmitt Trigger

图 6-10 shows the port schematic. 表 6-67 lists the settings to select the pin function.



Functional representation only.

图 6-10. P7.0, P7.1 and P7.2 Pin Schematic

表 6-67. Port P7 (P7.0 to P7.2) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.0/PM_SMCLK/ PM_DMAE0 R03	0	P7.0 (I/O)	I: 0; O: 1	0	0	X
		DMAE0	0	0	1	default
		SMCLK	1			
		R03(2)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			
P7.1/PM_C0OUT/ PM_TA0CLK R13/LCDREF	1	P7.1 (I/O)	I: 0; O: 1	0	0	X
		TA0CLK	0	0	1	default
		C0OUT	1			
		R13(2)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care
(2) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

表 6-67. Port P7 (P7.0 to P7.2) Pin Functions (continued)

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.2/PM_C1OUT/ PM_TA1CLK R23	2	P7.2 (I/O)	I: 0; O: 1	0	0	X
		TA1CLK	0	0	1	default
		C1OUT	1			
		R23(2)	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

6.12.8 Port P7, P7.3, Input/Output With Schmitt Trigger

图 6-11 shows the port schematic. 表 6-68 lists the settings to select the pin function.

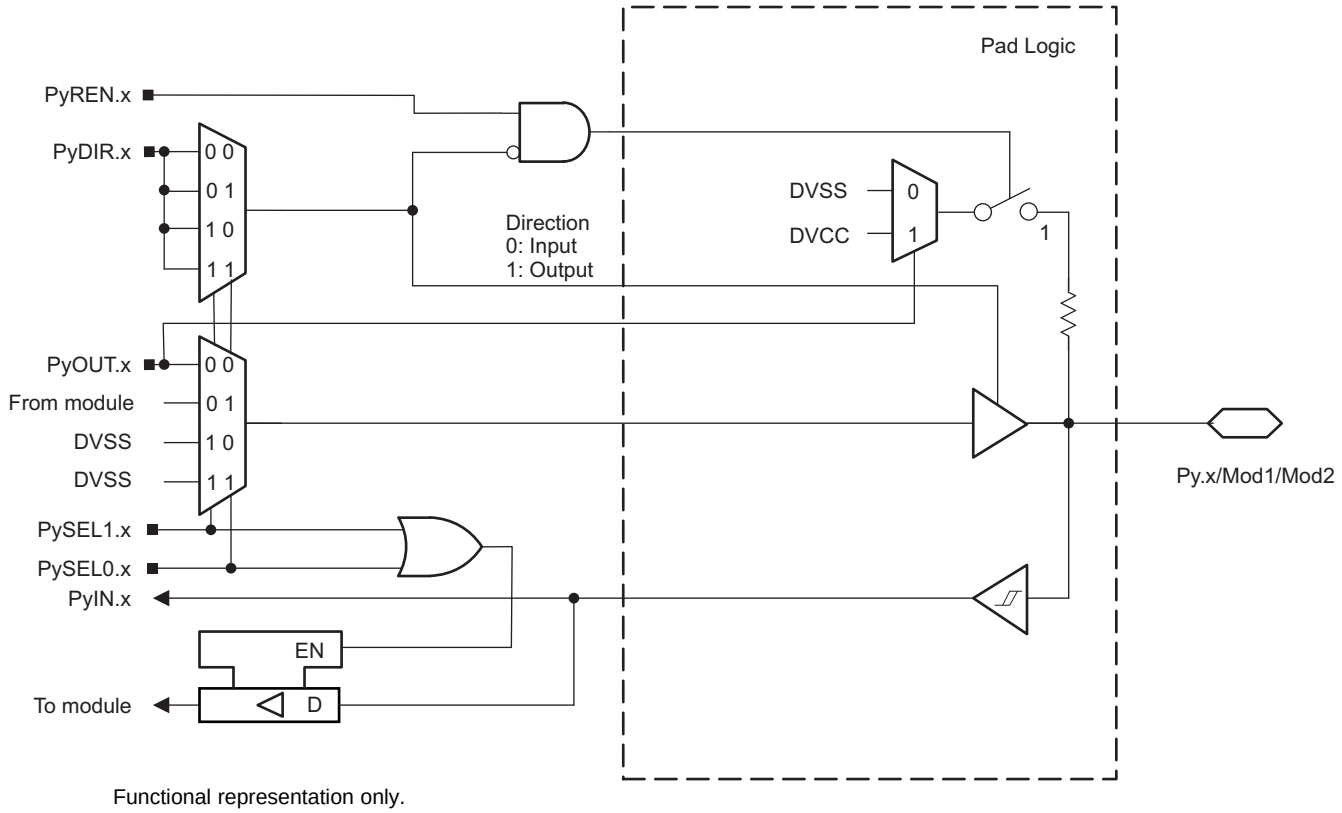


图 6-11. P7.3 Pin Schematic

表 6-68. Port P7 (P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.3/PM_TA0.0	3	P7.3 (I/O)	I: 0; O: 1	0	0	X
		TA0.CCI0A	0	0	1	default
		TA0.0	1			
		N/A	X	1	0	X
		N/A	0	1	1	X
		DVSS	1			

(1) X = Don't care

6.12.9 Port P9, P9.2 and P9.3, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-9

表 6-69 lists the settings to select the pin function.

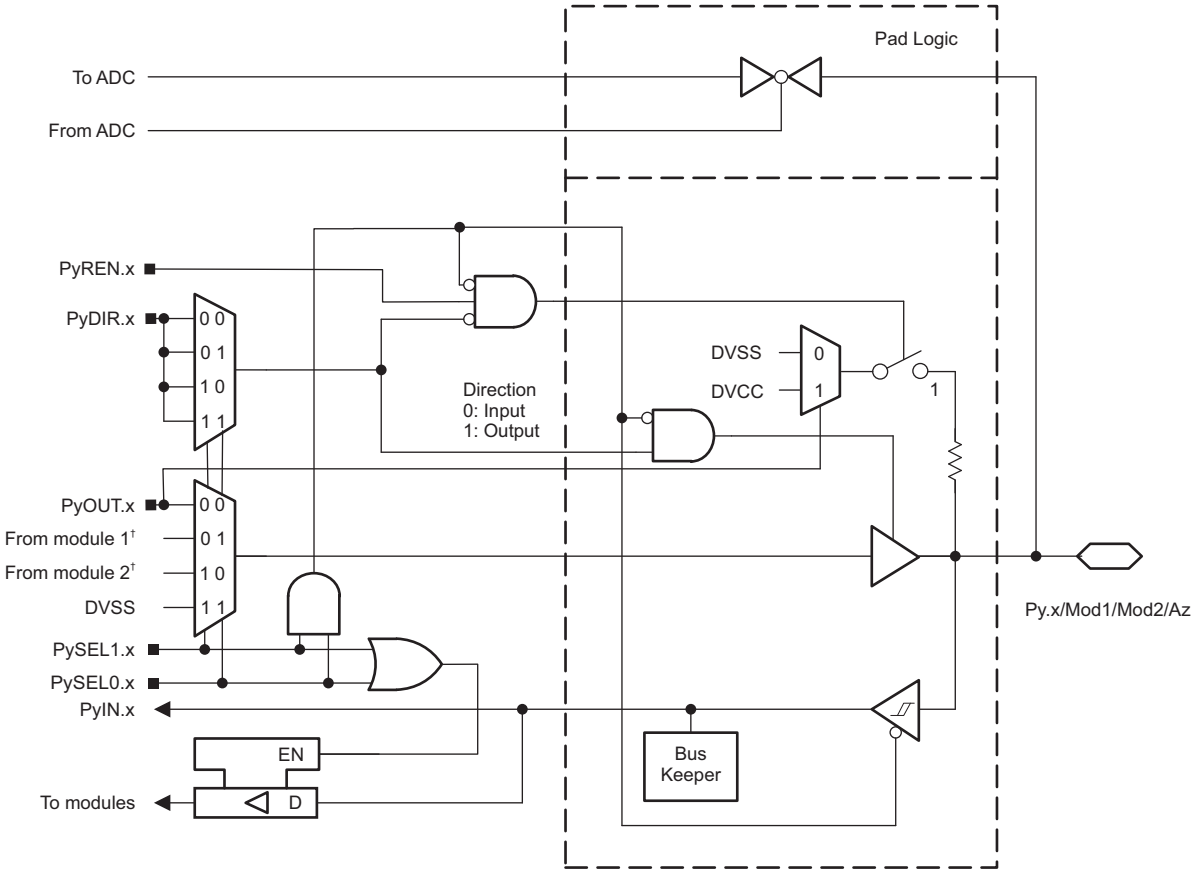
表 6-69. Port P9 (P9.2 and P9.3) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.2/TA3.3/L33(1)	2	P9.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI3A	0	0	1
		TA3.3	1		
		L33(2)	X	1	0
		N/A	0	1	1
		DVSS	1		
P9.3/TA3.4/L32(1)	3	P9.3 (I/O)	I: 0; O: 1	0	0
		TA3.CCI4A	0	0	1
		TA3.4	1		
		L32(2)	X	1	0
		N/A	0	1	1
		DVSS	1		

(1) Not available on 64-pin RGC package.
(2) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.12.10 Port P4, P4.2 to P4.7, Input/Output With Schmitt Trigger

图 6-12 shows the port schematic. 表 6-70 lists the settings to select the pin function.



† Output is DVSS if module 1 or module 2 function is not available. See the pin function tables.

Functional representation only.

图 6-12. Py.x/Mod1/Mod2/Az Pin Schematic

表 6-70. Port P4 (P4.2 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.2/ACLK/TA2CLK/A11	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		ACLK	1		
		TA2CLK	0	1	0
		DVSS	1		
		A11(2)	X	1	1
P4.3/MCLK/RTCCLK/A10	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		MCLK	1		
		N/A	0	1	0
		RTCCLK	1		
		A10(2)	X	1	1
P4.4/HSMCLK/SVMHOUT/A9	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		HSMCLK	1		
		N/A	0	1	0
		SVMHOUT	1		
		A9(2)	X	1	1
P4.5/A8	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A8(2)	X	1	1
P4.6/A7	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A7(2)	X	1	1
P4.7/A6	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A6(2)	X	1	1

(1) X = Don't care
(2) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.12.11 Port P5, P5.0 to P5.5, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-12

表 6-71 lists the settings to select the pin function.

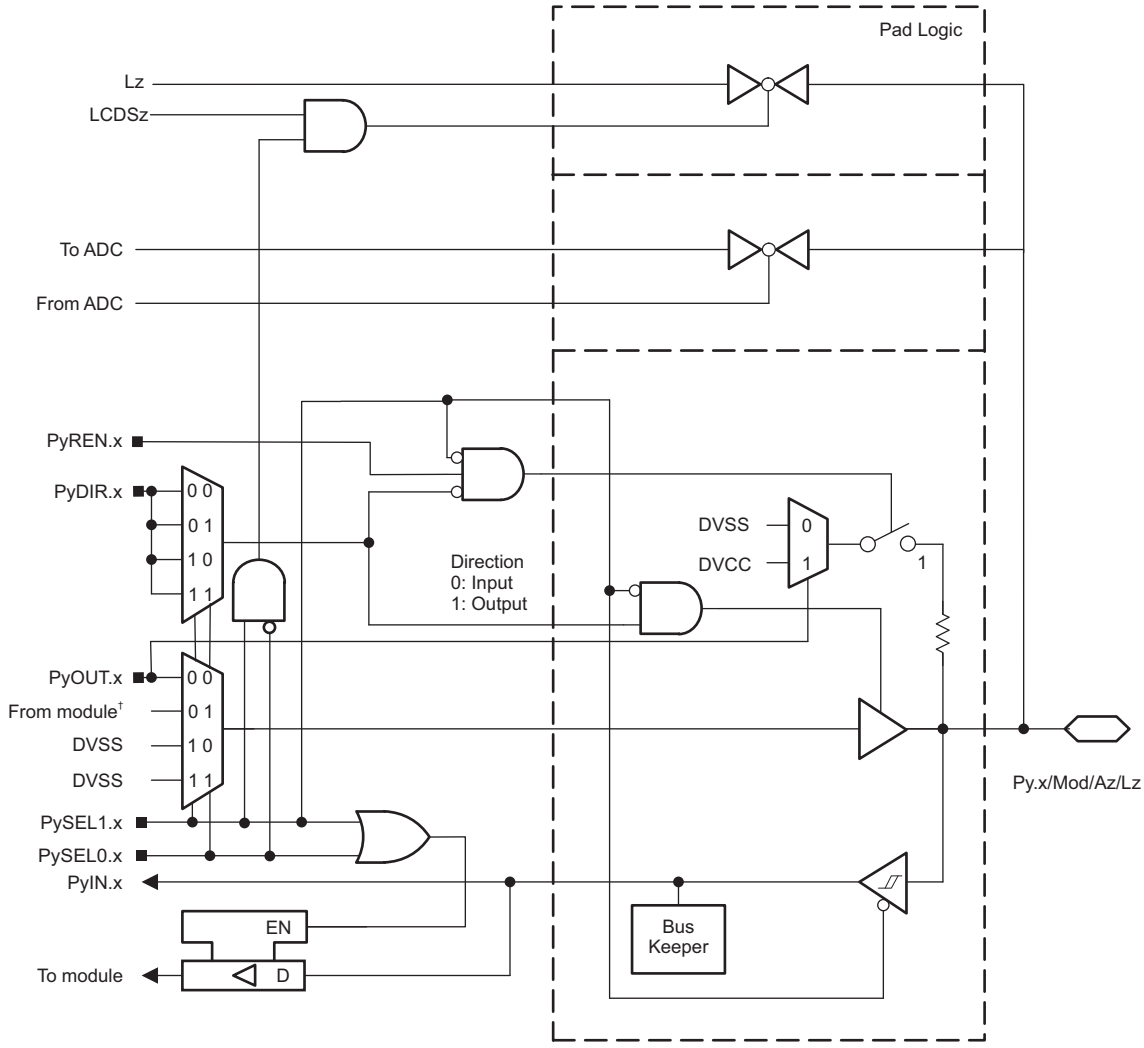
表 6-71. Port P5 (P5.0 to P5.5) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.0/A5	0	P5.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A5(2)	X	1	1
P5.1/A4	1	P5.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A4(2)	X	1	1
P5.2/A3	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A3(2)	X	1	1
P5.3/A2	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A2(2)	X	1	1
P5.4/A1	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A1(2)	X	1	1
P5.5/A0	5	P5.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		N/A	0	1	0
		DVSS	1		
		A0(2)	X	1	1

(1) X = Don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

6.12.12 Port P4, P4.0 to P4.1, Input/Output With Schmitt Trigger

图 6-13 shows the port schematic. 表 6-72 lists the settings to select the pin function.



† Output is DVSS if module function is not available. See the pin function tables.
Functional representation only.

图 6-13. Py.x/Mod/Az/Lz Pin Schematic

表 6-72. Port P4 (P4.0 to P4.1) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P4DIR.x	P4SEL1.x	P4SEL0.x
P4.0/A13/L13(2)	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L13(3)	X	1	0
		A13(4)	X	1	1
P4.1/A12/L12(2)	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L12(3)	X	1	0
		A12(4)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P4SEL1.x and P4SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

注

On pins with ADC and LCD multiplexing, make sure that only one of these functions is enabled at any time.

6.12.13 Port P6, P6.0 and P6.1, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-13

表 6-73 lists the settings to select the pin function.

表 6-73. Port P6 (P6.0 and P6.1) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.0/A15/L15(2)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L15(3)	X	1	0
		A15(4)	X	1	1
P6.1/A14/L14(2)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L14(3)	X	1	0
		A14(4)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

注

On pins with ADC and LCD multiplexing, make sure that only one of these functions is enabled at any time.

6.12.14 Port P8, P8.2 to P8.7, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-13

表 6-74 lists the settings to select the pin function.

表 6-74. Port P8 (P8.2 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.2/TA3.2/A23/L47(2)	2	P8.2 (I/O)	I: 0; O: 1	0	0
		TA3.CCI2A	0	0	1
		TA3.2	1		
		L47(3)	X	1	0
		A23(4)	X	1	1
P8.3/TA3CLK/A22/L46(2)	3	P8.3 (I/O)	I: 0; O: 1	0	0
		TA3CLK	0	0	1
		DVSS	1		
		L46(3)	X	1	0
		A22(4)	X	1	1
P8.4/A21/L45(2)	4	P8.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L45(3)	X	1	0
		A21(4)	X	1	1
P8.5/A20/L44(2)	5	P8.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L44(3)	X	1	0
		A20(4)	X	1	1
P8.6/A19/L19(2)	6	P8.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L19(3)	X	1	0
		A19(4)	X	1	1
P8.7/A18/L18(2)	7	P8.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L18(3)	X	1	0
		A18(4)	X	1	1

(1) X = Don't care
(2) Not available on 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

注

On pins with ADC and LCD multiplexing, make sure that only one of these functions is enabled at any time.

6.12.15 Port P9, P9.0 and P9.1, Input/Output With Schmitt Trigger

Pin schematic: see 图 6-13

表 6-75 lists the settings to select the pin function.

表 6-75. Port P9 (P9.0 and P9.1) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P9DIR.x	P9SEL1.x	P9SEL0.x
P9.0/A17/L17(2)	0	P9.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L17(3)	X	1	0
		A17(4)	X	1	1
P9.1/A16/L16(2)	1	P9.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	0	1
		DVSS	1		
		L16(3)	X	1	0
		A16(4)	X	1	1

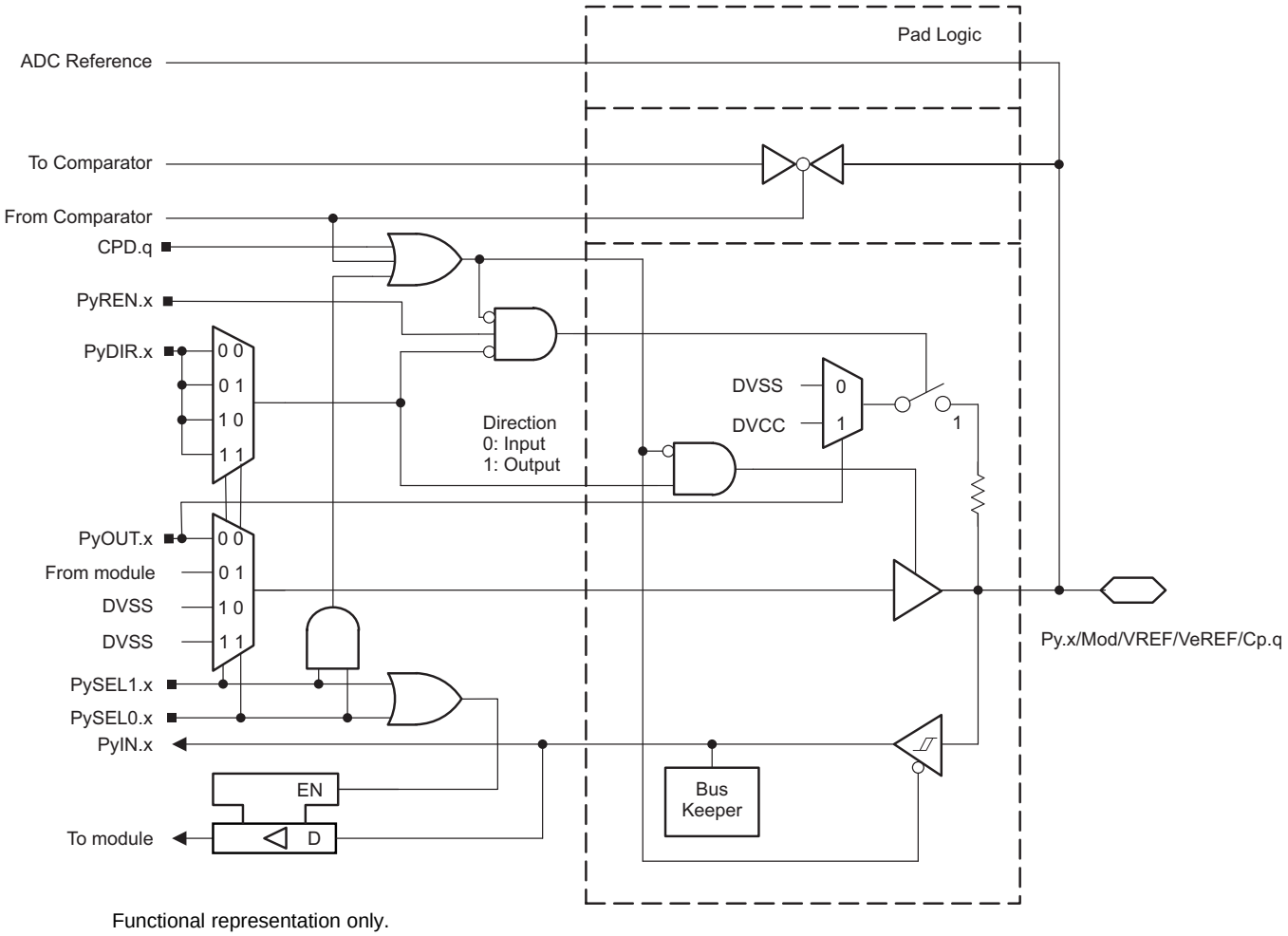
(1) X = Don't care
(2) Not available on 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P9SEL1.x and P9SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

注

On pins with ADC and LCD multiplexing, make sure that only one of these functions is enabled at any time.

6.12.16 Port P5, P5.6 and P5.7, Input/Output With Schmitt Trigger

图 6-14 shows the port schematic. 表 6-76 lists the settings to select the pin function.



Functional representation only.

图 6-14. Py.x/Mod/VREF/VeREF/Cp.q Pin Schematic

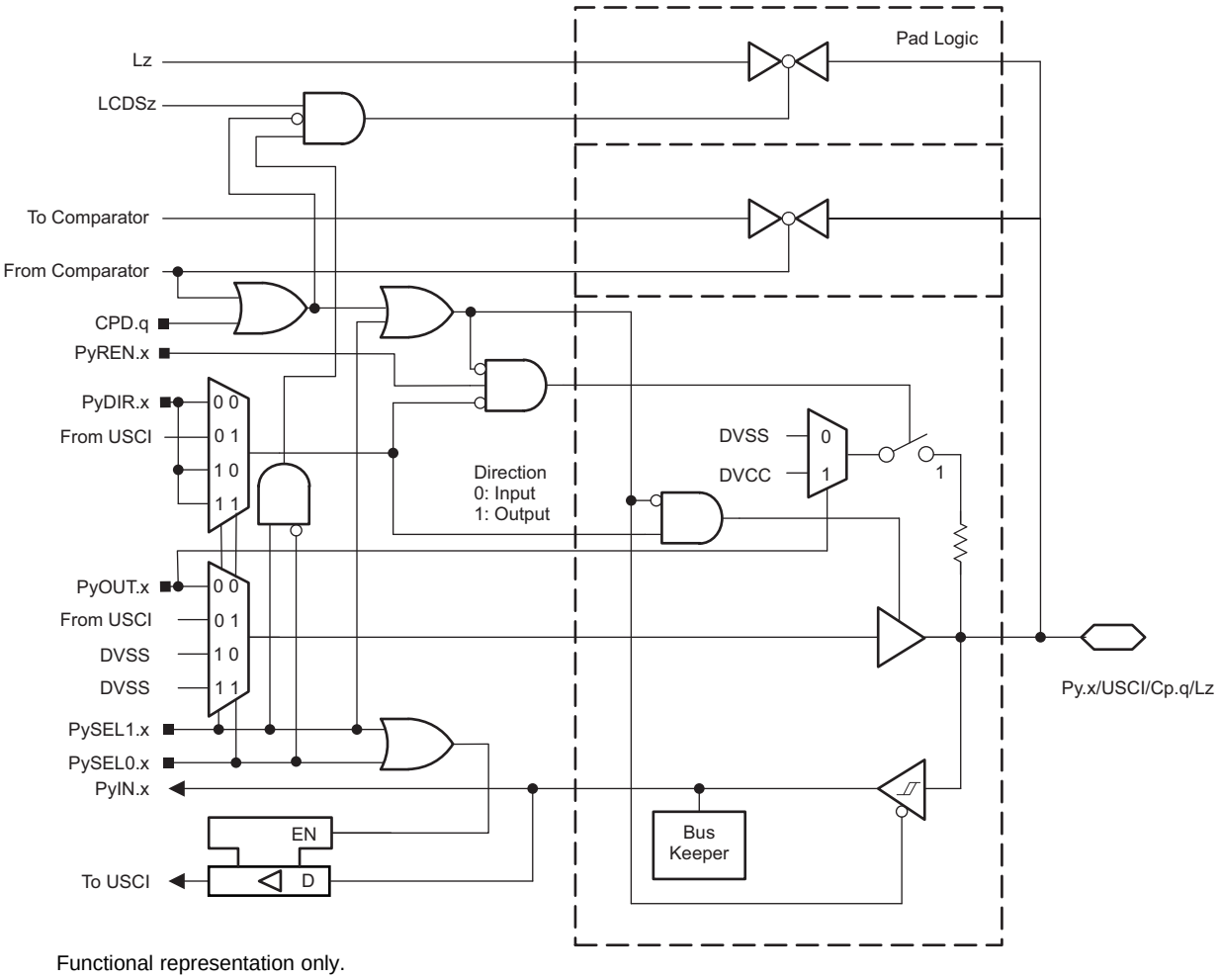
表 6-76. Port P5 (P5.6 and P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL1.x	P5SEL0.x
P5.6/TA2.1/VREF+/VeREF+/C1.7	6	P5.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI1A	0	0	1
		TA2.1	1		
		N/A	0	1	0
		DVSS	1		
		VREF+, VeREF+, C1.7(2)(3)	X	1	1
P5.7/TA2.2/VREF-/VeREF-/C1.6	7	P5.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI2A	0	0	1
		TA2.2	1		
		N/A	0	1	0
		DVSS	1		
		VREF-, VeREF-, C1.6(2)(3)	X	1	1

(1) X = Don't care
(2) Setting P5SEL1.x and P5SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

6.12.17 Port P6, P6.2 to P6.5, Input/Output With Schmitt Trigger

图 6-15 shows the port schematic. 表 6-77 lists the settings to select the pin function.



Functional representation only.

图 6-15. Py.x/USCI/Cp.q Pin Schematic

表 6-77. Port P6 (P6.2 to P6.5) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.2/UCB1STE/C1.5/L27(2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		UCB1STE	X(3)	0	1
		L27(4)	X	1	0
		C1.5(5)(6)	X	1	1
P6.3/UCB1CLK/C1.4/L26(2)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		UCB1CLK	X(3)	0	1
		L26(4)	X	1	0
		C1.4(5)(6)	X	1	1
P6.4/UCB1SIMO/UCB1SDA/C1.3/L25(2)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		UCB1SIMO/UCB1SDA	X(3)	0	1
		L25(4)	X	1	0
		C1.3(5)(6)	X	1	1
P6.5/UCB1SOMI/UCB1SCL/C1.2/L24(2)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		UCB1SOMI/UCB1SCL	X(3)	0	1
		L24(4)	X	1	0
		C1.2(5)(6)	X	1	1

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Direction controlled by eUSCI_B1 module.
(4) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(5) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(6) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

6.12.18 Port P6, P6.6 and P6.7, Input/Output With Schmitt Trigger

图 6-16 shows the port schematic. 表 6-78 lists the settings to select the pin function.

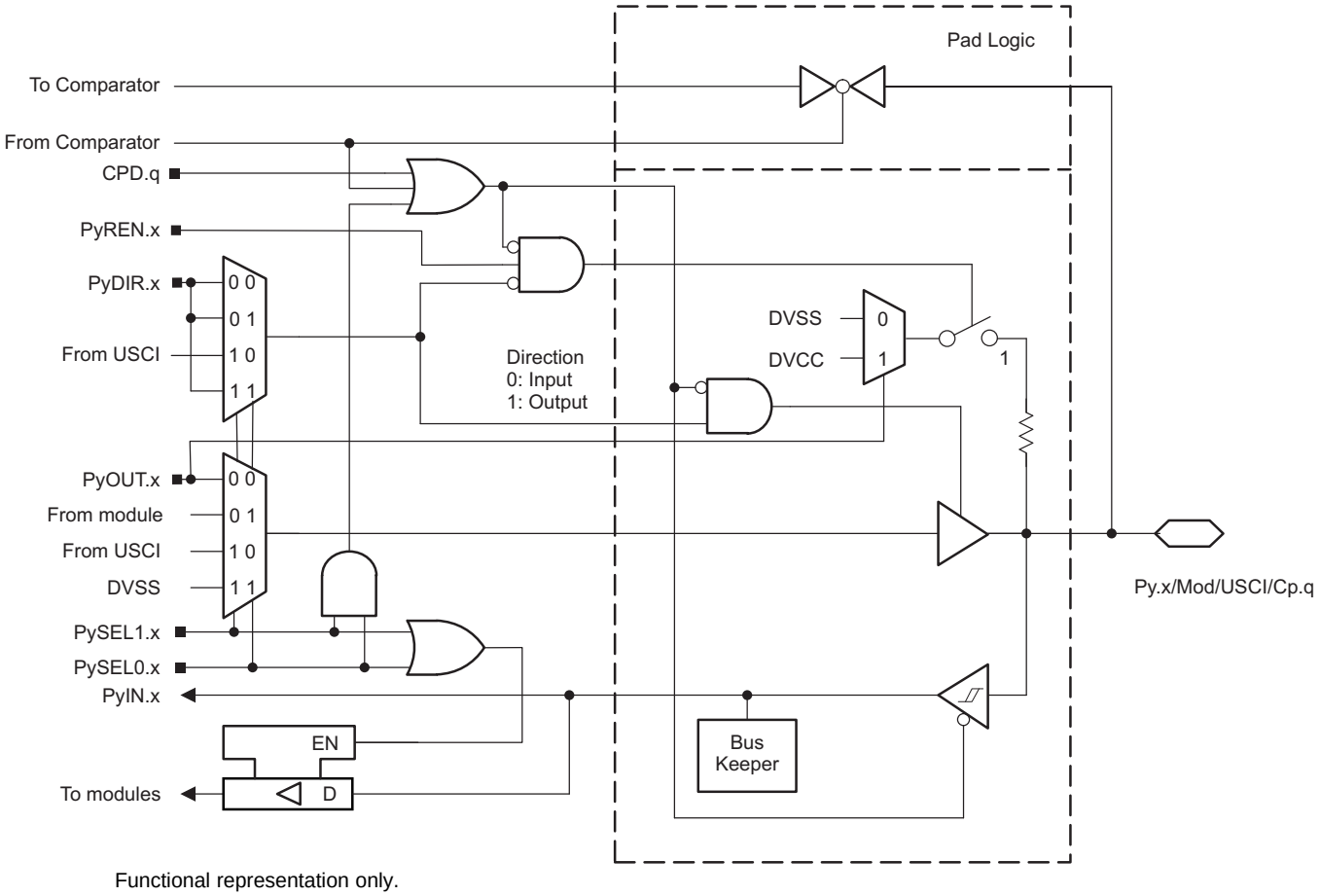


图 6-16. Py.x/Mod/USCI/Cp.q Pin Schematic

表 6-78. Port P6 (P6.6 and P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P6DIR.x	P6SEL1.x	P6SEL0.x
P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1	6	P6.6 (I/O)	I: 0; O: 1	0	0
		TA2.CCI3A	0	0	1
		TA2.3	1		
		UCB3SIMO/UCB3SDA	X(2)	1	0
		C1.1(3)(4)	X	1	1
P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0	7	P6.7 (I/O)	I: 0; O: 1	0	0
		TA2.CCI4A	0	0	1
		TA2.4	1		
		UCB3SOMI/UCB3SCL	X(2)	1	0
		C1.0(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P6SEL1.x and P6SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C1.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

6.12.19 Port P8, P8.0 and P8.1, Input/Output With Schmitt Trigger

图 6-17 shows the port schematic. 表 6-79 lists the settings to select the pin function.

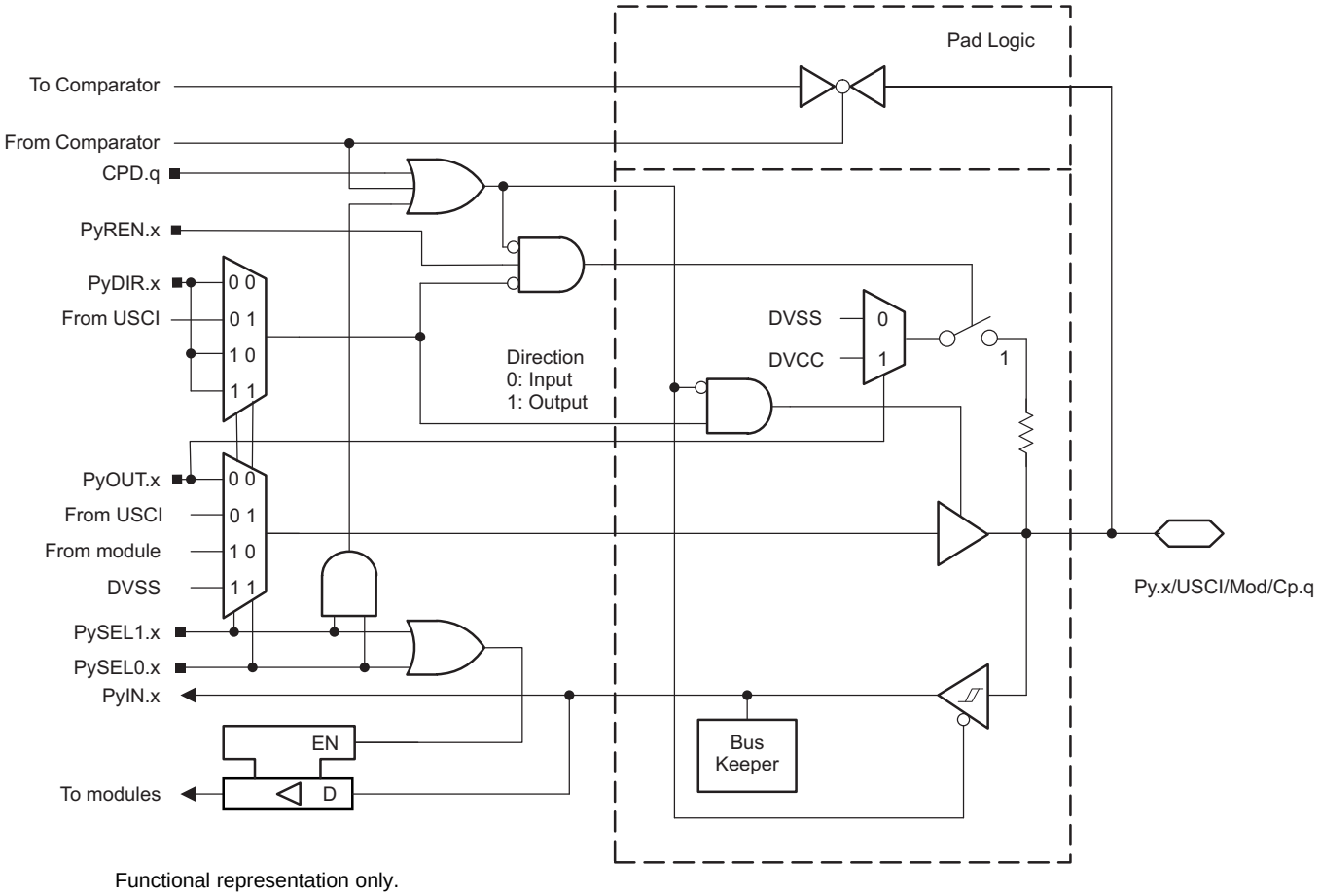


图 6-17. Py.x/USCI/Mod/Cp.q Pin Schematic

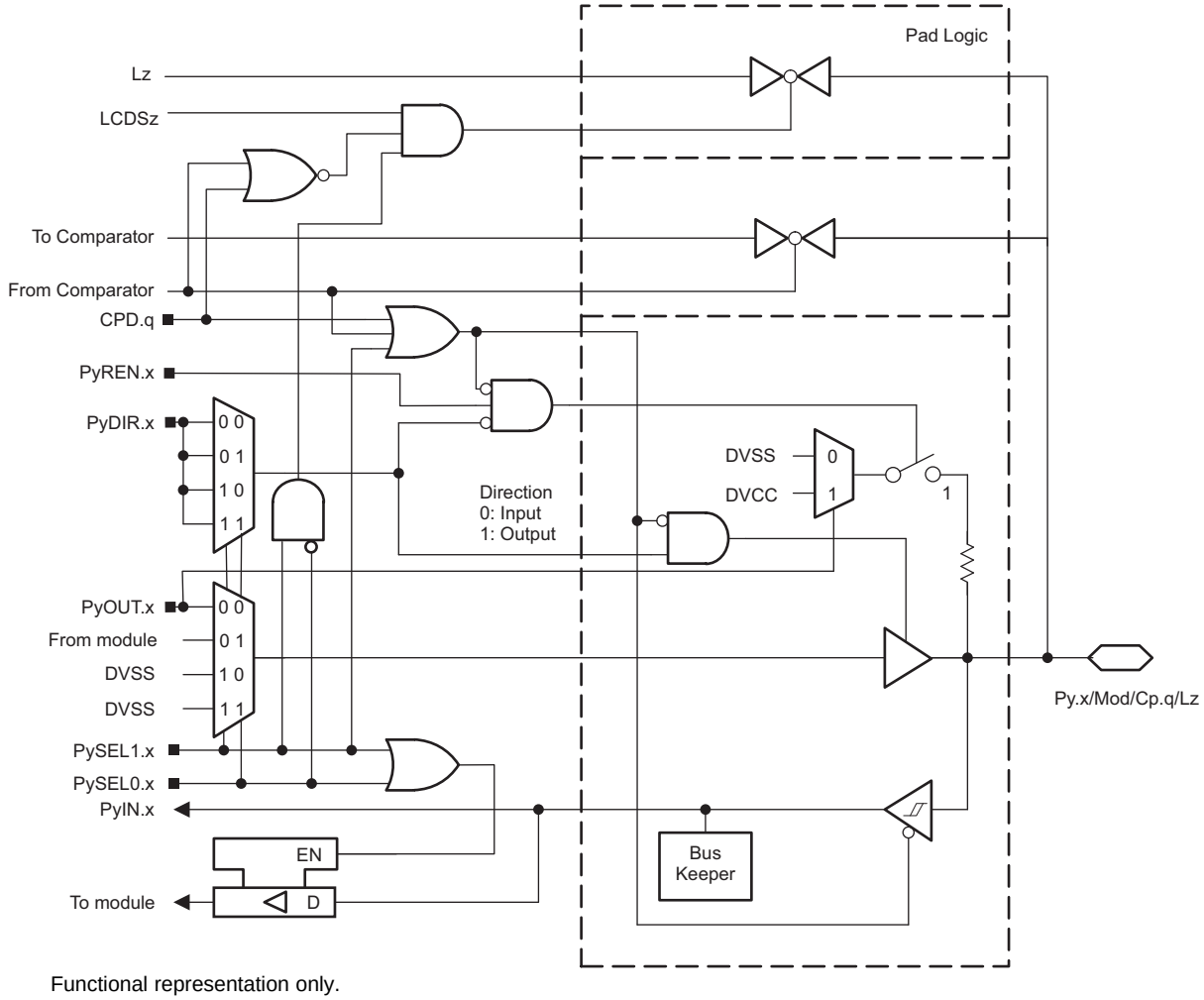
表 6-79. Port P8 (P8.0 and P8.1) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P8DIR.x	P8SEL1.x	P8SEL0.x
P8.0/UCB3STE/TA1.0/C0.1	0	P8.0 (I/O)	I: 0; O: 1	0	0
		UCB3STE	X(2)	0	1
		TA1.CCI0A	0	1	0
		TA1.0	1		
		C0.1(3)(4)	X	1	1
P8.1/UCB3CLK/TA2.0/C0.0	1	P8.1 (I/O)	I: 0; O: 1	0	0
		UCB3CLK	X(2)	0	1
		TA2.CCI0A	0	1	0
		TA2.0	1		
		C0.0(3)(4)	X	1	1

(1) X = Don't care
(2) Direction controlled by eUSCI_B3 module.
(3) Setting P8SEL1.x and P8SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(4) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

6.12.20 Port P10, P10.4 and P10.5, Input/Output With Schmitt Trigger

图 6-18 shows the port schematic. 表 6-80 lists the settings to select the pin function.



Functional representation only.

图 6-18. Py.x/Mod/Cp.q/Lz Pin Schematic

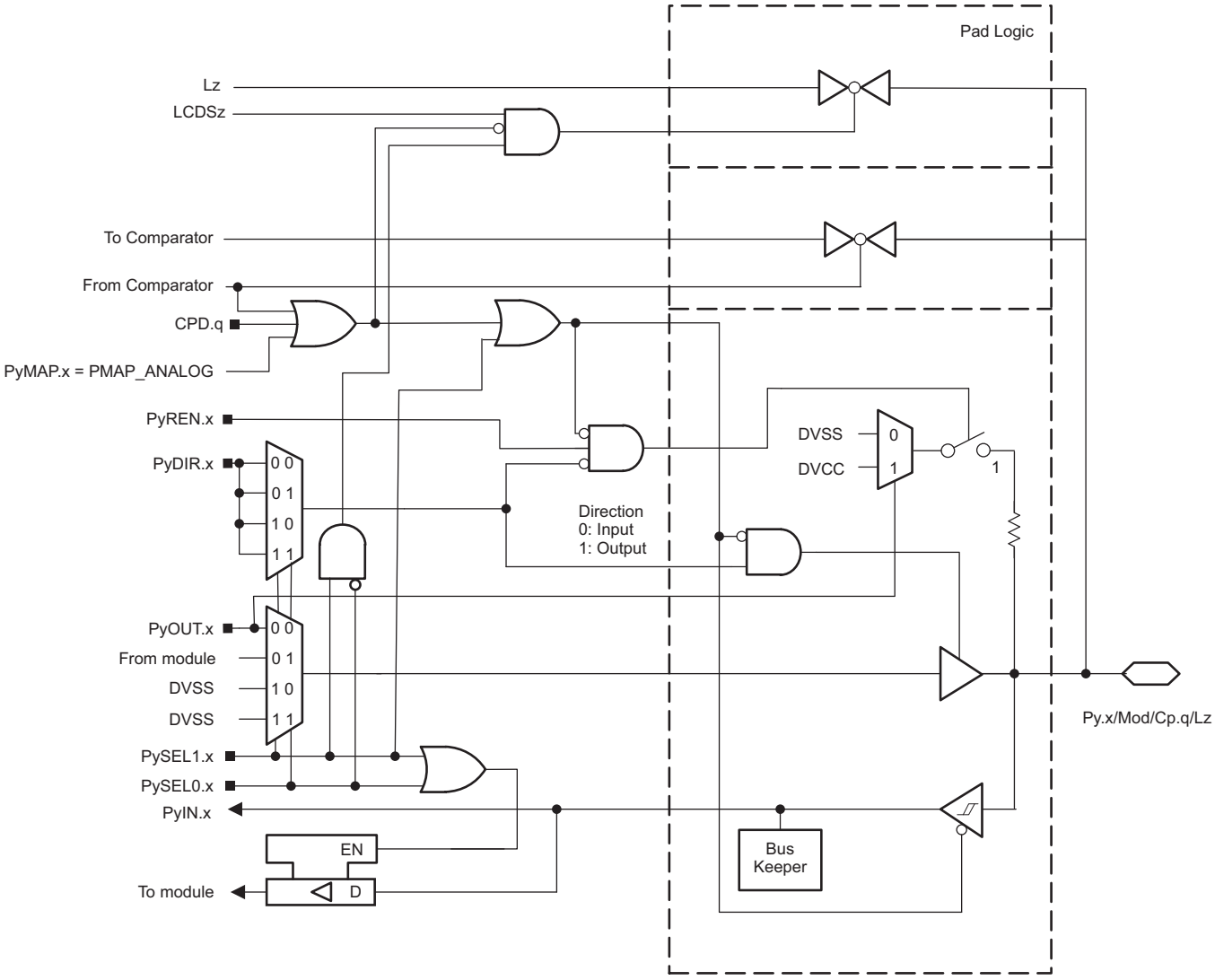
表 6-80. Port P10 (P10.4 and P10.5) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P10DIR.x	P10SEL1.x	P10SEL0.x
P10.4/TA3.0/C0.7/L35(2)	4	P10.4 (I/O)	I: 0; O: 1	0	0
		TA3.CCI0A	0	0	1
		TA3.0	1		
		L35(3)	X	1	0
		C0.7(4)(5)	X	1	1
P10.5/TA3.1/C0.6/L34(2)	5	P10.5 (I/O)	I: 0; O: 1	0	0
		TA3.CCI1A	0	0	1
		TA3.1	1		
		L34(3)	X	1	0
		C0.6(4)(5)	X	1	1

(1) X = Don't care
(2) Not available on 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P10SEL1.x and P10SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.

6.12.21 Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger

图 6-19 shows the port schematic. 表 6-81 lists the settings to select the pin function.



Functional representation only.

图 6-19. Py.x/Mod/Cp.q/Lz Pin Schematic

表 6-81. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P7DIR.x	P7SEL1.x	P7SEL0.x	P7MAPx
P7.4/PM_TA1.4/C0.5/L31(2)	4	P7.4 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI4A	0	0	1	default
		TA1.4	1			
		L31(3)	X	1	0	X
		C0.5(4)(5)(6)	X	1	1	X
P7.5/PM_TA1.3/C0.4/L30(2)	5	P7.5 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI3A	0	0	1	default
		TA1.3	1			
		L30(3)	X	1	0	X
		C0.4(4)(5)(6)	X	1	1	X
P7.6/PM_TA1.2/C0.3/L29(2)	6	P7.6 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI2A	0	0	1	default
		TA1.2	1			
		L29(3)	X	1	0	X
		C0.3(4)(5)(6)	X	1	1	X
P7.7/PM_TA1.1/C0.2/L28(2)	7	P7.7 (I/O)	I: 0; O: 1	0	0	X
		TA1.CCI1A	0	0	1	default
		TA1.1	1			
		L28(3)	X	1	0	X
		C0.2(4)(5)(6)	X	1	1	X

(1) X = Don't care
(2) Not available on the 64-pin RGC package.
(3) Setting the PSEL1.x and PSEL0.x bits to 10 disables both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.
(4) Setting P7SEL1.x and P7SEL0.x disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) Setting the CEPD.q bit of the comparator disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the C0.q input pin to the comparator multiplexer with the CEIPSEL or CEIMSEL bits automatically disables the output driver and input buffer for that pin, regardless of the state of the associated CEPD.q bit.
(6) Setting P7MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger independent of P7SEL1.x and P7SEL0.x settings.

6.12.22 Port PJ, PJ.0 and PJ.1 Input/Output With Schmitt Trigger

图 6-20 and 图 6-21 show the port schematics. 表 6-82 lists the settings to select the pin function.

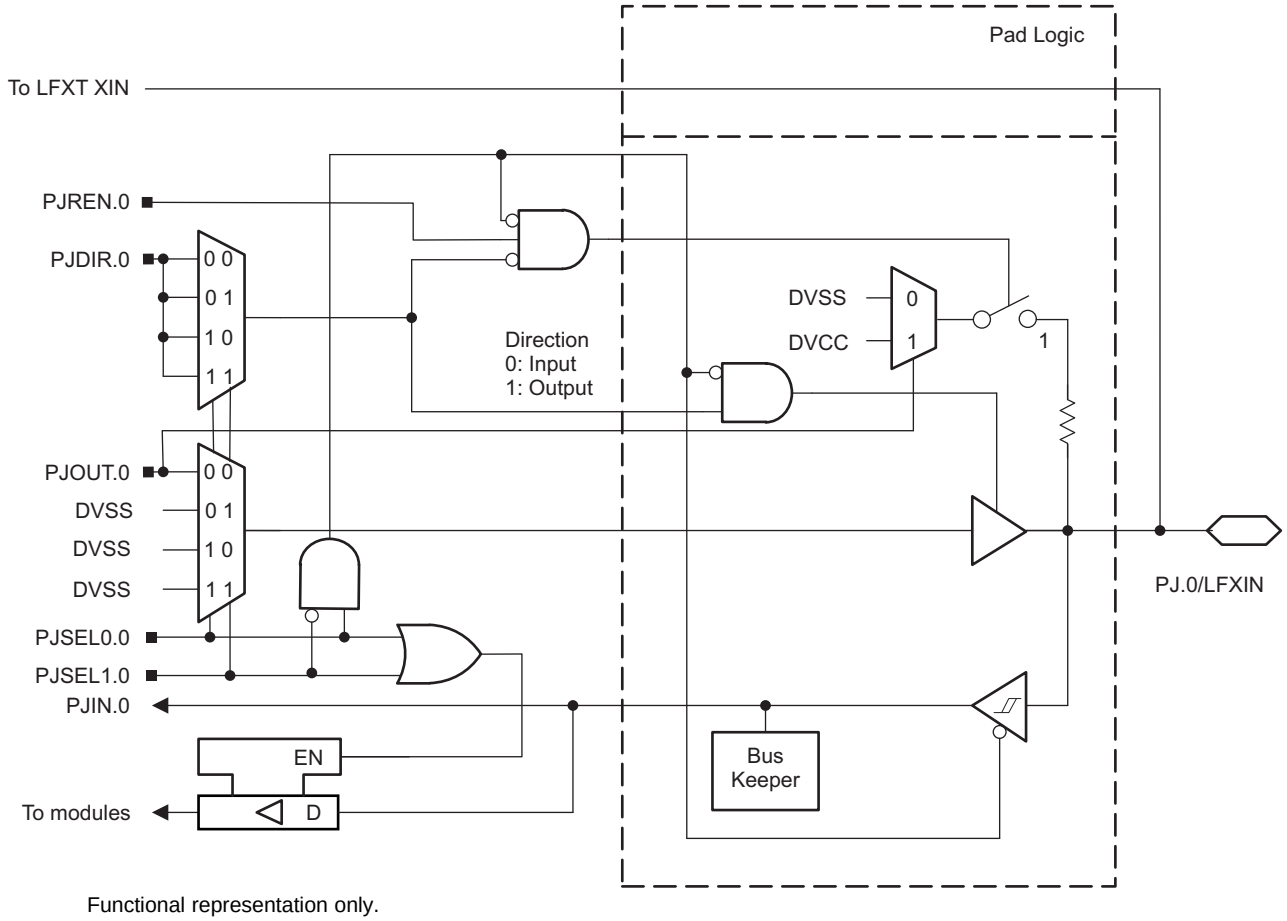
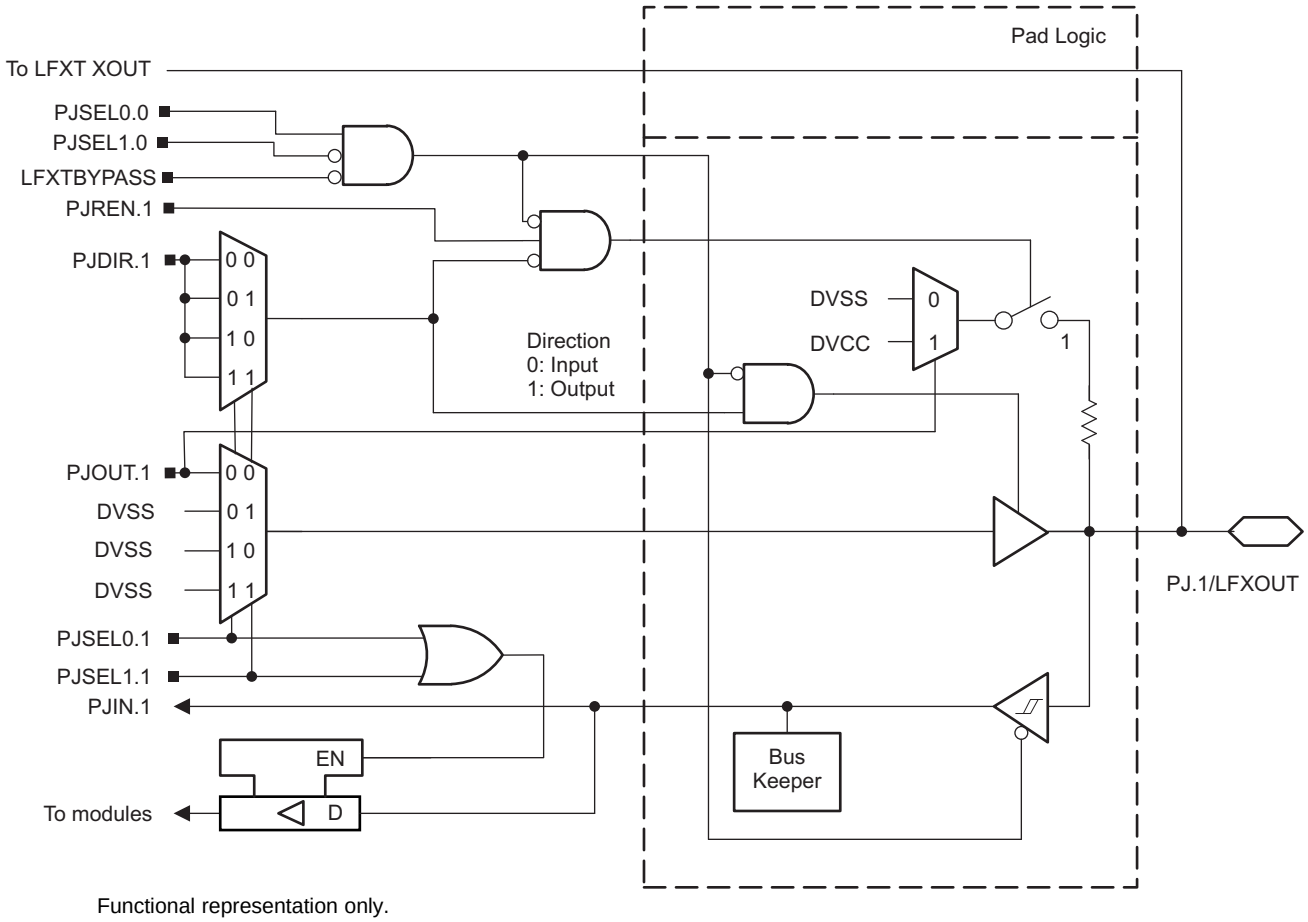


图 6-20. Port PJ (PJ.0) Schematic



Functional representation only.

图 6-21. Port PJ (PJ.1) Schematic

表 6-82. Port PJ (PJ.0 and PJ.1) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.1	PJSEL0.1	PJSEL1.0	PJSEL0.0	LFXT BYPASS
PJ.0/LFXIN	0	PJ.0 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		LFXIN crystal mode (2)	X	X	X	0	1	0
		LFXIN bypass mode (2)	X	X	X	0	1	1
PJ.1/LFXOUT	1	PJ.1 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		LFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.0 = 0 and PJSEL0.0 = 1 causes the general-purpose I/O to be disabled. When LFXTBYPASS = 0, PJ.0 and PJ.1 are configured for crystal operation and PJSEL1.1 and PJSEL0.1 are do not care. When LFXTBYPASS = 1, PJ.0 is configured for bypass operation and PJ.1 is configured as general-purpose I/O.
(3) When PJ.0 is configured in bypass mode, PJ.1 is configured as general-purpose I/O.
(4) With PJSEL0.1 = 1 or PJSEL1.1 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

6.12.23 Port PJ, PJ.2 and PJ.3 Input/Output With Schmitt Trigger

图 6-22 and 图 6-23 show the port schematics. 表 6-83 lists the settings to select the pin function.

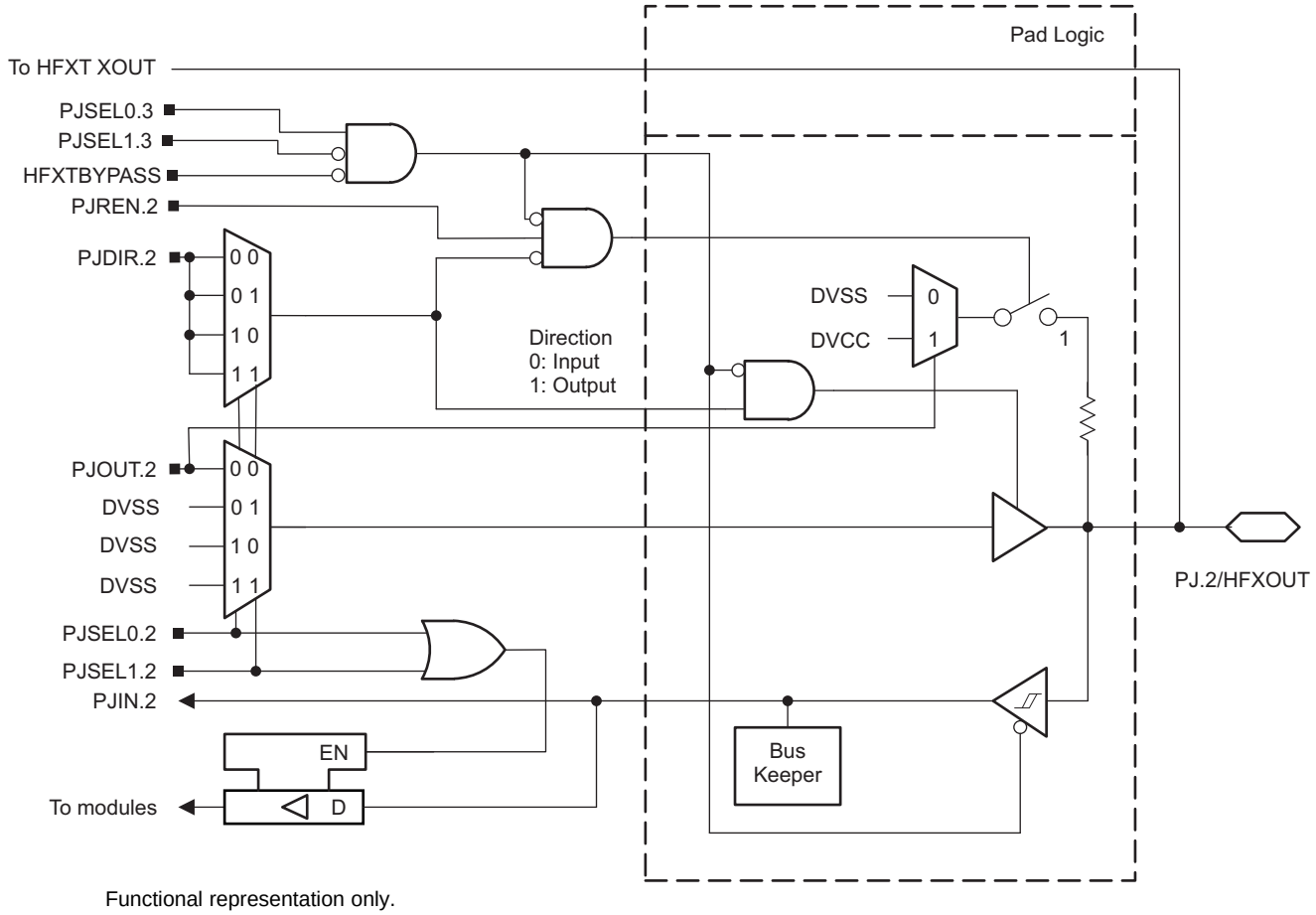


图 6-22. Port PJ (PJ.2) Schematic

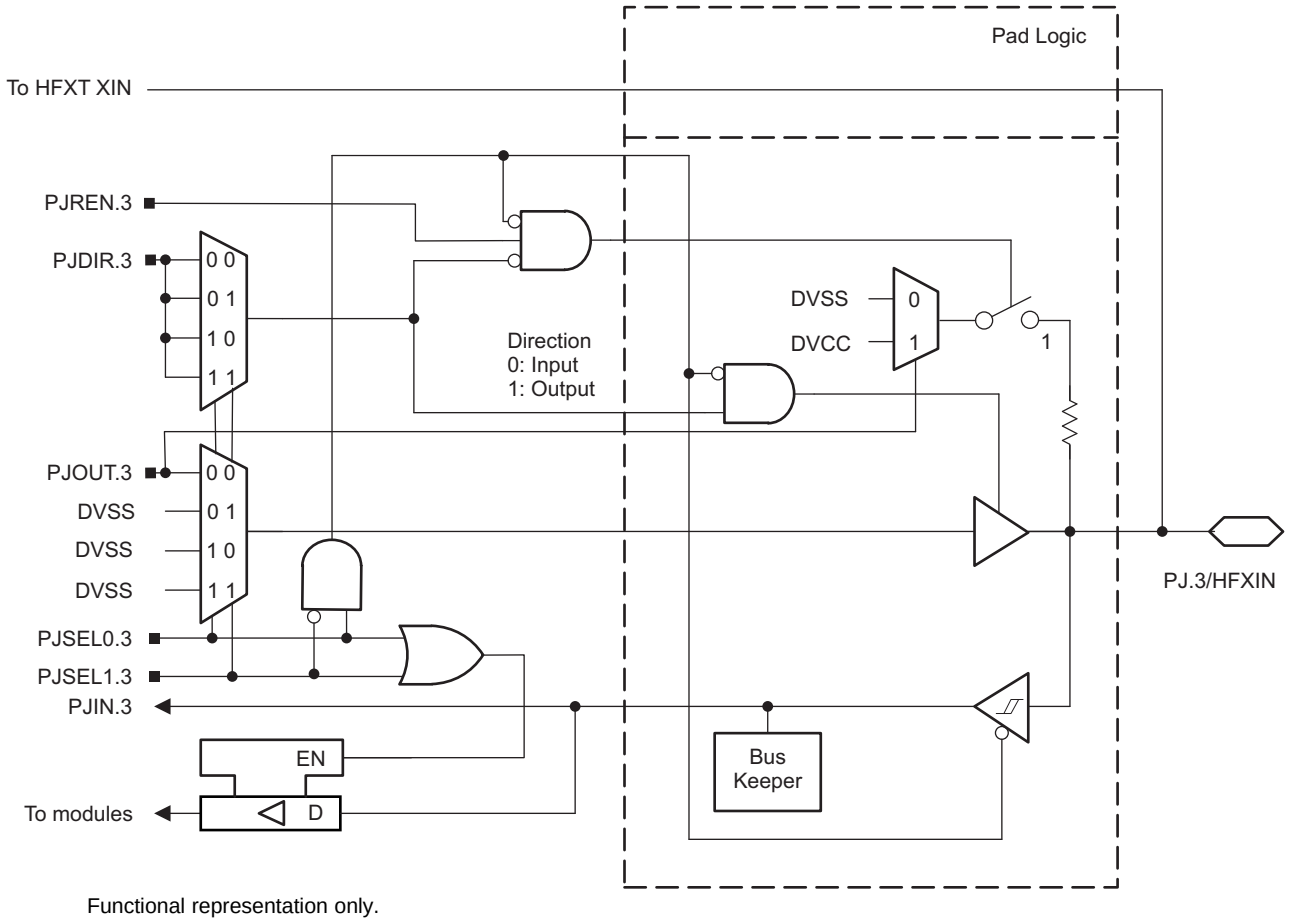


图 6-23. Port PJ (PJ.3) Schematic

表 6-83. Port PJ (PJ.2 and PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS (1)					
			PJDIR.x	PJSEL1.2	PJSEL0.2	PJSEL1.3	PJSEL0.3	HFXT BYPASS
PJ.3/HFXIN	3	PJ.3 (I/O)	I: 0; O: 1	X	X	0	0	X
		N/A	0	X	X	1	X	X
		DVSS	1					
		HFXIN crystal mode (2)	X	X	X	0	1	0
		HFXIN bypass mode (2)	X	X	X	0	1	1
PJ.2/HFXOUT	2	PJ.2 (I/O)	I: 0; O: 1	0	0	0	0	0
						1	X	
						X	X	1 (3)
		N/A	0	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		DVSS	1	see (4)	see (4)	0	0	0
						1	X	
						X	X	1 (3)
		HFXOUT crystal mode (2)	X	X	X	0	1	0

(1) X = Don't care
(2) Setting PJSEL1.3 = 0 and PJSEL0.3 = 1 causes the general-purpose I/O to be disabled. When HFXTBYPASS = 0, PJ.2 and PJ.3 are configured for crystal operation and PJSEL1.2 and PJSEL0.2 are do not care. When HFXTBYPASS = 1, PJ.3 is configured for bypass operation and PJ.2 is configured as general-purpose I/O.
(3) When PJ.3 is configured in bypass mode, PJ.2 is configured as general-purpose I/O.
(4) With PJSEL0.2 = 1 or PJSEL1.2 =1 the general-purpose I/O functionality is disabled. No input function is available. When configured as output, the pin is actively pulled to zero.

6.12.24 Port PJ, PJ.4 and PJ.5 Input/Output With Schmitt Trigger

表 6-84 lists the settings to select the pin function.

表 6-84. Port PJ (PJ.4 to PJ.5) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)				SWJ MODE OF OPERATION (1)
			PJDIR.x	PJSEL1.x	PJSEL0.x	PJMAPx	
PJ.4/TDI (2),	4	PJ.4 (I/O)	I: 0; O: 1	0	0	X	X
		TDI	X	0	1	default (3)	JTAG (4 wire)
		DVcc					SWD (2 wire)
		DVcc	X	1	X	X	X
PJ.5/TDO/SWO (4), (5)	5	PJ.5 (I/O)	I: 0; O: 1	0	0	X	X
		TDO	X	0	1	default (3)	JTAG (4 wire)
		SWO					SWD (2 wire)
		Hi-Z	X	1	X	X	X

(1) X indicates that the value of the control signal or mode of operation has no effect on the functionality.
(2) This pin is internally pulled up if PJSEL0 is 1.
(3) The *default* value in the table indicates the functionality that is selected whenever a Hard Reset (or higher class reset) occurs.
(4) This pin is has no internal pull feature. If used in User IO mode or left unused, pull to GND through an external pulldown resistor.
(5) After any hard reset (or higher class reset), this pin returns to TDO functionality with the SWJ in JTAG (4 wire) mode of operation. If used in User IO mode, this pin reflects the value of the external pullup until the PJSELx bits are reconfigured to the value 00.

6.12.25 Ports SWCLKTCK and SWDIOTMS With Schmitt Trigger

表 6-85 lists the settings to select the pin function.

表 6-85. Ports SWCLKTCK and SWDIOTMS Pin Functions

PIN NAME	FUNCTION	SWJ MODE OF OPERATION
SWCLKTCK (1)	TCK (input)	JTAG (4 wire)
	SWCLK (input)	SWD (2 wire)
SWDIOTMS (2)	TMS (input)	JTAG (4 wire)
	SWDIO (I/O)	SWD (2 wire)

(1) This pin is internally pulled to DV_{SS}.
(2) This pin is internal pulled to DV_{CC}.

6.13 Device Descriptors (TLV)

表 6-86 summarizes the Device IDs of the MSP432P4x1xT devices.

表 6-86. Device IDs

DEVICE	DEVICE ID
MSP432P4111TPZ	0000A020h
MSP432P411YTPZ	0000A022h
MSP432P411VTPZ	0000A026h
MSP432P4011TRGC	0000A029h
MSP432P401YTRGC	0000A02Bh
MSP432P401VTRGC	0000A02Fh

表 6-87 lists the contents of the device descriptor tag-length-value (TLV) structure for the MSP432P4x1xT devices.

表 6-87. Device Descriptor Table(1)

	DESCRIPTION	ADDRESS	VALUE
	TLV checksum	00201000h	Per unit
Info Block	Device Info Tag	00201004h	0000000Bh
	Device Info Length	00201008h	00000004h
	Device ID	0020100Ch	See 表 6-86.
	HW Revision	00201010h	00000041h
	Boot-code Revision	00201014h	00430044h
	ROM Driver Library Revision	00201018h	03400011h
Die Record	Die Record Tag	0020101Ch	0000000Ch
	Die Record Length	00201020h	00000008h
	Die X Position	00201024h	Per unit
	Die Y Position	00201028h	Per unit
	Wafer ID	0020102Ch	Per unit
	Lot ID	00201030h	Per unit
	Reserved	00201034h	Per unit
	Reserved	00201038h	Per unit
	Reserved	0020103Ch	Per unit
	Test Results	00201040h	FFFFFFFFh

(1) Per unit = the contents can differ from device to device

表 6-87. Device Descriptor Table(1) (continued)

	DESCRIPTION	ADDRESS	VALUE
Clock System Calibration	Clock System Calibration Tag	00201044h	00000003h
	Clock System Calibration Length	00201048h	00000010h
	DCO IR mode: Frequency calibration for DCORSEL 0 to 4	0020104Ch	Per unit
	Reserved	00201050h	FFFFFFFFh
	Reserved	00201054h	000000C0h
	Reserved	00201058h	000002C0h
	Reserved	0020105Ch	0000002Ah
	Reserved	00201060h	000002C0h
	DCO IR mode: DCO Constant (K) for DCORSEL 0 to 4	00201064h	Per unit
	Reserved	00201068h	FFFFFFFFh
	DCO ER mode: Frequency calibration for DCORSEL 0 to 4	0020106Ch	Per unit
	Reserved	00201070h	FFFFFFFFh
	Reserved	00201074h	000000B4h
	Reserved	00201078h	000002C0h
	Reserved	0020107Ch	00000028h
	Reserved	00201080h	000002C0h
	DCO ER mode: DCO Constant (K) for DCORSEL 0 to 4	00201084h	Per unit
	Reserved	00201088h	FFFFFFFFh
ADC14 Calibration	ADC14 Calibration Tag	0020108Ch	00000005h
	ADC14 Calibration Length	00201090h	00000018h
	Reserved	00201094h	FFFFFFFFh
	Reserved	00201098h	FFFFFFFFh
	Reserved	0020109Ch	FFFFFFFFh
	Reserved	002010A0h	FFFFFFFFh
	Reserved	002010A4h	FFFFFFFFh
	Reserved	002010A8h	FFFFFFFFh
	Reserved	002010ACh	FFFFFFFFh
	Reserved	002010B0h	FFFFFFFFh
	Reserved	002010B4h	FFFFFFFFh
	Reserved	002010B8h	FFFFFFFFh
	Reserved	002010BCh	FFFFFFFFh
	Reserved	002010C0h	FFFFFFFFh
	Reserved	002010C4h	FFFFFFFFh
	Reserved	002010C8h	FFFFFFFFh
	Reserved	002010CCh	FFFFFFFFh
	Reserved	002010D0h	FFFFFFFFh
	Reserved	002010D4h	FFFFFFFFh
	Reserved	002010D8h	FFFFFFFFh
	ADC 1.2V Reference Temp. Sensor 30°C(2)	002010DCh	Per unit
	ADC 1.2V Reference Temp. Sensor 125°C(2)	002010E0h	Per unit
	ADC 1.45V Reference Temp. Sensor 30°C(2)	002010E4h	Per unit
	ADC 1.45V Reference Temp. Sensor 125°C(2)	002010E8h	Per unit
	ADC 2.5V Reference Temp. Sensor 30°C(2)	002010ECh	Per unit
	ADC 2.5V Reference Temp. Sensor 125°C(2)	002010F0h	Per unit
REF Calibration	REF Calibration Tag	002010F4h	00000008h
	REF Calibration Length	002010F8h	00000003h
	Reserved	002010FCh	FFFFFFFFh
	Reserved	00201100h	FFFFFFFFh
	Reserved	00201104h	FFFFFFFFh

(2) Corresponds to junction temperature

表 6-87. Device Descriptor Table(1) (continued)

	DESCRIPTION	ADDRESS	VALUE
Flash Info	Flash Info Tag	00201108h	00000004h
	Flash Info Length	0020110Ch	00000002h
	Flash Maximum Programming Pulses	00201110h	00000005h
	Flash Maximum Erase Pulses	00201114h	0000014Eh
Random Number	128-bit Random Number Tag	00201118h	0000000Dh
	128-bit Random Number Length	0020111Ch	00000004h
	128-bit Random Number(3)	00201120h	Per unit
		00201124h	Per unit
		00201128h	Per unit
		0020112Ch	Per unit
BSL Configuration	BSL Configuration Tag	00201130h	0000000Fh
	BSL Configuration Length	00201134h	00000004h
	BSL Peripheral Interface Selection	00201138h	FFC2D0C0h
	BSL Port Interface Configuration for UART	0020113Ch	FCFFFDA0h
	BSL Port Interface Configuration for SPI	00201140h	F0FF9770h
	BSL Port Interface Configuration for I2C	00201144h	FCFFFF72h
TLV End	TLV End Word	00201148h	0BD0E11Dh
	Reserved	0020114Ch-00201FFFh	FFFFFFFFh

(3) 128-Bit Random Number: The random number is generated during production test using the CryptGenRandom() function from Microsoft®.

6.14 Identification

6.14.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 节 8.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Hardware Revision entry in the Device Descriptor structure (see 节 6.13).

6.14.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to the errata sheets for the devices in this data sheet, see 节 8.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the Device ID entry in the Device Descriptor structure (see 节 6.13).

6.14.3 Arm Cortex-M4F ROM Table Based Part Number

MSP432P4xx family of devices incorporate a part number for the device in addition to the device IDs specified in the device descriptors (TLV) for the IDEs to recognize the device. This section describes how this information is organized on the device.

The IEEE 1149.1 standard defines the use of a IDCODE register in the JTAG chain that provides the fields in 表 6-88

表 6-88. Structure of Device Identification Code

Bit Position	Field Description
31-28	Version
27-12	Part Number of the device
11-1	Manufacturer Identity
0	Reserved (Always tied to 1)

On MSP432P4xx devices all the fields in 表 6-88 are implemented on the Arm Cortex-M4 ROM table. The part number can be read by the IDE tools to determine the device with which they are working.

图 6-24 shows the Peripheral ID register bit descriptions according to the Arm Cortex-M4 specifications.

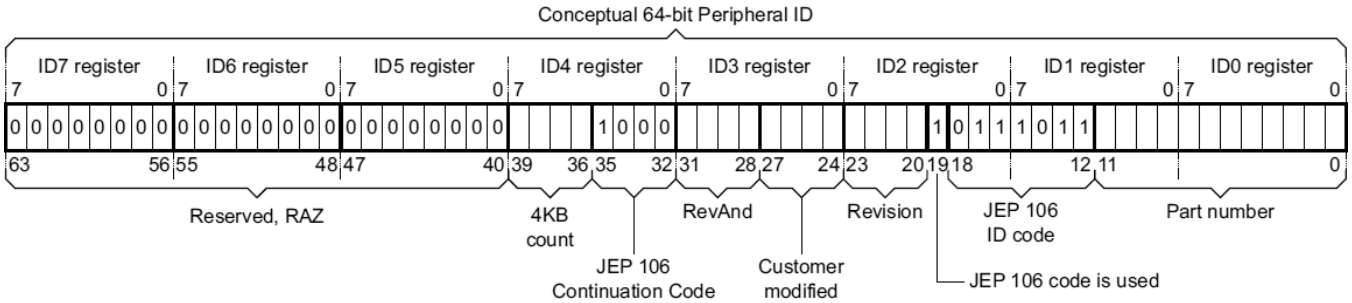


图 6-24. Arm Cortex-M4 Peripheral ID Register Description

See the *Arm Debug Interface V5 Architecture Specification* for bit-level details on the Arm Cortex-M4 Peripheral ID registers.

图 6-24 shows that a one-to-one mapping is not possible for the following fields from 表 6-88

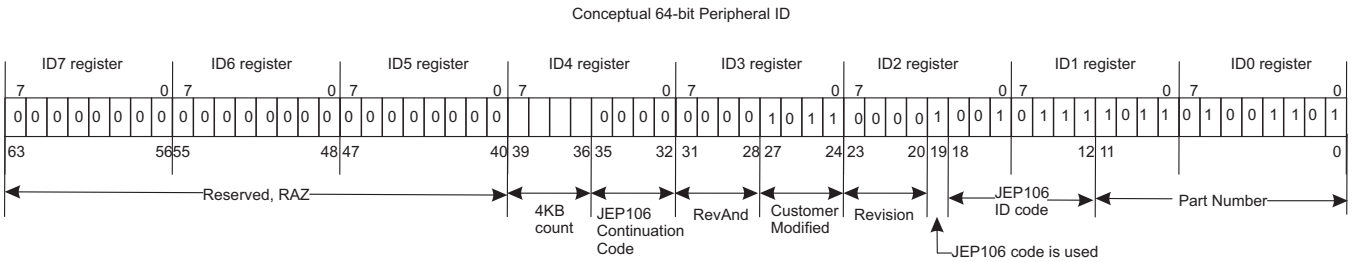
1. Version: IEEE 1149.1 defines a 4-bit field, whereas the CoreSight®-compliant PID registers have 4 bits

each for Revision (major revision) and RevAnd (minor revision).

2. Part Number: IEEE 1149.1 defines a 16-bit entity. However, the PID registers in the ROM table have only 12 bits reserved for this purpose (part number in the PID1 and PID0 registers).

For the MSP432P4xx family, the Revision and RevAnd fields store the major and minor revisions, and the 4-bit customer-modified field extends the part number to 16 bits, which accommodates all the fields needed by IEEE 1149.1 into the ROM table.

The ROM table with the IEEE 1149.1 complaint device IDCODE for MSP432P4x1xT device example is 0000-1011-1011-0100-1101-0000-0010-1111 and is populated as shown in 图 6-25.



Bits with no value shown are IMPLEMENTATION DEFINED.
Other bits not shown as Reserved are for an implementation designed by Arm Limited.

图 6-25. ROM PID Entries for MSP432P4x1xT Device

7 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP432P4xx microcontrollers. These guidelines are established to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 4.7-µF plus a 100-nF low-ESR ceramic decoupling capacitor to each AVCC and DVCC pin. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Additionally, separated grounds with a single-point connection are recommended for better noise isolation from digital-to-analog circuits on the board and are particularly recommended to achieve high analog accuracy.

图 7-1 shows the recommended decoupling of the power supply pins.

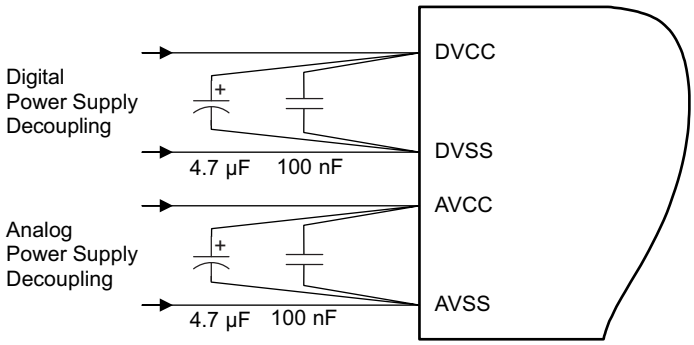


图 7-1. Power Supply Decoupling

7.1.2 External Oscillator

The device supports a low-frequency crystal (32.768 kHz) on the LFXT pins and a high-frequency crystal on the HFXT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN and HFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS or HFXTBYPASS mode is selected. In this case, the associated LFXOUT and HFXOUT pins can be used for other purposes.

图 7-2 shows a typical connection diagram.

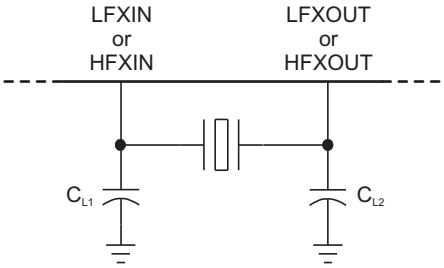


图 7-2. Typical Crystal Connection

See *MSP430 32-kHz Crystal Oscillators* for more information on selecting, testing, and designing a crystal oscillator with the MSP432 devices.

7.1.3 General Layout Recommendations

- Use proper grounding and short traces for the external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Use specified bypass capacitors on DVCC, AVCC, and reference pins, if used.
- Do not route any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Design in proper ESD level protection to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

7.1.4 Do's and Don'ts

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in Absolute Maximum Ratings. Exceeding the specified limits may cause malfunction of the device.

7.2 Peripheral and Interface-Specific Design Information

7.2.1 Precision ADC Peripheral

7.2.1.1 Partial Schematic

图 7-3 shows the recommended decoupling circuit when an external voltage reference is used.

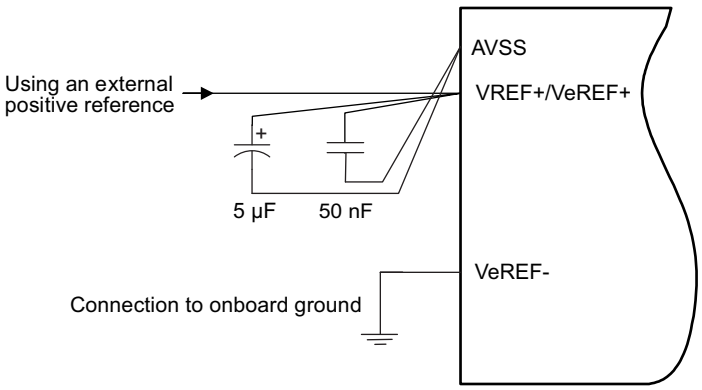


图 7-3. Precision ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate PCB layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in 节 7.1.1 combined with the connections shown in 节 7.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 5-µF capacitor is used to buffer the reference pin and filter any low-frequency ripple. A 50-nF bypass capacitor is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see 图 7-3) should be placed as close as possible to the respective device pins. Avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

If differential mode is used for the Precision ADC, the analog differential input signals must be routed closely together to minimize the effect of noise on the resulting signal.

8 器件和文档支持

8.1 开始使用

有关 MSP432™ 系列器件以及有助于开发的工具和库的更多信息，请访问 SimpleLink™ Arm® MSP432 微控制器。

8.2 器件命名规则

为了标明产品开发周期的阶段，TI 为所有 MSP MCU 器件的部件号分配了前缀。每个 MSP MCU 商用系列产品成员都具有以下两个前缀之一：MSP 或 XMS。这些前缀代表了产品开发的发展阶段，即从工程原型 (XMS) 直到完全合格的生产器件 (MSP)。

XMS - 实验器件，不一定代表最终器件的电气规格

MSP - 完全合格的生产器件

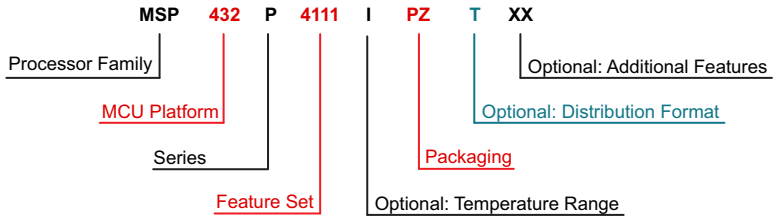
XMS 器件在供货时附带如下免责声明：

“开发中的产品用于内部评估用途。”

MSP 器件的特性已经全部明确，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书对该器件适用。

预测显示原型器件 (XMS) 的故障率大于标准生产器件。由于这些器件的预计最终使用故障率尚不确定，德州仪器 (TI) 建议不要将它们用于任何生产系统。请仅使用合格的生产器件。

TI 器件的命名规则还包括一个带有器件系列名称的后缀。此后缀表示温度范围、封装类型和配送形式。图 8-1 提供了解读完整器件名称的图例。



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon			
MCU Platform	432 = TI's 32-bit Low-Power SimpleLink Microcontroller Platform			
Series	P = Performance and Low-Power Series			
Feature Set	**First Digit** 4 = Flash-based devices	**Second Digit** 0 = General purpose 1 = LCD	**Third Digit** 1 = ADC14	**Fourth Digit** 1 = 2048KB of flash 256KB of SRAM Y = 1024KB of flash 256KB of SRAM V = 512KB of flash 128KB of SRAM
Optional: Temperature Range	S = 0°C to 50°C I = –40°C to 85°C T = –40°C to 105°C			
Packaging	http://www.ti.com/packaging			
Optional: Distribution Format	T = Small reel R = Large reel No markings = Tube or tray			
Optional: Additional Features	-EP = Enhanced product (–40°C to 105°C) -HT = Extreme temperature parts (–55°C to 150°C) -Q1 = Automotive Q100 qualified			

图 **8-1.** 器件命名规则

8.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请到 SimpleLink™ Arm® MSP432 微控制器中查看所有这些工具。

表 8-1 列出了支持的调试 特性。请参阅《*适用于 SimpleLink™ MSP432™ MCU 的 Code Composer Studio™ IDE 用户指南*》，以了解可用硬件详细信息 特性的详细信息。

表 8-1. 硬件调试 特性

系列	JTAG	SWD	断点数	ITM	DWT	FPB
MSP432P4xx	是	是	4	是	是	是

EnergyTrace 技术可用于 Code Composer Studio 6.0 及更高版本。它需要专用的调试器电路，而新一代板载 eZ-FET 闪存仿真工具和新一代独立 MSP-FET JTAG 仿真器支持这种电路。请参阅以下文档，了解更多详细信息。

《MSP430 高级功耗优化：ULP Advisor™ 和 EnergyTrace™ 技术》

《适用于 SimpleLink™ MSP432™ MCU 的 Code Composer Studio™ IDE 用户指南》

《MSP432™ SimpleLink™ 微控制器硬件工具用户指南》

设计套件与评估模块

MSP432P4111T LaunchPad™ 开发套件 MSP432P4111T LaunchPad 开发套件支持开发可从低功耗运行开发 需要低功耗运行的低于 1GHz 高性能无线应用。该套件 采用 MSP432P4111T 包括 24MHz Arm Cortex-M4F、100µA/MHz 工作功耗和 14.4µA RTC 运行、14 位 1Msps 差分 SAR ADC 以及 AES256 加速器。

适用于 **MSP432P4x MCU 的 100 引脚目标开发板** MSP-TS432PZ100 是一款独立的 ZIF 插座目标板，用于通过 JTAG 接口或串行线调试（SWD 2 线制 JTAG）协议对 MSP432 系统进行编程和调试。该开发板支持所有采用 100 引脚 LQFP 封装（TI 封装代码：PZ）的 MSP432P4x1xT 闪存部件。

软件

SimpleLink MSP432 软件开发套件 (SDK) SimpleLink MSP432 SDK 是一个全面的软件包，可帮助工程师快速开发基于 MSP432 MCU 的功能强大的 应用 。该 SDK 由多个兼容软件组件构成，其中包括 RTOS、驱动程序、中间件以及如何一起使用这些组件的示例。示例用于展示各功能区和支持的各个器件，并可用作您自己的项目的起点。SimpleLink MSP432 SDK 是 TI 的 SimpleLink 平台的一部分，允许在 SimpleLink MCU 之间实现 100% 的代码重用。

适用于 **MSP432 微控制器的 RTOS** MSP432 MCU 可与多种 TI 和第三方实时操作系统 (RTOS) 兼容。

MSP EnergyTrace™ 技术 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

开发工具

适用于 **MSP 微控制器的 Code Composer Studio 集成开发环境** Code Composer Studio 是一种集成开发环境 (IDE)，支持所有 MSP 微控制器。Code Composer Studio 包含一整套开发和调试嵌入式应用 的嵌入式软件实用程序的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。有关更多信息，请参阅《*适用于 SimpleLink™ MSP432™ MCU 的 Code Composer Studio™ IDE 7.1+ 用户指南*》。

Arm® Keil® MDK - 免费 32KB IDE Arm Keil MDK 是一套完整的调试器和 C/C++ 编译器工具链，可用于构建和调试嵌入式 应用而设计的单片集成电路。Keil MDK 支持低功耗 + 高性能 MSP432 MCU 系列，并且包括一个全集成调试器，适用于源代码级调试和反汇编级调试，支持复杂代码和数据断点。有关更多信息，请参阅 *《适用于 SimpleLink™ MSP432™ MCU 的 ARM® Keil® MDK 版本 5 的用户指南》*。

IAR Embedded Workbench Kickstart 适用于 MSP 的 IAR 嵌入式工作平台 Kickstart 是一套完整的调试器和 C/C++ 编译器工具链， 应用 。MSP430 器件和 MSP432 器件的 C/C++ 编译器代码大小限制分别为 8KB 和 32KB。有关更多信息，请参阅*《适用于 SimpleLink™ MSP432™ MCU 的 ARM 7.x IAR 嵌入式工作平台用户指南》*。

《MSP432P4xx CMSIS 器件系列软件包》 TI 为 MSP432P4xx 器件提供了符合 CMSIS 标准的器件系列套件。此套件向 IAR EWARM 8.x、Keil MDK 5.x 和 Atollic TrueSTUDIO® 7.x。在 IAR EWARM 中，该套件是可选的，因为 IDE 本身便支持这些器件。

适用于 MSP432 的调试器 根据设计，MSP432 MCU 可与德州仪器 (TI) 及第三方供应商的各种调试器结合使用。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可让用户在 MSP 低功耗微控制器 (MCU) 上快速进行应用开发。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 和 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

引脚复用工具 Pin Mux 实用程序是一款软件工具，可提供图形用户界面用于配置引脚多路复用设置、解决冲突以及指定 TI MPU 的 I/O 单元特性。结果采用 C 头文件和代码文件的形式输出，可导入软件开发套件 (SDK) 或用于配置定制软件。

ULP（超低功耗）Advisor ULP（超低功耗）Advisor 是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用独特的超低功耗 超低功耗 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地利用应用程序。

8.4 文档支持

以下文档对 MCU 进行了介绍。TI 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请转至 ti.com.cn 上您的器件对应的产品文件夹（关于产品文件夹的链接，请参见节 8.5）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《MSP432P4111T 器件勘误表》 介绍功能规格的已知例外情况。

《MSP432P411YT 器件勘误表》 介绍功能规格的已知例外情况。

《MSP432P411VT 器件勘误表》 介绍功能规格的已知例外情况。

《MSP432P4011T 器件勘误表》 介绍功能规格的已知例外情况。

《MSP432P401YT 器件勘误表》 介绍功能规格的已知例外情况。

《MSP432P401VT 器件勘误表》 说明了功能技术规格的已知例外情况。

用户指南

《MSP432P4xx SimpleLink™ 微控制器技术参考手册》 可 说明 。

《适用于 SimpleLink™ MSP432™ 微控制器的 Code Composer Studio™ IDE 用户指南》 此手册介绍了如何将 TI Code Composer Studio IDE (CCS) 与 MSP432 低功耗微控制器结合使用。

《适用于 SimpleLink™ MSP432™ 微控制器的 IAR Embedded Workbench for Arm 用户指南》 此手册介绍了如何将 IAR Embedded Workbench for Arm (EWARM) 与 MSP432 低功耗微控制器结合使用。

《适用于 SimpleLink™ MSP432™ 微控制器的 Arm® Keil® MDK 用户指南》 此用户指南介绍了如何将 Arm Keil MDK 与 MSP432 低功耗微控制器结合使用。

《适用于 SimpleLink™ MSP432™ 微控制器的 GCC ARM® 嵌入式工具链用户指南》 本手册介绍了使用 GCC ARM 编译器和 GDB 调试器对 MSP432 进行编程和调试时的设置和基本操作。

《MSP432™ SimpleLink™ 微控制器引导加载程序 (BSL) 用户指南》 MSP432 BSL 允许用户在原型设计、投产和维护等各阶段与 MSP432 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 可根据需要进行修改。

《MSP432 电容式触控软件库编程人员指南》 MSP432 微控制器配有执行电容测量所需的外设。电容式触控软件库专门用于创建可集成到 MSP432 器件外设集的单独界面。此文档介绍了电容式触控库配置以及与 MSP432 器件的交互使用。

应用报告

平台迁移至 SimpleLink™ MSP432™ 系列 本移植指南旨在帮助开发人员精确评估将现有应用由一种 MSP 平台移植到另一平台的相关工作，最终通过完整的软硬件覆盖范围制订移植策略，从而在避免因平台差异而引入漏洞的前提下正确移植现有应用，同时充分利用新平台引入的独特 特性 或性能改进措施。

《采用 SimpleLink™ MSP432™ 微控制器设计超低功耗 (ULP) 应用》 随着超低功耗微控制器 应用中系统复杂度的不断增大，最大程度降低总能耗已成为亟待解决的难题之一。硅片、其他板载硬件组件和应用软件等方面都必须加以考虑。一些效果明显的通用技术可以用来降低能耗，例如降低工作电压或频率。这些通用技术中有很多在单独使用时并不能显著降低能耗，但搭配起来使用时效果非常显著，因为它们之间存在强烈的依存关系。

《最大限度提高 MSP432P4xx 稳压器效率》 此应用报告介绍了 MSP432P4xx 直流/直流和 LDO 间的关系，提供了为应用选择最高效器件的相关指南，并介绍了直流/直流转换器电路板布局的注意事项。

《利用 SimpleLink™ MSP432P4xx 微控制器的低频功耗模式》 在所有电池供电的嵌入式 应用中，低功耗非常重要，但这些嵌入式 应用 的工作频率会因应用需求而异。某些 应用 需要在较高的频率下工作，大约几兆赫兹；而另外一些 应用 可能需要在较低的频率下工作，大约几十至几百千赫兹。当目标应用使用较低工作频率时，MSP432P4xx 微控制器的低频功耗模式可展现超低功耗性能。

MSP432P4xx 微控制器上的软件 IP 保护 嵌入式软件 应用程序不同， 最终的产品也会千差万别。各家公司纷纷投入大量资金来构建差异化软件应用程序。因此，保护这类资产（应用程序或部分应用程序）极为重要。此应用报告介绍了如何保护 MSP432P4xx 系列微控制器上所运行软件的知识产权 (IP)。

8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 **8-2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP432P4111T	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP432P4011T	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP432P411YT	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP432P401YT	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP432P411VT	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP432P401VT	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》。

TI E2E™ 社区
TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.7 商标

MSP432, SimpleLink, 有了 LaunchPad, LaunchPad, EnergyTrace, E2E are trademarks of Texas Instruments.
Arm, Cortex, Thumb, CoreSight, Keil are registered trademarks of Arm Limited.
Bluetooth is a registered trademark of Bluetooth SIG.
Microsoft is a registered trademark of Microsoft Corporation.
Wi-Fi is a registered trademark of Wi-Fi Alliance.

8.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

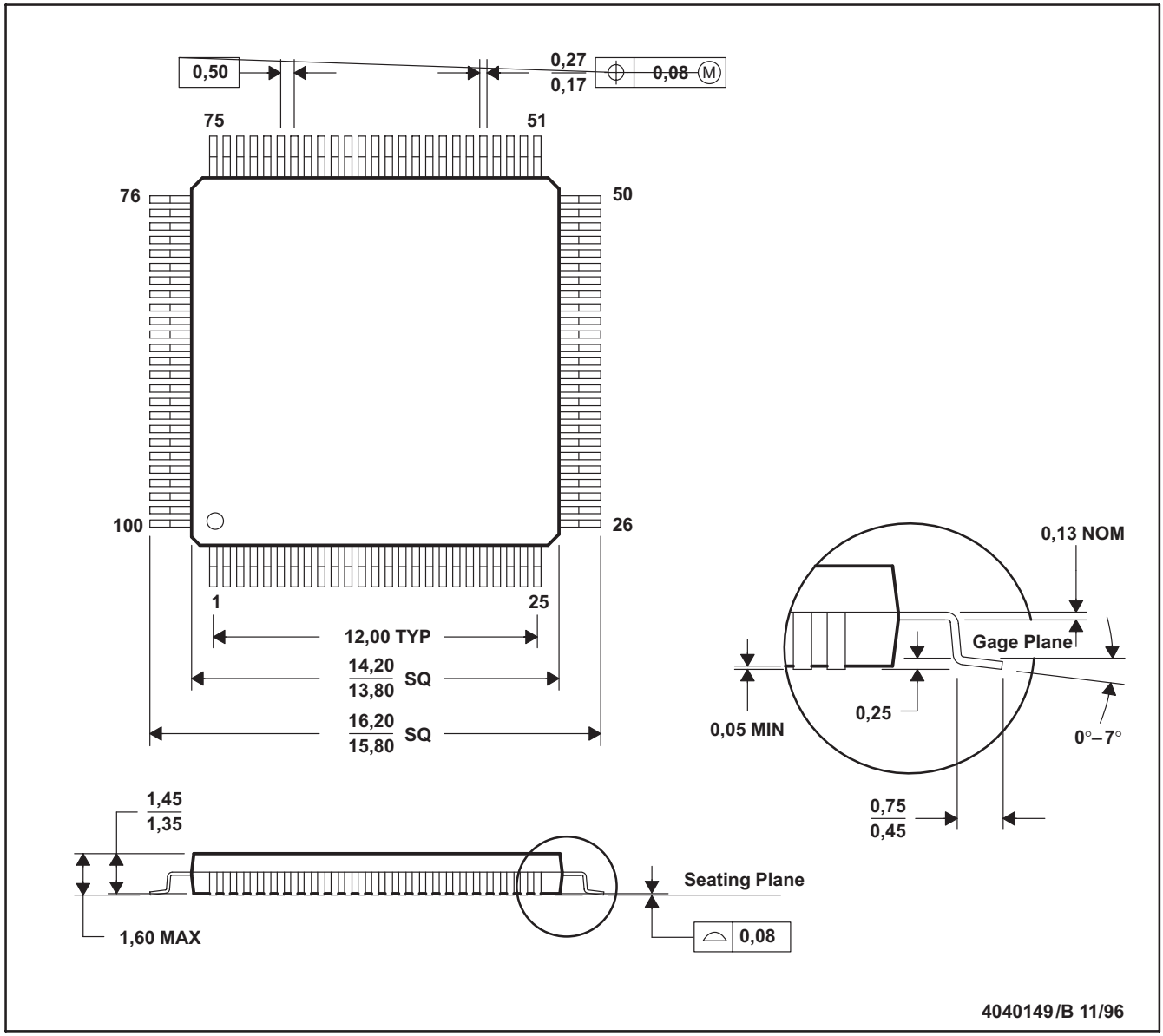
9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

MECHANICAL DATA

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

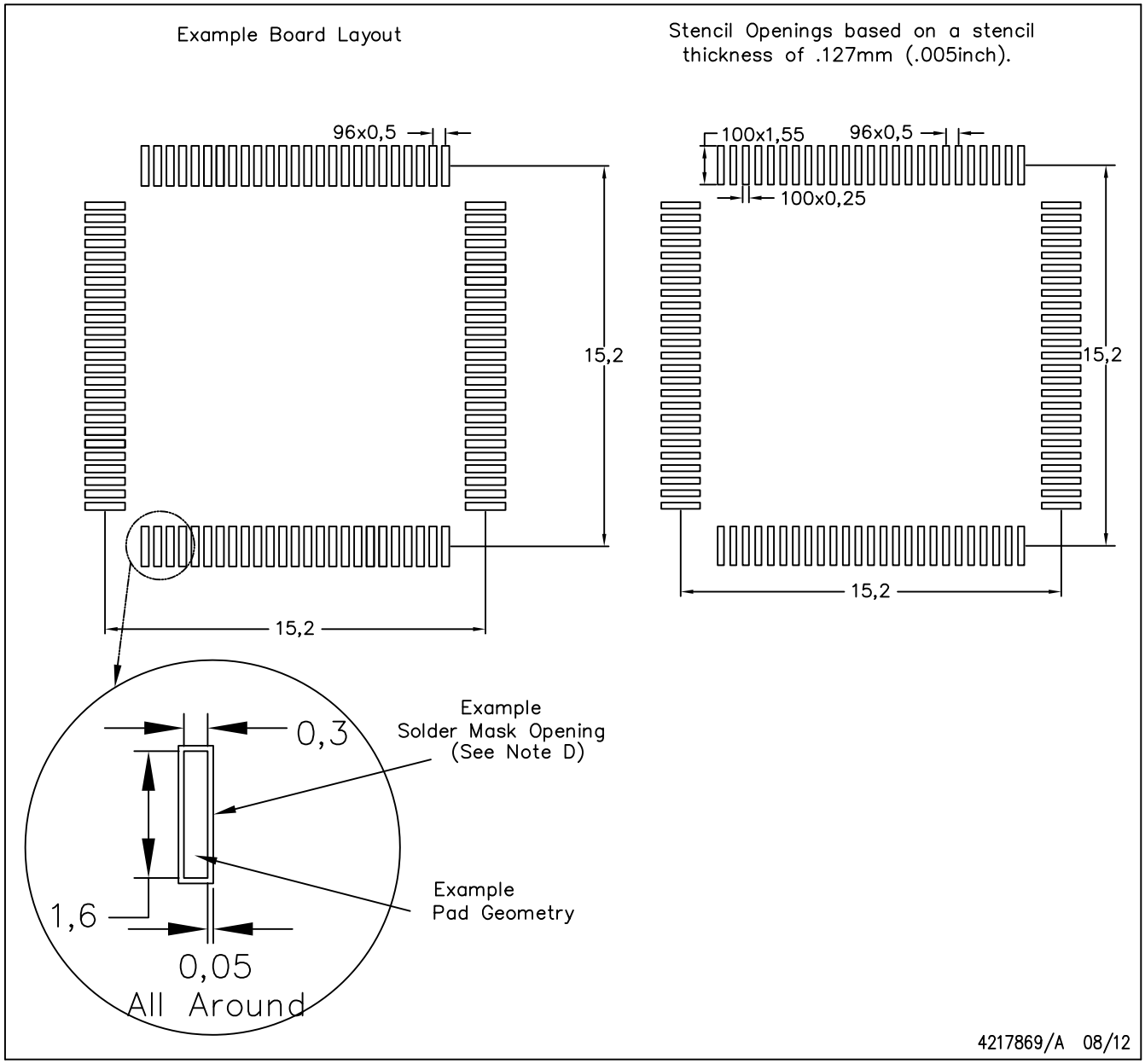
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

LAND PATTERN DATA

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK

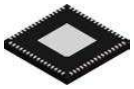


NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

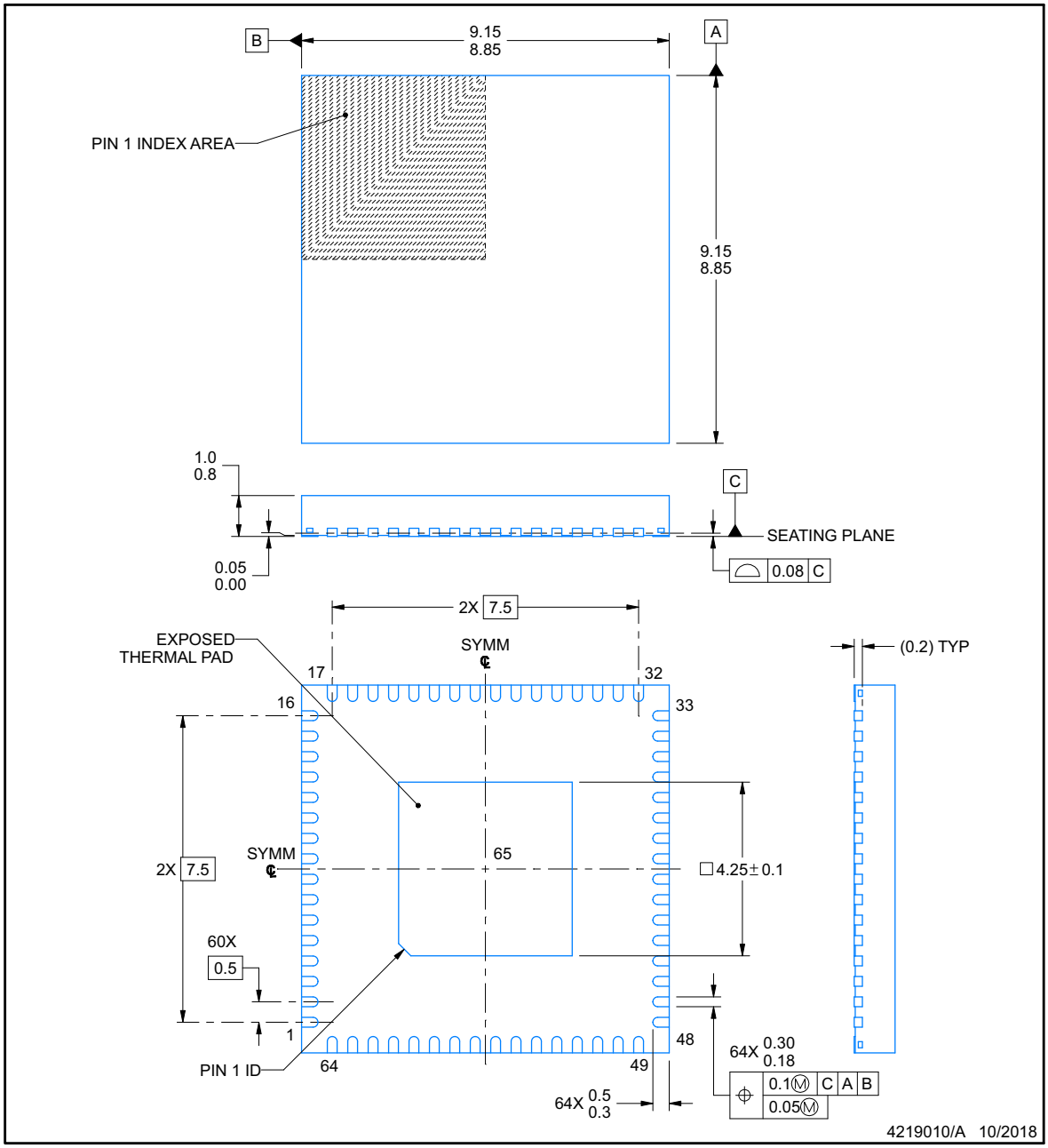
PACKAGE OUTLINE

RGC0064B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

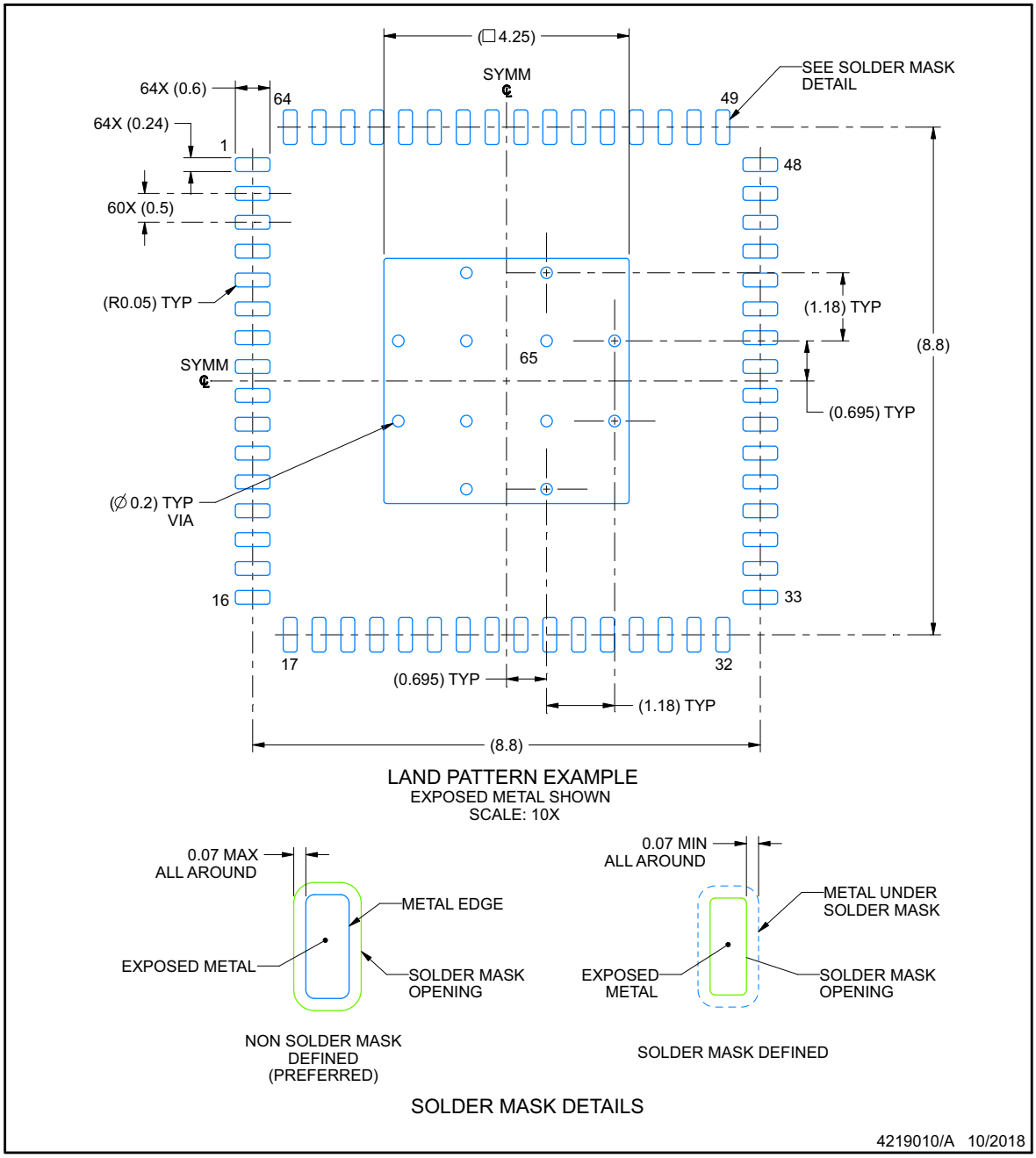
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGC0064B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



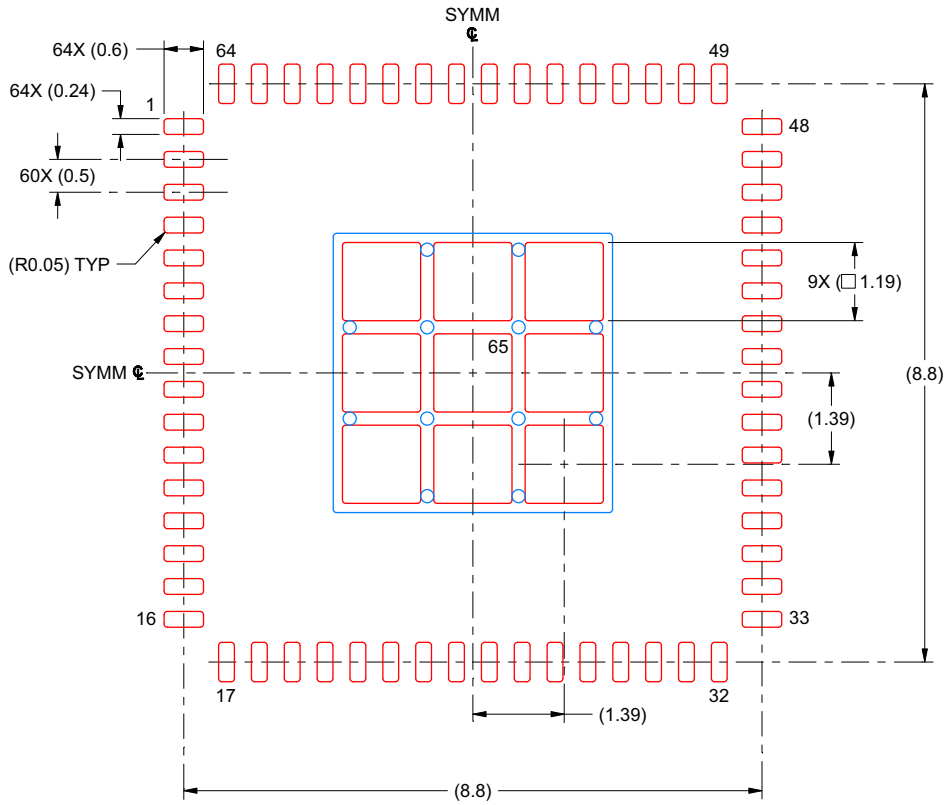
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGC0064B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219010/A 10/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP432P4011TRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P4011T	Samples
MSP432P4011TRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P4011T	Samples
MSP432P401VTRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P401VT	Samples
MSP432P401VTRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P401VT	Samples
MSP432P401YTRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P401YT	Samples
MSP432P401YTRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 105	P401YT	Samples
MSP432P4111TPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P4111T	Samples
MSP432P4111TPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P4111T	Samples
MSP432P411VTPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P411VT	Samples
MSP432P411VTPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P411VT	Samples
MSP432P411YTPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P411YT	Samples
MSP432P411YTPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	MSP432P411YT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

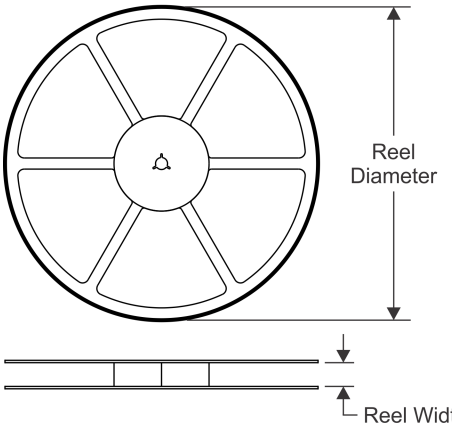
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

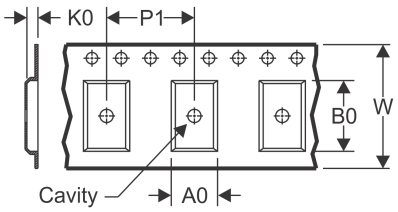
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

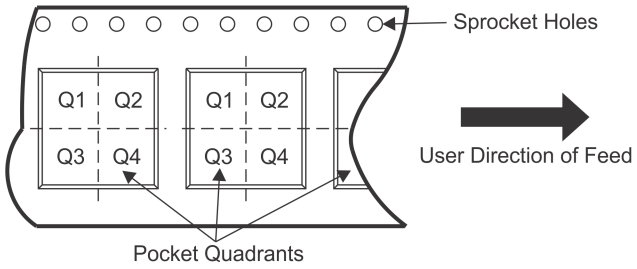


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

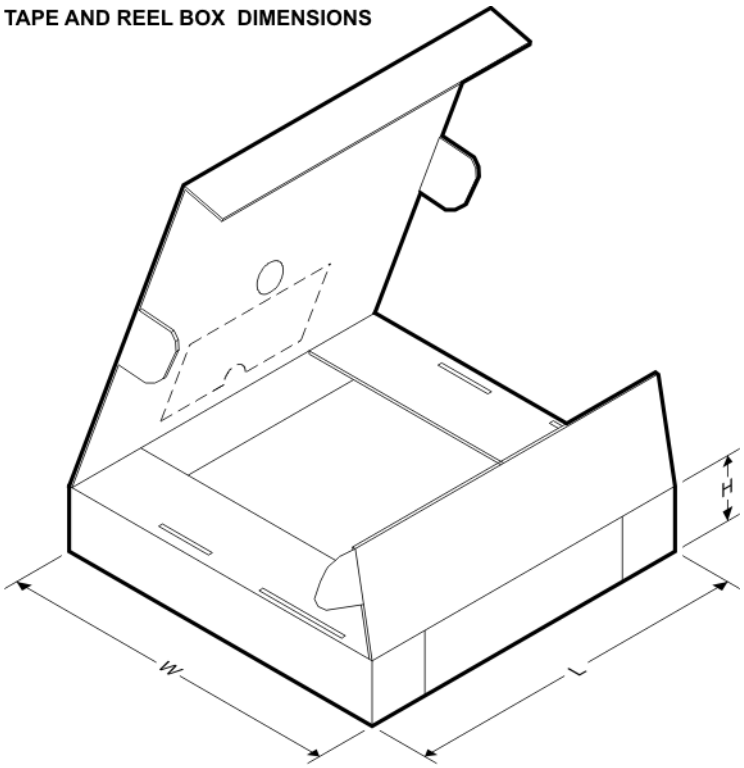
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP432P4011TRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P4011TRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P401VTRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P401VTRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P401YTRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P401YTRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
MSP432P4111TPZR	LQFP	PZ	100	1000	330.0	32.4	16.9	16.9	2.0	24.0	32.0	Q2
MSP432P411VTPZR	LQFP	PZ	100	1000	330.0	32.4	16.9	16.9	2.0	24.0	32.0	Q2
MSP432P411YTPZR	LQFP	PZ	100	1000	330.0	32.4	16.9	16.9	2.0	24.0	32.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP432P4011TRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP432P4011TRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP432P401VTRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP432P401VTRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP432P401YTRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP432P401YTRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP432P4111TPZR	LQFP	PZ	100	1000	367.0	367.0	55.0
MSP432P411VTPZR	LQFP	PZ	100	1000	367.0	367.0	55.0
MSP432P411YTPZR	LQFP	PZ	100	1000	367.0	367.0	55.0

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122