

FGD3440G2-F085V

EcoSPARK[®] 2 Ignition IGBT

335 mJ, 400 V, N-Channel Ignition IGBT

Features

- SCIS Energy = 335 mJ at $T_J = 25^\circ\text{C}$
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Application

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
BV_{CER}	Collector to Emitter Breakdown Voltage ($I_C = 1\text{ mA}$)	400	V
BV_{ECS}	Emitter to Collector Voltage – Reverse Battery Condition ($I_C = 10\text{ mA}$)	28	V
E_{SCIS25}	Self Clamping Inductive Switching Energy (Note 1)	335	mJ
$E_{SCIS150}$	Self Clamping Inductive Switching Energy (Note 2)	195	mJ
I_{C25}	Collector Current Continuous at $V_{GE} = 4.0\text{ V}$, $T_C = 25^\circ\text{C}$	26.9	A
I_{C110}	Collector Current Continuous at $V_{GE} = 4.0\text{ V}$, $T_C = 110^\circ\text{C}$	25	A
V_{GEM}	Gate to Emitter Voltage Continuous	± 10	V
P_D	Power Dissipation Total, $T_C = 25^\circ\text{C}$	166	W
	Power Dissipation Derating, $T_C > 25^\circ\text{C}$	1.1	W/ $^\circ\text{C}$
T_J	Operating Junction and Storage Temperature	-40 to $+175$	$^\circ\text{C}$
T_{STG}	Storage Junction Temperature Range	-40 to $+175$	$^\circ\text{C}$
T_L	Max. Lead Temperature for Soldering (Leads at 1.6 mm from case for 10 s)	300	$^\circ\text{C}$
T_{PKG}	Max. Lead Temperature for Soldering (Package Body for 10s)	260	$^\circ\text{C}$
ESD	HBM–Electrostatic Discharge Voltage at 100 pF, 1500 Ω	4	kV

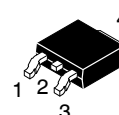
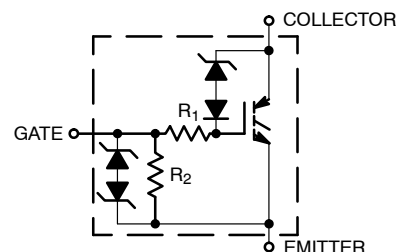
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self clamped inductive Switching Energy (E_{SCIS25}) of 335 mJ is based on the test conditions that is starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{SCIS} = 15\text{ A}$, $V_{CC} = 100\text{ V}$ during inductor charging and $V_{CC} = 0\text{ V}$ during time in clamp.
2. Self Clamped inductive Switching Energy ($E_{SCIS150}$) of 195 mJ is based on the test conditions that is starting $T_J = 150^\circ\text{C}$, $L = 3\text{ mH}$, $I_{SCIS} = 11.4\text{ A}$, $V_{CC} = 100\text{ V}$ during inductor charging and $V_{CC} = 0\text{ V}$ during time in clamp.



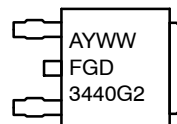
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DPAK (SINGLE GAUGE)
CASE 369C

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
FGD3440G2 = Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FGD3440G2–F085V

THERMAL RESISTANCE RATINGS

Characteristic	Symbol	Max	Units
Junction-to-Case – Steady State (Drain)	$R_{\theta JC}$	0.9	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ.	Max.	Units
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OFF CHARACTERISTICS

BV _{CER}	Collector to Emitter Breakdown Voltage	I _{CE} = 2 mA, V _{GE} = 0 V, R _{GE} = 1 kΩ, T _J = −40 to 150°C		370	400	430	V
BV _{CES}	Collector to Emitter Breakdown Voltage	I _{CE} = 10 mA, V _{GE} = 0 V, R _{GE} = 0, T _J = −40 to 150°C		390	420	450	V
BV _{ECS}	Emitter to Collector Breakdown Voltage	I _{CE} = −20 mA, V _{GE} = 0 V, T _J = 25°C		28	–	–	V
BV _{GES}	Gate to Emitter Breakdown Voltage	I _{GES} = ±2 mA		±12	±14	–	V
I _{CER}	Collector to Emitter Leakage Current	V _{CE} = 250 V R _{GE} = 1 kΩ	T _J = 25°C	–	–	25	μA
			T _J = 150°C	–	–	1	mA
I _{ECS}	Emitter to Collector Leakage Current	V _{EC} = 24 V	T _J = 25°C	–	–	1	mA
			T _J = 150°C	–	–	40	
R ₁	Series Gate Resistance			–	120	–	Ω
R ₂	Gate to Emitter Resistance			10K	–	30K	Ω

ON CHARACTERISTICS (Note 5)

$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 6\text{ A}$, $V_{GE} = 4\text{ V}$, $T_J = 25^\circ\text{C}$	–	1.1	1.2	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 10\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	–	1.3	1.45	V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	$I_{CE} = 15\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	–	1.6	1.75	V

DYNAMIC CHARACTERISTICS

Q _{G(ON)}	Gate Charge	I _{CE} = 10 A, V _{CE} = 12 V, V _{GE} = 5 V		–	24	–	nC
V _{GE(TH)}	Gate to Emitter Threshold Voltage	I _{CE} = 1 mA V _{CE} = V _{GE}	T _J = 25°C	1.3	1.7	2.2	V
			T _J = 150°C	0.75	1.2	1.8	
V _{GEP}	Gate to Emitter Plateau Voltage	V _{CE} = 12 V, I _{CE} = 10 A		–	2.8	–	V

SWITCHING CHARACTERISTICS

$t_{d(ON)R}$	Current Turn-On Delay Time–Resistive	$V_{CE} = 14\text{ V}$, $R_L = 1\text{ }\Omega$, $V_{GE} = 5\text{ V}$, $R_G = 1\text{ k}\Omega$, $T_J = 25^\circ\text{C}$	–	1.0	4	μs
t_{rR}	Current Rise Time–Resistive		–	2.0	7	
$t_{d(OFF)L}$	Current Turn-Off Delay Time–Inductive	$V_{CE} = 300\text{ V}$, $L = 1\text{ mH}$, $V_{GE} = 5\text{ V}$, $R_G = 1\text{ k}\Omega$, $I_{CE} = 6.5\text{ A}$, $T_J = 25^\circ\text{C}$	–	5.3	10	
t_{fL}	Current Fall Time–Inductive		–	2.3	15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Diameter	Tape Width	Qty [†]
FGD3440G2	FGD3440G2–F085V	DPAK (Pb–Free)	330 mm	16 mm	2500

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

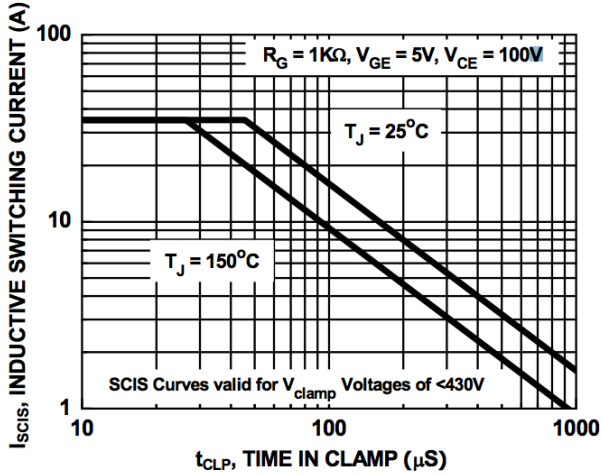


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

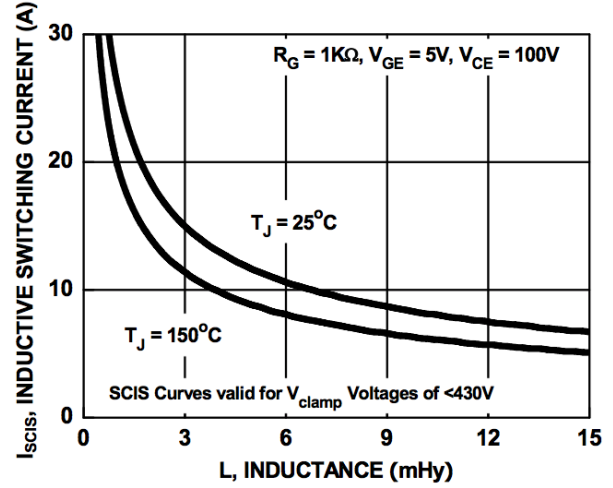


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

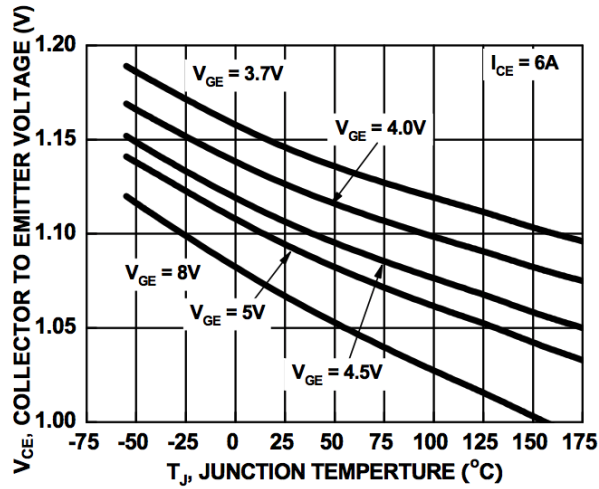


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

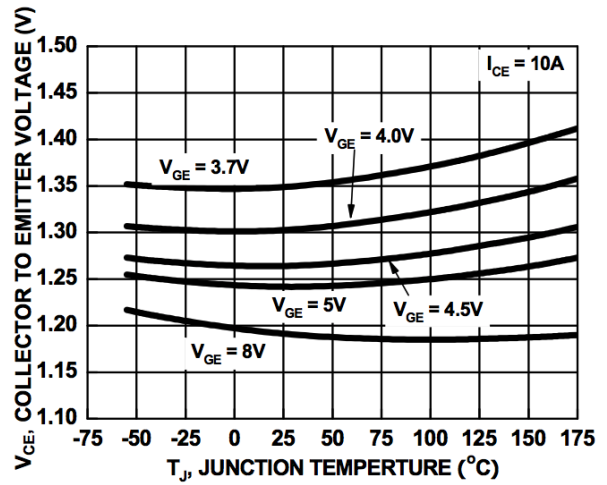


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

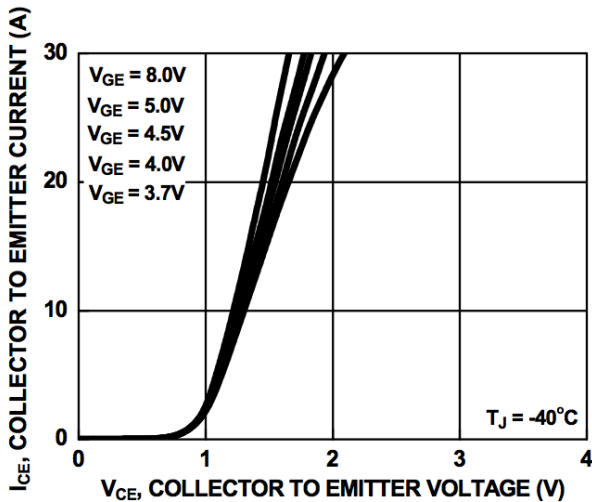


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

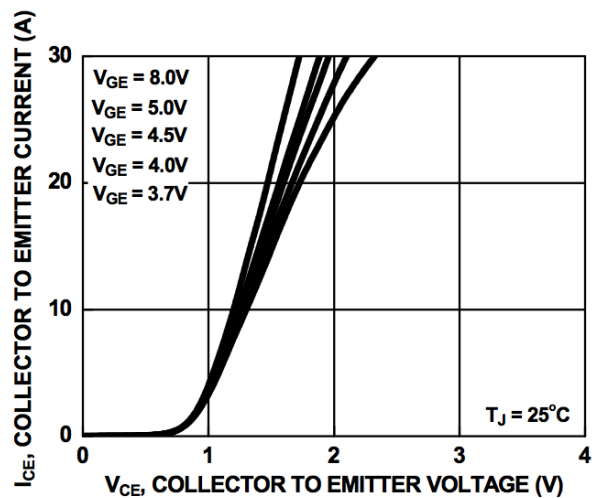


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

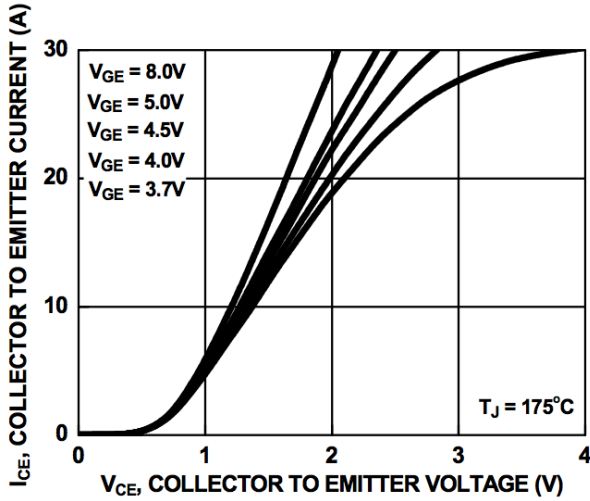


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

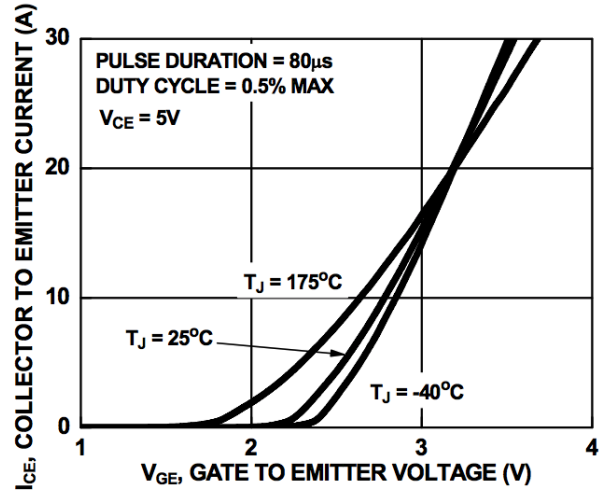


Figure 8. Transfer Characteristics

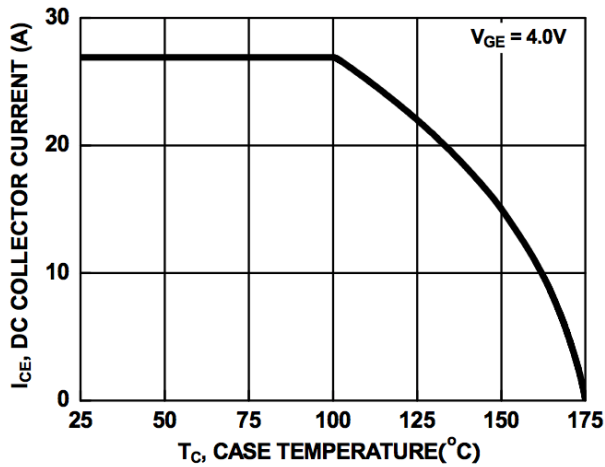


Figure 9. DC Collector Current vs. Case Temperature

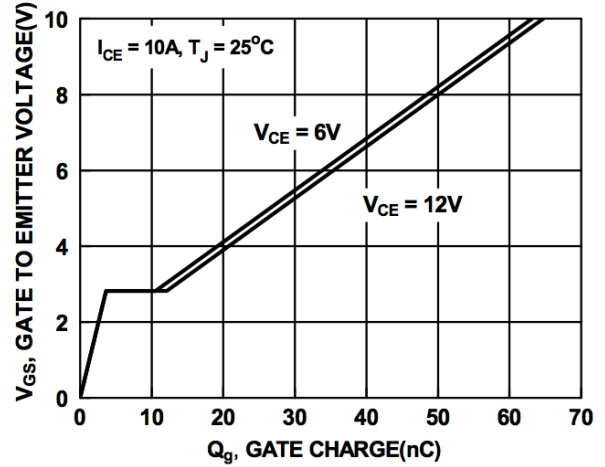


Figure 10. Gate Charge

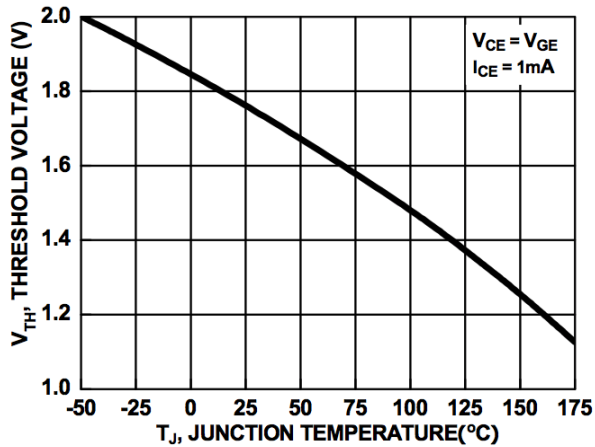


Figure 11. Threshold Voltage vs. Junction Temperature

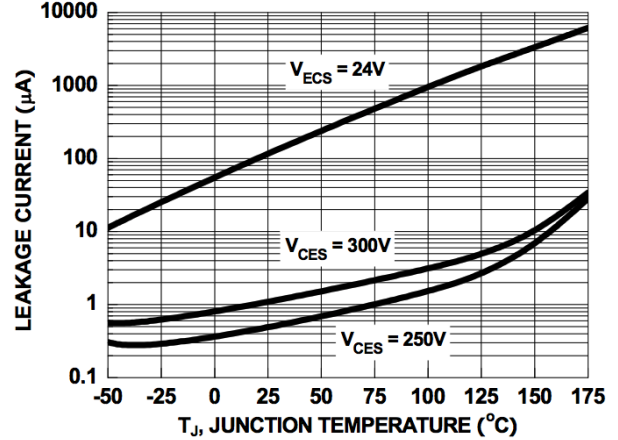


Figure 12. Leakage Current vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

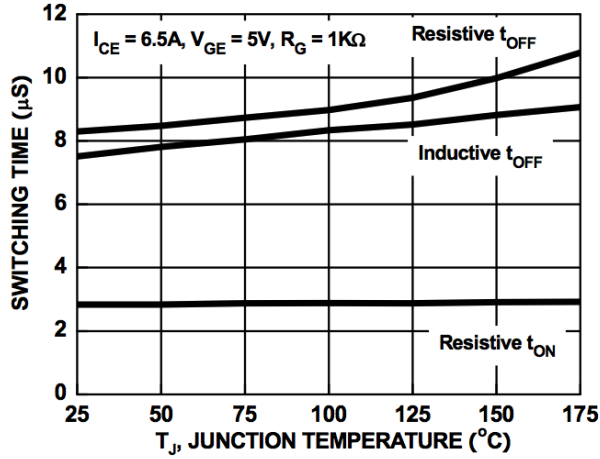


Figure 13. Switching Time vs. Junction Temperature

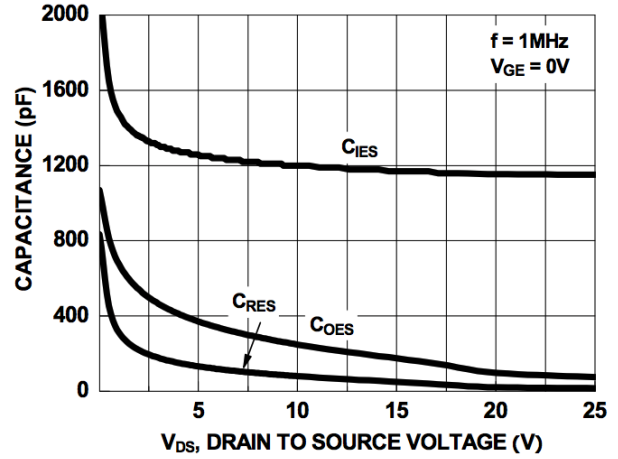


Figure 14. Capacitance vs. Collector to Emitter

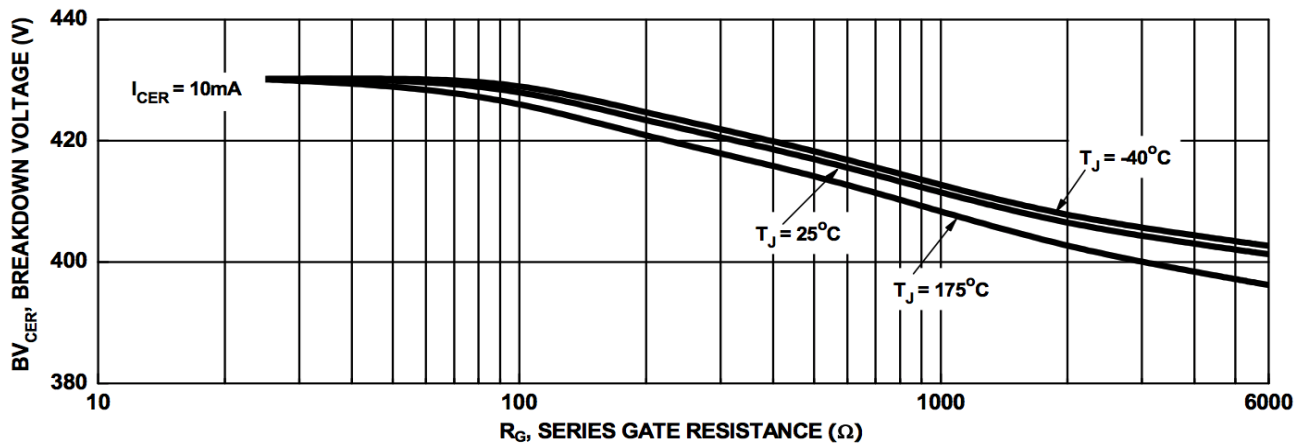


Figure 15. Break Down Voltage vs. Series Resistance

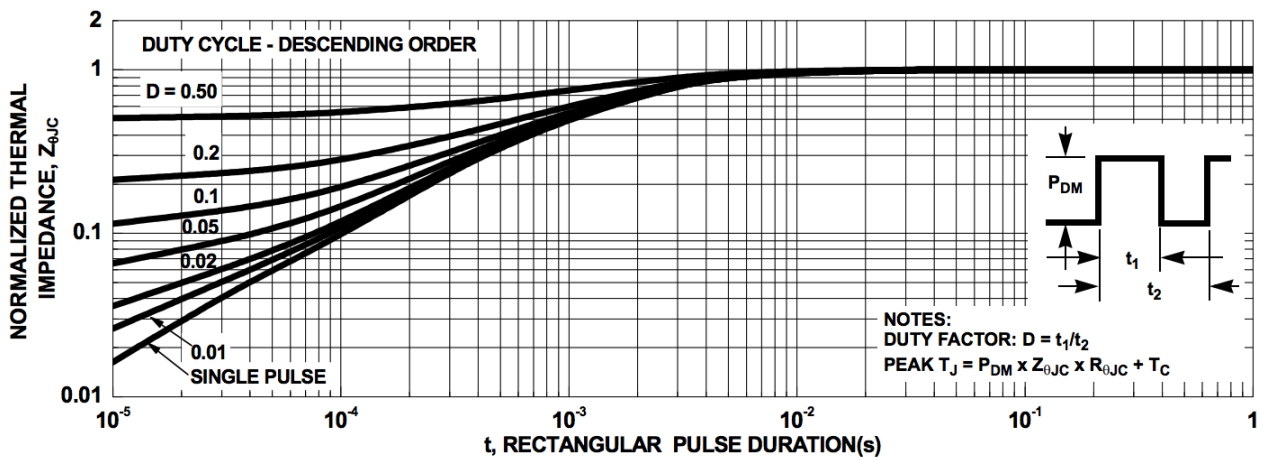


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUIT AND WAVEFORMS

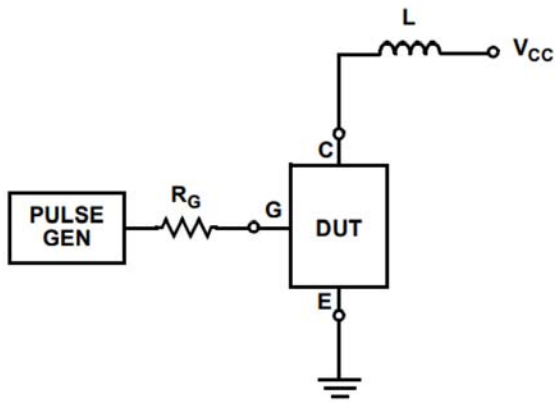


Figure 17. Inductive Switching Test Circuit

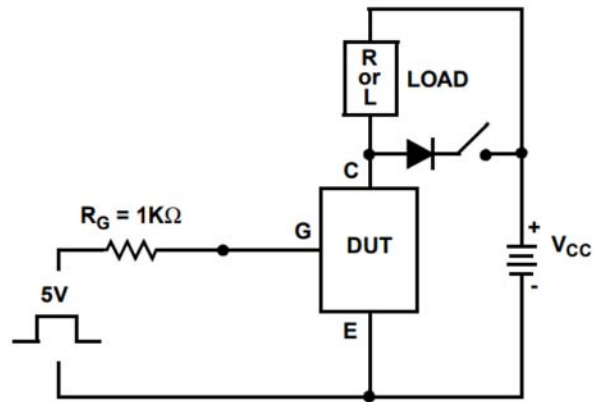


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

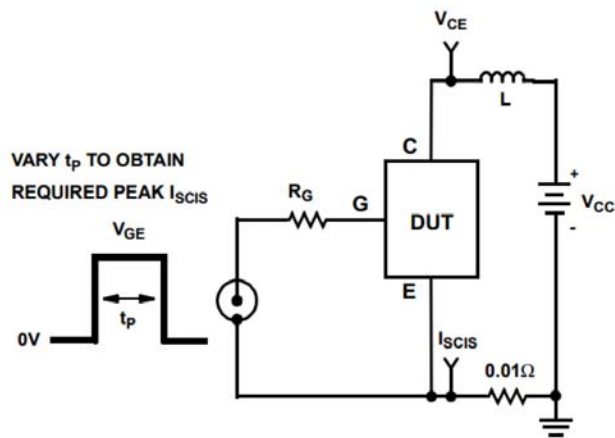


Figure 19. Energy Test Circuit

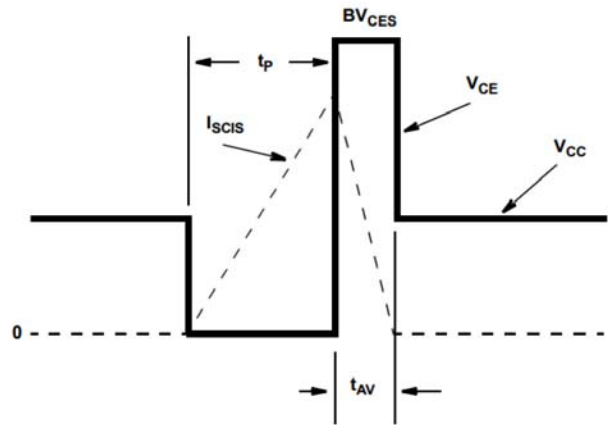


Figure 20. Energy Waveforms

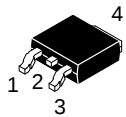
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON



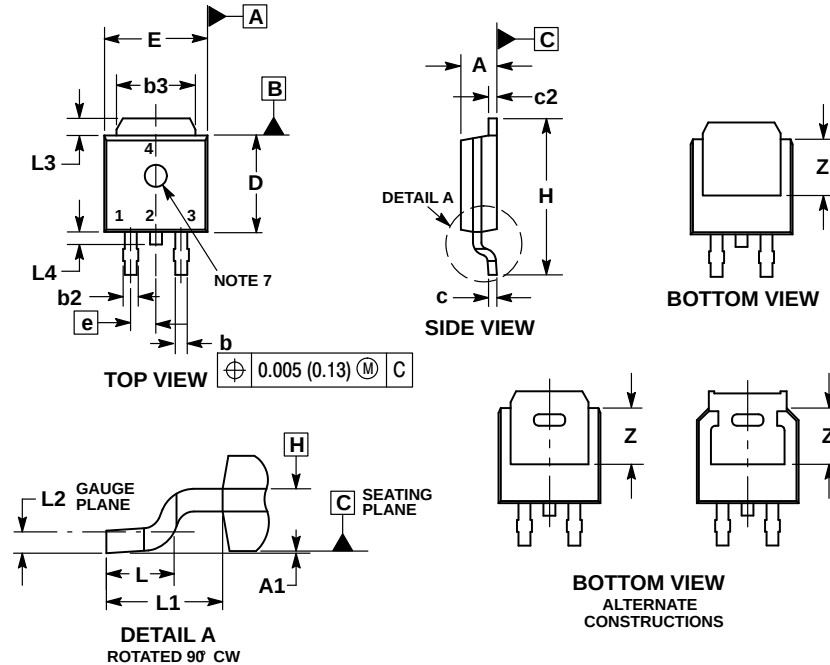
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE F

DATE 21 JUL 2015

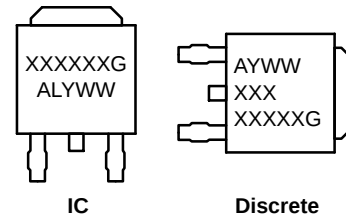


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

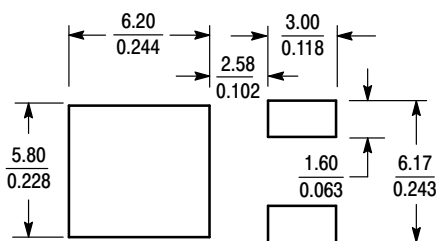


XXXXXX = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- STYLE 1:**
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR
- STYLE 2:**
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN
- STYLE 3:**
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. CATHODE
- STYLE 4:**
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE
- STYLE 5:**
 PIN 1. GATE
 2. ANODE
 3. CATHODE
 4. ANODE
- STYLE 6:**
 PIN 1. MT1
 2. MT2
 3. GATE
 4. MT2
- STYLE 7:**
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR
- STYLE 8:**
 PIN 1. N/C
 2. CATHODE
 3. ANODE
 4. CATHODE
- STYLE 9:**
 PIN 1. ANODE
 2. CATHODE
 3. RESISTOR ADJUST
 4. CATHODE
- STYLE 10:**
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. ANODE

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC TO-252	
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT	PAGE 1 OF 2

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